JZ8F8003

8 Bit FLASH Microcontroller Datasheet

VERSION V1.2

Revision History

Version	Revision Description	Note
V1.0	Finish the first draft	
V1.1	Modifying the Content Format	
V1.2	Add ESD description	P94

Statement:

- The content of this information will be updated as the product improves without prior notice. Please consult our sales staff before using this material to ensure that the content of this material is the latest version.
- Please use this product within the limit specified in this document. Our company will not be responsible for any loss caused by improper use.
- Although our company is always committed to improving product quality and reliability, semiconductor products have a certain probability of failure or wrong work. In order to prevent personal injury or property damage caused by such accidents, please pay full attention to safety design during use
- When exporting this product or this data overseas, it shall comply with applicable import and export control laws and regulations
- Without the permission of the Company, it is strictly prohibited to reproduce or reprint this material in any form, in whole or in part
- The test data in this document is for reference only. The actual data is subject to the test of the target prototype

Contents

1 General Description ..... - 8 -
1.1 Features ..... - 8 -
1.2 Pin Assignment ..... - 9 -
1.3 Pin Description ..... - 10 -
2 Memory Structure ..... - 13 -
3 Functional Description ..... - 17 -
3.1 Operational Registers ..... - 17 -
3.1.1 0x80(RSR): RAM Select Register ..... - 17 -
3.1.2 0x81(PCH): PC High Address Register(PCH) ..... - 17 -
3.1.3 0x82(PCL): PC Low Address Register(PCL) ..... - 17 -
3.1.4 0x83(STATUS): Status Register ..... - 18 -
3.1.5 0x84(TC0CON): TC0 Control Register ..... - 19 -
3.1.6 0x85(TC0C): TC0 register and counter ..... - 20 -
3.1.7 0x86(TBRDH): The TBRD table lookup points to the high level register ..... - 20 -
3.1.8 0x87(TBRDL): TBRD Table lookup points to low and EEPROM address register ..... - 20 -
3.1.9 0x88(CPUCON): CPU Clock Mode Selection Register ..... - 20 -
3.1.10 0x89(IRCCAL): IRC Frequency Adjustment Register ..... - 21 -
3.1.11 0x8A(PORT5): P5 Port Data Register ..... - 21 -
3.1.12 0x8B(PORT6): P6 Port Data Register ..... - 21 -
3.1.13 0x8C(PORT7): P7 Port Data Register ..... - 22 -
3.1.14 0x8D(P5CR): P5 Port control register ..... - 22 -
3.1.15 0x8E(P6CR): P6 Port control register ..... - 22 -
3.1.16 0x8F(P7CR): P7 Port control register ..... - 22 -
3.1.17 0x90(P5PHCR): P5 Pull-up Control register ..... - 22 -
3.1.18 0x91(P6PHCR): P6 Pull-up Control register ..... - 22 -
3.1.19 0x92(P7PHCR): P7 Pull-up Control register ..... - 23 -
3.1.20 0x93(P5PDCR): P5 Pull-down Control Register ..... - 23 -
3.1.21 0x94(P6PDCR): P6 Pull-down Control Register ..... - 23 -
3.1.22 0x95(P7PDCR): P7 Pull-down Control Register ..... - 23 -
3.1.23 0x96(P6ODCR): P6 open-drain Control Register ..... - 23 -
3.1.24 0x97(P5IWE): P5 changes Interrupt and Wake up Enable Control Register ..... - 23 -
3.1.25 0x98(P6IWE): P6 Change Interrupt, Wake Up Enable Control Register ..... - 24 -
3.1.26 0x99(P7IWE): P7 Changes Interrupt and Wake Up Enable Control Register ..... - 24 -
3.1.27 0x9A(P5HDCR): P5 High pull Current Control Register ..... - 24 -
3.1.28 0x9B(P6HDCR): P6 High pull Current Control Register ..... - 24 -
3.1.29 0x9C(P7HDCR): P7 High pull Current Control Register ..... - 24 -
3.1.30 0x9D(P5HSCR): P5 High Irrigation Current Control Register ..... - 24 -
3.1.31 0x9E(P6HSCR): P6 High Irrigation Current Control Register ..... - 25 -
3.1.32 0x9F(P7HSCR): P7 High Irrigation Current Control Register ..... - 25 -
3.1.33 0xA0(P5ADE): P5 AD input port Selection control register ..... - 25 -
3.1.34 0xA1(P6ADE): P6 AD input port Selection control register ..... - 25 -
3.1.35 0xA2(P7ADE): P7 AD input port Selection control register ..... - 25 -

3.1.36 0xA3(ADDATA): ADC conversion result high 8-bit register ..... - 26 -
3.1.37 0xA4(ADDATA1H): ADC conversion result high 4-bit register ..... - 26 -
3.1.38 0xA5(ADDATA1L): Low 8-bit register of ADC conversion result ..... - 26 -
3.1.39 0xA6(ADIGS): ADC input and trigger source control register ..... - 26 -
3.1.40 0xA7(ADOC): ADC Voltage and Compensation Calibration control register ..... - 27 -
3.1.41 0xA8(ADCON): ADC control register ..... - 28 -
3.1.42 0xAD(CMPCON): Comparator and OP-amp control register ..... - 29 -
3.1.43 0xAE(LVDCON): LVD control register ..... - 29 -
3.1.44 0xAF(WDTCON): WDT control register ..... - 30 -
3.1.45 0xB0(PWM0CON): T0/PWM0 control register ..... - 30 -
3.1.46 0xB1(PWM0RD): PWM0 period register ..... - 31 -
3.1.47 0xB2(PWM0DT): PWM0 duty cycle register ..... - 31 -
3.1.48 0xB3(TMR0): T0 timer register ..... - 31 -
3.1.49 0xB4(PWM1CON): T1/PWM1 control register ..... - 32 -
3.1.50 0xB5(PWM1RD): PWM1 period register ..... - 32 -
3.1.51 0xB6(PWM1DT): PWM1 duty cycle register ..... - 32 -
3.1.52 0xB7(TMR1): T1 timer register ..... - 33 -
3.1.53 0xB8(PWM2CON): T2/PWM2 control register ..... - 33 -
3.1.54 0xB9(PWM2RD): PWM2 period register ..... - 33 -
3.1.55 0xBA(PWM2DT): PWM2 duty cycle register ..... - 34 -
3.1.56 0xBB(TMR2): T2 timer register ..... - 34 -
3.1.57 0xBC(PWM3CON): T3/PWM3 control register ..... - 34 -
3.1.58 0xBD(PWM3RD): PWM3 period register ..... - 35 -
3.1.59 0xBE(PWM3DT): PWM3 duty cycle register ..... - 35 -
3.1.60 0xBF(TMR3): T3 timer register ..... - 35 -
3.1.61 0xC9(PWMCS): PWM Cascade and dead zone control register ..... - 35 -
3.1.62 0xCA(PWMDEADT): PWM deadzone time control register ..... - 36 -
3.1.63 0xCB(PWMIS1): PWM Port Mapping Control Register 1 ..... - 36 -
3.1.64 0xCC(PWMIS2): PWM Port Mapping Control Register 2 ..... - 36 -
3.1.65 0xD0(TC1CON): TC1 control register ..... - 37 -
3.1.66 0xD1(TC1CH): TC1 high level counter and register ..... - 38 -
3.1.67 0xD2(TC1CL): TC1 low level counter and register ..... - 38 -
3.1.68 0xD5(EINTR): External Interrupt Control Register ..... - 38 -
3.1.69 0xD6(IMR1): Interrupts Enable control register 1 ..... - 39 -
3.1.70 0xD7(IMR2): Interrupts Enable control register 2 ..... - 39 -
3.1.71 0xDA(ISR1): Interrupt flag register 1 ..... - 39 -
3.1.72 0xDB(ISR2): Interrupt flag register 2 ..... - 40 -
3.1.73 0xDE(WECR): Wakes up the enable control register ..... - 40 -
3.1.74 0xE0(EEPCON): EP2 Read/Write Control Register ..... - 41 -
3.1.75 0xE1(EEPDAT): EEPROM write data register ..... - 41 -
3.1.76 0xFF(IAR): Indirection address register ..... - 41 -
3.2 GPIO Function Module ..... - 42 -
3.2.1 GPIO Register Description ..... - 42 -
0x8A(PORT5): P5 port data register ..... - 42 -
0x8B(PORT6): P6 port data register ..... - 42 -

0x8C(PORT7): P7 port data register ..... - 42 -
0x8D(P5CR): P5 port control register ..... - 42 -
0x8E(P6CR): P6 port control register ..... - 42 -
0x8F(P7CR): P7 port control register ..... - 42 -
0x90(P5PHCR): P5 Pull-up control register ..... - 43 -
0x91(P6PHCR): P6 Pull-up control register ..... - 43 -
0x92(P7PHCR): P7 Pull-up control register ..... - 43 -
0x93(P5PDCR): P5 Pull-down control register ..... - 43 -
0x94(P6PDCR): P6 Pull-down control register ..... - 43 -
0x95(P7PDCR): P7 Pull-down control register ..... - 43 -
0x96(P6ODCR): P6 drain open control register ..... - 44 -
0x9A(P5HDCR): P5 High pull current control register ..... - 44 -
0x9B(P6HDCR): P6 High pull current control register ..... - 44 -
0x9C(P7HDCR): P7 high pull current control register ..... - 44 -
0x9D(P5HSCR): P5 High irrigation current control register ..... - 44 -
0x9E(P6HSCR): P6 high irrigation current control register ..... - 44 -
0x9F(P7HSCR): P7 high irrigation current control register ..... - 45 -
3.2.2 Wake Up when the Port Status Changes ..... - 45 -
3.3 Timer ..... - 47 -
3.3.1 TC0 timing counter ..... - 47 -
3.3.1.1 TC0 Timing Settings ..... - 47 -
3.3.1.2 TC0 Timing Calculation Description ..... - 47 -
3.3.1.3 TC0 Wake Up in Idle Mode ..... - 48 -
3.3.2 TC1 timing counter ..... - 48 -
3.3.2.1 TC1 8Bit Timing Settings ..... - 49 -
3.3.2.2 TC1 16Bit Timing Settings ..... - 49 -
3.3.2.3 TC1 Timing Calculation Description ..... - 49 -
3.3.2.4 TC1 Wake Up in Idle Mode ..... - 50 -
3.4 LVD Function Module ..... - 51 -
3.4.1 LVD Voltage Detection Settings ..... - 51 -
3.5 ADC Function Module ..... - 52 -
3.5.1 ADC Register ..... - 52 -
0xA0(P5ADE): P5 AD input port selection control register ..... - 52 -
0xA1(P6ADE): P6 AD input port selection control register ..... - 52 -
0xA2(P7ADE): P7 AD input port selection control register ..... - 53 -
0xA3(ADDATA): high 8-bit register of ADC conversion result ..... - 53 -
0xA4(ADDATA1H): ADC conversion result high 4 bit register ..... - 53 -
0xA5(ADDATA1L): Low 8-bit register of ADC conversion result ..... - 53 -
0xA6(ADIGS): ADC input and trigger source control register ..... - 53 -
0xA7(ADOC): ADC voltage and compensation calibration control register ..... - 54 -
0xA8(ADCON): ADC control register ..... - 55 -
3.5.2 ADC analog-to-digital conversion Settings ..... - 56 -
3.5.3 ADC analog-to-digital conversion Settings ..... - 56 -
3.6 PWM Function Module ..... - 57 -
3.6.1 PWM Register ..... - 57 -

0xB0(PWM0CON): T0/PWM0 control register ..... - 57 -
0xB1(PWM0RD): PWM0 period register ..... - 58 -
0xB2(PWM0DT): PWM0 duty cycle register ..... - 58 -
0xB4(PWM1CON): T1/PWM1 control register ..... - 58 -
0xB5(PWM1RD): PWM1 cycle register ..... - 59 -
0xB6(PWM1DT): PWM1 duty cycle register ..... - 59 -
0xB8(PWM2CON): T2/PWM2 control register ..... - 59 -
0xB9(PWM2RD): PWM2 period register ..... - 60 -
0xBA(PWM2DT): PWM2 duty cycle register ..... - 60 -
0xBC(PWM3CON): T3/PWM3 control register ..... - 60 -
0xBD(PWM3RD): PWM3 cycle register ..... - 61 -
0xBE(PWM3DT): PWM3 duty cycle register ..... - 61 -
0xC9(PWMCS): PWM cascade and dead zone control register ..... - 61 -
0xCA(PWMDEADT): PWM deadzone time control register ..... - 62 -
0xCB(PWMIS1): PWM port mapping control register 1 ..... - 62 -
0xCC(PWMIS2): PWM port mapping control register 2 ..... - 62 -
3.6.2 PWM Period and Duty Cycle ..... - 63 -
3.6.3 Cascade 16-Bit PWM ..... - 64 -
3.6.4 PWM Deadzone Control Description ..... - 65 -
3.6.5 Wake Up in Idle Mode of PWM ..... - 65 -
3.6.6 PWM Setting Description ..... - 65 -
3.7 CMP/OP Function Module ..... - 66 -
3.7.1 CMP/OP Register ..... - 66 -
0xAD(CMPCON): Comparator and OP amp control register ..... - 66 -
3.7.2 CMP Setting Instructions ..... - 67 -
3.7.3 OP Setting Instructions ..... - 67 -
3.8 Interrupt Function Module ..... - 68 -
3.8.1 Interrupt Register ..... - 69 -
0xD5(EINTR): External Interrupt control register ..... - 69 -
0xD6(IMR1): Interrupt enable control register 1 ..... - 69 -
0xD7(IMR2): Interrupts enable control register 2 ..... - 70 -
0xDA(ISR1): Interrupt flag register 1 ..... - 70 -
0xDB(ISR2): Interrupt flag register 2 ..... - 70 -
3.8.2 Interrupting On-site Protection ..... - 71 -
3.9 Reset Function Module ..... - 72 -
3.9.1 Overview ..... - 72 -
3.9.2 Restarting the POR ..... - 72 -
3.9.3 WDT Reset ..... - 73 -
3.9.4 LVR Low-voltage Reset ..... - 73 -
3.9.5 Operating frequency and LVR Low voltage reset ..... - 74 -
3.10 System Clock Function Module ..... - 76 -
3.10.1 Internal RC oscillator ..... - 76 -
3.10.2 External crystal/ceramic oscillator ..... - 76 -
3.11 Working Mode ..... - 78 -
3.11.1 High-speed Mode ..... - 79 -

3.11.2 Low-speed Mode ..... - 79 -
3.11.3 Idle Mode ..... - 79 -
3.11.4 Sleep Mode ..... - 80 -
3.12 EEPROM Live erasable Programmable memory ..... - 81 -
3.12.1 EEPROM Application Description ..... - 81 -
4 CODE OPTION Configuration table ..... - 82 -
5 Electrical characteristics ..... - 84 -
5.1 IC Limiting Characteristics ..... - 84 -
5.2 DC Electrical Characteristics ..... - 84 -
5.3 Feature Curve ..... - 86 -
5.3.1 Internal low speed 128K RC oscillator - voltage frequency characteristic curve ..... - 86 -
5.3.2 Internal low speed 128K RC oscillator -- temperature-frequency characteristic curve ..... - 86 -
5.3.3 Internal 1Mhz RC oscillator - voltage frequency characteristic curve ..... - 87 -
5.3.4 Internal 1Mhz RC oscillator - temperature-frequency characteristic curve ..... - 87 -
5.3.5 Internal 4Mhz RC oscillator - voltage frequency characteristic curve ..... - 88 -
5.3.6 Internal 4Mhz RC oscillator -- temperature-frequency characteristic curve ..... - 88 -
5.3.7 Internal 8Mhz RC oscillator - voltage frequency characteristic curve ..... - 89 -
5.3.8 Internal 8Mhz RC oscillator -- temperature-frequency characteristic curve ..... - 89 -
5.3.9 Internal 16Mhz RC oscillator - voltage frequency characteristic curve ..... - 90 -
5.3.10 Internal 16Mhz RC oscillator -- temperature-frequency characteristic curve ..... - 90 -
6 Packaging Configuration ..... - 91 -
6.1 SOP20PIN Packaging ..... - 91 -
6.2 QFN20 Packaging ..... - 92 -
6.3 TSSOP20 Packaging ..... - 93 -
7 ESD performance description ..... - 94 -

1 General Description

1.1 Features

CPU Configuration

- 8K×16-Bit MTP ROM
- 128×8-Bit EEPROM
- 256×8-Bit SRAM
- 12-level stacks
- 4 programmable Level Voltage Detector
  4.5V, 4.0V, 3.3V, 2.2V
- 4 programmable Level Voltage Reset
  4.2V, 3.7V, 2.9V, 1.8V
- Operating current less than 3 mA
  (4MHz/5V)
- Operating current less than 10 μA
  (16KHz/3V)
- Operating current less than 1 μA
  (Sleep mode)

I/O Port Configuration

- 3 bidirectional I/O:P5, P6, P7
- 18 I/O pins
- Wake-up port:P5、P6、P7
- 18 programmable pull-up I/O pins
- 18 programmable pull-down I/O pins
- 8 programmable open-drain I/O pins
- 18 programmable high-sink current I/O pins
- External interrupt:
  INT1(P65/P50)
  INT0(P67/P51)

Operating Voltage

- Operating voltage range:
  1.8V～5.5V (0℃-70℃)
  2.3V～5.5V (-40℃-85℃)
- EEPROM voltage range:
  2.6V～5.5V(-45℃-85℃)

Operating Frequency range

- Internal RC Oscillator Mode:
  16MHz, 8MHz, 4MHz, 1MHz
- External RC Oscillator Mode
- External XT Oscillator Circuit:
  DC～16MHz (more than 4.5V)
  DC～8MHz (more than 3V)
  DC～4MHz (more than 2.5V)
- Clock Cycle Frequency Division:
  2Clock, 4Clock, 8Clock, 16Clock

Peripheral Configuration

- 8Bit real-time clock/counter TC0
- 8Bit/16bit counter TC1
- 18 Channel 12 Bit ADC
- Two pairs of CMP or OP AMP
- 4 pairs of 8Bit Complementary pulse width modulator PWM
- Two sets of 16Bit PWM can be cascaded separately

Interrupts

- TC0 overflow interrupt
- TC1 overflow interrupt
- Input port status changed interrupt
- External interrupt0
- External interrupt1
- ADC completion interrupt
- Comparator status changed interrupt 0
- Comparator status changed interrupt 1
- PWM0 period/duty match interrupt
- PWM1 period/duty match interrupt
- PWM2 period/duty match interrupt
- PWM3 period/duty match interrupt

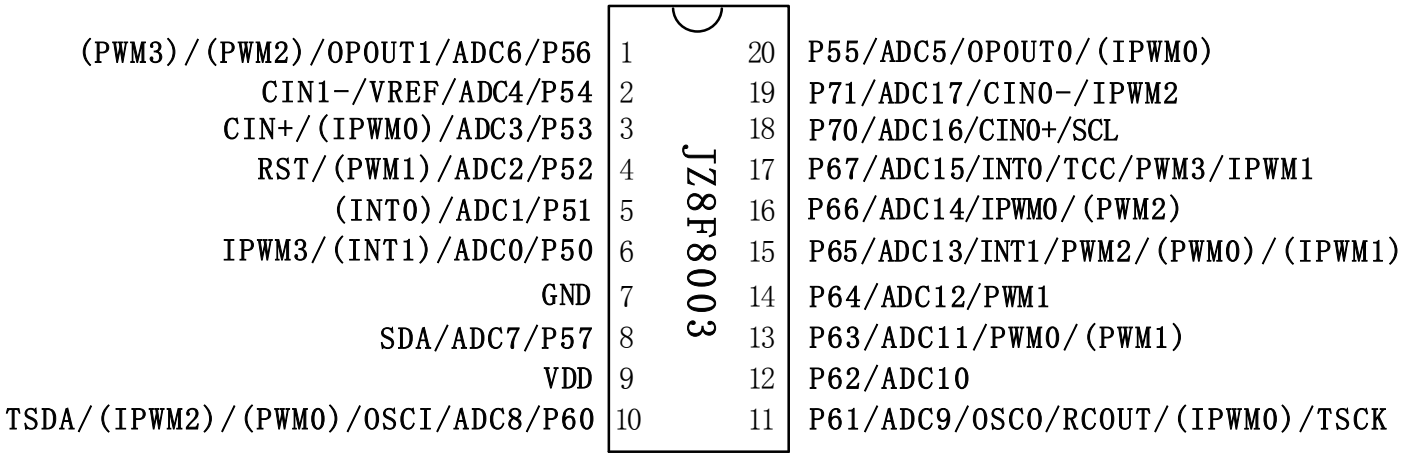
Features

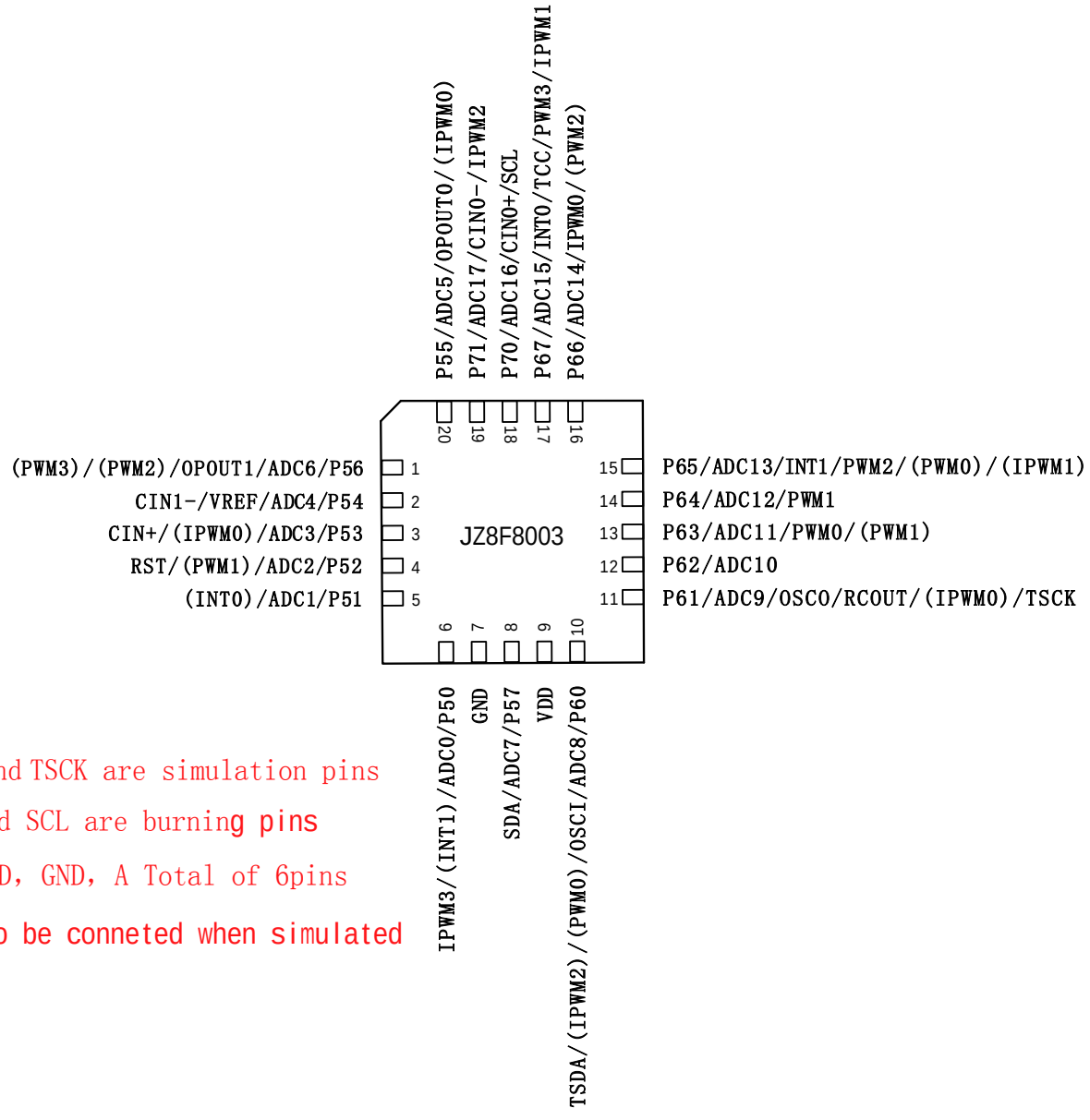
- Programmable Watchdog Timer
- 4 working modes switch
- RTC Dual-clock timing mode

Package Type

- JZ8F8003-SOP20/TSSOP20;
- JZ8F8003-QFN20;

1.2 Pin Assignment





NOTE: TSDA and TSCK are simulation pins
SDA and SCL are burning pins
and VDD, GND, A Total of 6pins
need to be conneted when simulated

1.3 Pin Description

Name	Pin	I/O	Description
P50	P50	I/O	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC0	AN	ADC Input 0
	IPWM3	CMOS	IPWM3 output
	INT1	I	External interrupt Input 1
P51	P51	I/O	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC1	AN	ADC Input 1
	INT0	I	External interrupt Input 0
P52	P52	I/O	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC2	AN	ADC Input 2
	PWM1	CMOS	PWM1 output
	RST	I	System reset pin
P53	P53	I/O	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC3	AN	ADC Input 3
	IPWM0	CMOS	IPWM0 output
	CIN1+	AN	Comparator 1 input “+” end
P54	P54	I/O	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC4	AN	ADC Input 4
	VREF	AN	ADC external voltage reference
	CIN1-	AN	Comparator 1 input “-” end
P55	P55	I/O	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC5	AN	ADC Input 5
	IPWM0	CMOS	IPWM0 output
	OPOUT0	O	Comparator 0 output
P56	P56	I/O	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC6	AN	ADC Input 6
	PWM2	CMOS	PWM2 output
	PWM3	CMOS	PWM3 output
	OPOUT1	O	Comparator 1 output
P57	P57	I/O	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC7	AN	ADC Input7

P60	P60	I/O	Bidirectional I/O pin with with programmable open-drain pull-down, pull-high, high-driver, high-sink and pin change
	ADC8	AN	ADC Input 8
	PWM0	CMOS	PWM0 output
	IPWM2	CMOS	IPWM2 output
	OSCI	I	Clock input of crystal oscillator
P61	P61	I/O	Bidirectional I/O pin with with programmable open-drain pull-down, pull-high, high-driver, high-sink and pin change
	ADC9	AN	ADC Input 9
	IPWM0	CMOS	IPWM0 output
	RCOUT	O	Clock output of RC oscillator
	OSCO	O	Clock output of crystal oscillator
P62	P62	I/O	Bidirectional I/O pin with with programmable open-drain pull-down, pull-high, high-driver, high-sink and pin change
	ADC10	AN	ADC Input 10
P63	P63	I/O	Bidirectional I/O pin with with programmable open-drain pull-down, pull-high, high-driver, high-sink and pin change
	ADC11	AN	ADC Input 11
	PWM0	CMOS	PWM0 output
	PWM1	CMOS	PWM1 output
P64	P64	I/O	Bidirectional I/O pin with with programmable open-drain pull-down, pull-high, high-driver, high-sink and pin change
	ADC12	AN	ADC Input 12
	PWM1	CMOS	PWM1 output
P65	P65	I/O	Bidirectional I/O pin with with programmable open-drain pull-down, pull-high, high-driver, high-sink and pin change
	ADC13	AN	ADC Input 13
	PWM0	CMOS	PWM0 output
	IPWM1	CMOS	IPWM1 output
	PWM2	CMOS	PWM2 output
	INT1	I	External interrupt Input 1
P66	P66	I/O	Bidirectional I/O pin with with programmable open-drain pull-down, pull-high, high-driver, high-sink and pin change
	ADC14	AN	ADC Input 14
	IPWM0	CMOS	IPWM0 output
	PWM2	CMOS	PWM2 output
P67	P67	I/O	Bidirectional I/O pin with with programmable open-drain pull-down, pull-high, high-driver, high-sink and pin change
	ADC15	AN	ADC Input 15
	IPWM1	CMOS	IPWM1 output
	PWM3	CMOS	PWM3 output

	INT0	I	External interrupt Input 0
	TC0	I	TC0 External clock Input
P70	P70	I/O	Bidirectional I/O pin with with programmable pull-down, pull-high, high-driver, high-sink and pin change
	ADC16	AN	ADC Input 16
	CIN0+	AN	Comparator 0 input “+” end
P71	P71	I/O	Bidirectional I/O pin with with programmable pull-down, pull-high, high-driver, high-sink and pin change
	ADC17	AN	ADC Input 17
	IPWM2	CMOS	IPWM2 output
	CIN0-	AN	Comparator 0 input “-” end
	VDD	--	Power
	VSS	--	Ground

2 Memory Structure

Direct addressing/Indirect addressing RAM 0x00	
……	
……	
……	
0x7f	
Indirect addressing RAM 0x80	Direct addressing SFR 0x80
……	……
……	……
……	……
0xff	0xff

Address	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
0x80	FSR<7>	FSR<6>	FSR<5>	FSR<4>	FSR<3>	FSR<2>	FSR<1>	FSR<0>
0x81				PC<12>	PC<11>	PC<10>	PC<9>	PC<8>
0x82	PC<7>	PC<6>	PC<5>	PC<4>	PC<3>	PC<2>	PC<1>	PC<0>
0x83	RST	INT	LVD	T	P	Z	DC	C
0x84	RTCEN	RTCS	TS	TE	PSTC0E	PSTC0<2>	PSTC0<1>	PSTC0<0>
0x85	TC0<7>	TC0<6>	TC0<5>	TC0<4>	TC0<3>	TC0<2>	TC0<1>	TC0<0>
0x86				RBIT<12>	RBIT<11>	RBIT<10>	RBIT<9>	RBIT<8>
0x87	RBIT<7>	RBIT<6>	RBIT<5>	RBIT<4>	RBIT<3>	RBIT<2>	RBIT<1>	RBIT<0>
0x88			DB_EN	TIMERSC	CPUS	IDEL	RCM<1>	RCM<0>
0x89		INCAL<6>	INCAL<5>	INCAL<4>	INCAL<3>	INCAL<2>	INCAL<1>	INCAL<0>
0x8A	P5<7>	P5<6>	P5<5>	P5<4>	P5<3>	P5<2>	P5<1>	P5<0>
0x8B	P6<7>	P6<6>	P6<5>	P6<4>	P6<3>	P6<2>	P6<1>	P6<0>
0x8C							P7<1>	P7<0>
0x8D	C5<7>	C5<6>	C5<5>	C5<4>	C5<3>	C5<2>	C5<1>	C5<0>
0x8E	C6<7>	C6<6>	C6<5>	C6<4>	C6<3>	C6<2>	C6<1>	C6<0>
0x8F							C7<1>	C7<0>
0x90	PH5<7>	PH5<6>	PH5<5>	PH5<4>	PH5<3>	PH5<2>	PH5<1>	PH5<0>
0x91	PH6<7>	PH6<6>	PH6<5>	PH6<4>	PH6<3>	PH6<2>	PH6<1>	PH6<0>
0x92							PH7<1>	PH7<0>
0x93	PD5<7>	PD5<6>	PD5<5>	PD5<4>	PD5<3>	PD5<2>	PD5<1>	PD5<0>
0x94	PD6<7>	PD6<6>	PD6<5>	PD6<4>	PD6<3>	PD6<2>	PD6<1>	PD6<0>
0x95							PD7<1>	PD7<0>
0x96	P6OD<7>	P6OD<6>	P6OD<5>	P6OD<4>	P6OD<3>	P6OD<2>	P6OD<1>	P6OD<0>
0x97	IWE5<7>	IWE5<6>	IWE5<5>	IWE5<4>	IWE5<3>	IWE5<2>	IWE5<1>	IWE5<0>

0x98	IWE6<7>	IWE6<6>	IWE6<5>	IWE6<4>	IWE6<3>	IWE6<2>	IWE6<1>	IWE6<0>
0x99							IWE7<1>	IWE7<0>
0x9A	HD5<7>	HD5<6>	HD5<5>	HD5<4>	HD5<3>	HD5<2>	HD5<1>	HD5<0>
0x9B	HD6<7>	HD6<6>	HD6<5>	HD6<4>	HD6<3>	HD6<2>	HD6<1>	HD6<0>
0x9C							HD7<1>	HD7<0>
0x9D	HS5<7>	HS5<6>	HS5<5>	HS5<4>	HS5<3>	HS5<2>	HS5<1>	HS5<0>
0x9E	HS6<7>	HS6<6>	HS6<5>	HS6<4>	HS6<3>	HS6<2>	HS6<1>	HS6<0>
0x9F							HS7<1>	HS7<0>
0xA0	ADE5<7>	ADE5<6>	ADE5<5>	ADE5<4>	ADE5<3>	ADE5<2>	ADE5<1>	ADE5<0>
0xA1	ADE6<7>	ADE6<6>	ADE6<5>	ADE6<4>	ADE6<3>	ADE6<2>	ADE6<1>	ADE6<0>
0xA2							ADE7<1>	ADE7<0>
0xA3	AD<11>	AD<10>	AD<9>	AD<8>	AD<7>	AD<7>	AD<5>	AD<4>
0xA4					AD<11>	AD<10>	AD<9>	AD<8>
0xA5	AD<7>	AD<6>	AD<5>	AD<4>	AD<3>	AD<2>	AD<1>	AD<0>
0xA6	TRIGS<2>	TRIGS<1>	TRIGS<0>	ADIS<4>	ADIS<3>	ADIS<2>	ADIS<1>	ADIS<0>
0xA7	VREFS	VREF<1>	VREF<0>	CALI	SIGN	VOF<2>	VOF<1>	VOF<0>
0xA8	ADEN	ADRUN		ADTRS	ADSH<1>	ADSH<0>	ADCKR<1>	ADCKR<0>
0xA9								
0xAA								
0xAB								
0xAC								
0xAD	CMP<1>	CMP<0>	CIN1S	CIN0S	COS1<1>	COS1<0>	COS0<1>	COS0<0>
0xAE	LVDEN						LVD<1>	LVD<0>
0xAF	WDTE				PSWE	PSW<2>	PSW<1>	PSW<0>
0xB0	T0EN	IPWM0A	PWM0A	IPWM0E	PWM0E	PST0<2>	PST0<1>	PST0<0>
0xB1	PRD0<7>	PRD0<6>	PRD0<5>	PRD0<4>	PRD0<3>	PRD0<2>	PRD0<1>	PRD0<0>
0xB2	DT0<7>	DT0<6>	DT0<5>	DT0<4>	DT0<3>	DT0<2>	DT0<1>	DT0<0>
0xB3	T0<7>	T0<6>	T0<5>	T0<4>	T0<3>	T0<2>	T0<1>	T0<0>
0xB4	T1EN	IPWM1A	PWM1A	IPWM1E	PWM1E	PST1<2>	PST1<1>	PST1<0>
0xB5	PRD1<7>	PRD1<6>	PRD1<5>	PRD1<4>	PRD1<3>	PRD1<2>	PRD1<1>	PRD1<0>
0xB6	DT1<7>	DT1<6>	DT1<5>	DT1<4>	DT1<3>	DT1<2>	DT1<1>	DT1<0>
0xB7	T1<7>	T1<6>	T1<5>	T1<4>	T1<3>	T1<2>	T1<1>	T1<0>
0xB8	T2EN	IPWM2A	PWM2A	IPWM2E	PWM2E	PST2<2>	PST2<1>	PST2<0>
0xB9	PRD2<7>	PRD2<6>	PRD2<5>	PRD2<4>	PRD2<3>	PRD2<2>	PRD2<1>	PRD2<0>
0xBA	DT2<7>	DT2<6>	DT2<5>	DT2<4>	DT2<3>	DT2<2>	DT2<1>	DT2<0>
0xBB	T2<7>	T2<6>	T2<5>	T2<4>	T2<3>	T2<2>	T2<1>	T2<0>
0xBC	T3EN	IPWM3A	PWM3A	IPWM3E	PWM3E	PST3<2>	PST3<1>	PST3<0>
0xBD	PRD3<7>	PRD3<6>	PRD3<5>	PRD3<4>	PRD3<3>	PRD3<2>	PRD3<1>	PRD3<0>
0xBE	DT3<7>	DT3<6>	DT3<5>	DT3<4>	DT3<3>	DT3<2>	DT3<1>	DT3<0>
0xBF	T3<7>	T3<6>	T3<5>	T3<4>	T3<3>	T3<2>	T3<1>	T3<0>
0xC0								

0xC1								
0xC2								
0xC3								
0xC4								
0xC5								
0xC6								
0xC7								
0xC8								
0xC9	PWMCAS1	PWMCAS0	DEADT3E	DEADT2E	DEADT1E	DEADT0E	PSTD<1>	PSTD<0>
0xCA	DEADT<7>	DEADT<6>	DEADT<5>	DEADT<4>	DEADT<3>	DEADT<2>	DEADT<1>	DEADT<0>
0xCB	IPWM1S<1>	IPWM1S<0>	PWM1S<1>	PWM1S<0>	IPWM0S<1>	IPWM0S<0>	PWM0S<1>	PWM0S<0>
0xCC	IPWM3S<1>	IPWM3S<0>	PWM3S<1>	PWM3S<0>	IPWM2S<1>	IPWM2S<0>	PWM2S<1>	PWM2S<0>
0xCD								
0xCE								
0xCF								
0xD0	TC1EN		RELOAD	TC1HEN	PSTC1E	PSTC1<2>	PSTC1<1>	PSTC1<0>
0xD1	TC1<15>	TC1<14>	TC1<13>	TC1<12>	TC1<11>	TC1<10>	TC1<9>	TC1<8>
0xD2	TC1<7>	TC1<6>	TC1<5>	TC1<4>	TC1<3>	TC1<2>	TC1<1>	TC1<0>
0xD3								
0xD4								
0xD5	NRE1	INTEG1	EXPS1	EIS1	NRE0	INTEG0	EXPS0	EIS0
0xD6	TC1IE	CMP1IE	CMP0IE	ADIE	EX1IE	EX0IE	ICIE	TC0IE
0xD7	DT3IE	DT2IE	DT1IE	DT0IE	PWM3IE	PWM2IE	PWM1IE	PWM0IE
0xD8								
0xD9								
0xDA	TC1IF	CMP1IF	CMP0IF	ADIF	EX1IF	EX0IF	ICIF	TC0IF
0xDB	DT3IF	DT2IF	DT1IF	DT0IF	PWM3IF	PWM2IF	PWM1IF	PWM0IF
0xDC								
0xDD								
0xDE	WDTWE	CMP1WE	CMP0WE	ADWE	EX1WE	EX0WE	ICWE	TMRWE
0xDF								
0xE0						EE_WRERR	EEREAD	EEWRIT
0xE1	EEDIN<7>	EEDIN<6>	EEDIN<5>	EEDIN<4>	EEDIN<3>	EEDIN<2>	EEDIN<1>	EEDIN<0>
0xE2								
0xE3								
0xE4								
0xE5								
0xE6								
0xE7								
0xE8								
0xE9								

0xEA								
0xEB								
0xEC								
0xED								
0xEE								
0xEF								
0xF0								
0xF1								
0xF2								
0xF3								
0xF4								
0xF5								
0xF6								
0xF7								
0xF8								
0xF9								
0xFA								
0xFB								
0xFC								
0xFD								
0xFE								
0xFF	IAR<7>	IAR<6>	IAR<5>	IAR<4>	IAR<3>	IAR<2>	IAR<1>	IAR<0>

3 Functional Description

3.1 Operational Registers

3.1.1 0x80(RSR): RAM Select Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
FSR<7>	FSR<6>	FSR<5>	FSR<4>	FSR<3>	FSR<2>	FSR<1>	FSR<0>

For RAM selection in indirect addressing mode(Address 0x00~0xff)

The RSR register is used in conjunction with the IAR register for indirect addressing operations。The user can put the address corresponding to a register into the RSR, The indirect addressing register IAR is then accessed, The address will then point to the register of the corresponding address in the RSR。

NOTE:RAM storage area addresses 0X00 to 0X7F can be addressed directly or indirectly, addresses 0X80 to 0XFF can only be addressed indirectly。

3.1.2 0x81(PCH): PC High Address Register(PCH)

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	PC<12>	PC<11>	PC<10>	PC<9>	PC<8>

3.1.3 0x82(PCL): PC Low Address Register(PCL)

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PC<7>	PC<6>	PC<5>	PC<4>	PC<3>	PC<2>	PC<1>	PC<0>

A program counter (PC) is a pointer that records the instructions to be processed by the CPU during each instruction cycle. During the CPU cycle, the PC pushes the instruction pointer into the program memory and then incrementalizes the pointer by one to proceed to the next cycle. The JZ8M8003 has a 13-bit wide program counter (PC) with low bytes from the read-write PCL and high bytes from the read-write PCH.

The JZ8M8003 stack is used to record the instruction pointer returned by the program. When the subroutine is called, the PC presses the instruction pointer on the stack. When the return instruction is executed, the stack sends the instruction pointer back to the PC and continues the original process. The JZ8M8003 has a 12-level stack that takes up neither program nor data storage space, and the stack pointer cannot read or write.

- The PC and hardware stack is 13 bits wide
- Generate 8K 16-bit on-chip MTP ROM address to address the corresponding program instruction code. A program page is 1024 words long.
- During the reset, all bits of the PC are set to 0.

▪ The "JMP" instruction loads 13 bits of a program counter directly. Thus, the "JMP" instruction allows the PC to jump to any location in the program.

▪ The "CALL" instruction first loads the PC's 13 bits, then pushes the PC+1 onto the stack. Therefore, the subroutine entry address can be located anywhere in the program.

▪ The "RET" ("RETL k", "RETI") instruction loads the stack top value to the current PC.

▪ "ADD PCL, A" adds a relative address to the current PC, with the ninth digit of the PC and above incremented.

▪ "MOV PCL, A" can load an address from the "A" register to the lower 8 Bit of the PC, the ninth bit of the PC and above remain unchanged.

▪ Any instruction (other than the "ADD PCL,A" instruction) that writes values to R2 (e.g. "MOV PCL, A", "BC PCL, 6") will leave the high level of PC (PC12 to PC9) unchanged.

▪ Any instruction other than "TBRD R" is a single instruction cycle.

3.1.4 0x83(STATUS): Status Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
RST	INT	LVD_FG	T	P	Z	DC	C

Bit<7>: RST-Bit of reset type
0: Other reset types
1: Wake-up from sleep on pin change, comparator status change, or AD conversion completed.
Bit<6>: INT-Interrupt Enable flag
0: Disabled by DISI or hardware interrupt
1: Enabled by the ENI/RETI instructions
Bit<5>: LVD_FG-Low voltage Detector state (Read only)
0: Low voltage is detected
1: Low voltage is not detected or LVD function is disabled
Bit<4>: T-Time-out bit
0: WDT time-out
1: Set to "1" by the "SLEEP" and "CWDT" commands or during power on
Bit<3>: P-Power-down bit
0: Execute SLEEP instruction
1: Power on reset or Execute CWDT instruction
Affect T/P event shown in the following table:

Type	RST	T	P
Power on reset	0	1	1
Press RESET under working mode	0	hold	hold
RESET wake up	0	1	0
WDT overflow in working mode	0	0	hold

WDT overflow wake	0	0	0
Port state changes wake up	1	1	0
Execute WDTC instruction	hold	1	1
Execute SLEEP instruction	hold	1	0

Bit<2>: Z-Zero flag

0: When arithmetic or logic is not zero

1: When arithmetic or logic is 0

Bit<1>:DC: Auxiliary carry flag

0: When the addition operation is performed, the lower four bits are not carried. When performing a subtraction operation, the lower four bits borrow

1: When performing the addition operation, the lower four bits have carry; When subtracting, the lower four bits do not borrow

Bit<0>:C: Carry flag

0: When the addition operation is performed, the higher four bits are not carried. When performing a subtraction operation, the high four bits borrow

1: When the addition operation is performed, the higher four bits have carry. When performing a subtraction operation, the high four digits do not borrow

3.1.5 0x84(TC0CON): TC0 Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
RTCEN	RTCS	TS	TE	PSTC0E	PSTC0<2>	PSTC0<1>	PSTC0<0>

Bit<7>:RTCEN-RTC enable bit

0:Disable RTC

1:Enable RTC (Need to synchronize the RTC function in OPTION)

Bit<6>:RTCS-RTC select bit

0:Internal system clock or external input clock as TC0 clock source (selected by TS)

1:RTC is the TC0 clock source

Bit<5>:TS-TC0 Clock Source Selection

0:Internal system clock (master/secondary clock selected by TIMERSC)

1:External input clock, P67 input TC0 clock signal

Bit<4>:TE-TC0 external clock signal along selection

0:When the transmitted signal on the TC0 pin changes from low to high, TC0 adds 1

1:TC0 plus 1 when the transmitted signal on the TC0 pin changes from high to low

Bit<3>:PSTC0E-TC0 Enables predivision

0:Pre-division is prohibited,and TC0 frequency division ratio is 1:1

1:Pre-division is enabled.TC0 frequency division ratio is set by Bit2~Bit0

Bit<2:0>:PSTC02~ PSTC00-TC0 predivision selection

PSTC0<2>	PSTC0<1>	PSTC0<2>	TC0frequency division ratio

0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.6 0x85(TC0C): TC0 register and counter

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TC0<7>	TC0<6>	TC0<5>	TC0<4>	TC0<3>	TC0<2>	TC0<1>	TC0<0>

The TC0 is an 8Bit upstream counter, the clock source is optional internal/external clock, count overflow can form interrupts, and the TC0C register can be read and written.

TC0 can be triggered by the signal edge on the P67 pin to produce a plus 1 operation. If 1 PSTC0E is set, a pre-divider will be assigned to TC0. When the TC0 register or TC0 pre-divider is assigned a value, the value of the pre-divider will be cleared to 0.

3.1.7 0x86(TBRDH): The TBRD table lookup points to the high level register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	RBIT<12>	RBIT<11>	RBIT<10>	RBIT<9>	RBIT<8>

3.1.8 0x87(TBRDL): TBRD Table lookup points to low and EEPROM address register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
RBIT<7>	RBIT<6>	RBIT<5>	RBIT<4>	RBIT<3>	RBIT<2>	RBIT<1>	RBIT<0>

3.1.9 0x88(CPUCON): CPU Clock Mode Selection Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	DB_EN	TIMERSC	CPUS	IDEL	RCM<1>	RCM<0>

Bit<5>:DB_EN-PWM clock frequency doubling is selected
0: Disable
1: Enable
Bit<4>:TIMERSC-TC0, TC1, PWM0, PWM1, PWM2, PWM3 Clock source selection
0:Fs(secondary clock, low speed oscillator)
1:Fm(master clock, high speed oscillator)

Bit<3>:CPUS-select a clock source

0:Fs(secondary clock, low speed oscillator)

1:Fm(master clock, high speed oscillator)

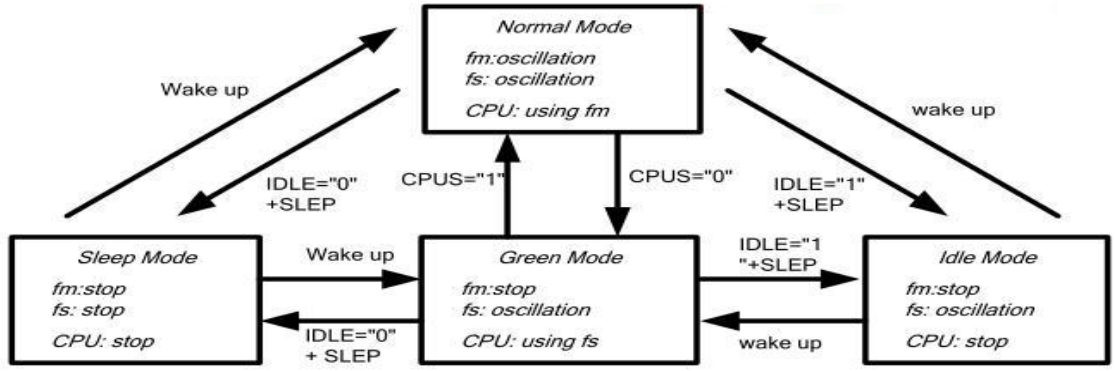
When CPUS=0, the CPU oscillator chooses the secondary oscillator and the primary oscillator stops.

Bit<2>:IDLE-Indicates the idle mode enablement bit

1: Enter idle mode after executing SLEEP (CPU stops, peripherals do not stop)

0: Enter the SLEEP mode after executing sleep (CPU+ peripherals are stopped)

This bit determines which working mode the CPU will enter after executing the SLEEP instruction



Bit<1:0>:RCM1:RCM0-IRC mode selection bit

RCM1	RCM0	Frequency （Mhz）
1	1	4
1	0	16
0	1	8
0	0	1

3.1.10 0x89(IRCCAL): IRC Frequency Adjustment Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	INCAL<6>	INCAL<5>	INCAL<4>	INCAL<3>	INCAL<2>	INCAL<1>	INCAL<0>

3.1.11 0x8A(PORT5): P5 Port Data Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
P5<7>	P5<6>	P5<5>	P5<4>	P5<3>	P5<2>	P5<1>	P5<0>

3.1.12 0x8B(PORT6): P6 Port Data Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
P6<7>	P6<6>	P6<5>	P6<4>	P6<3>	P6<2>	P6<1>	P6<0>

3.1.13 0x8C(PORT7): P7 Port Data Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	P7<1>	P7<0>

3.1.14 0x8D(P5CR): P5 Port control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
C5<7>	C5<6>	C5<5>	C5<4>	C5<3>	C5<2>	C5<1>	C5<0>

P5 direction control bit:

0: Output

1: Input

3.1.15 0x8E(P6CR): P6 Port control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
C6<7>	C6<6>	C6<5>	C6<4>	C6<3>	C6<2>	C6<1>	C6<0>

P6 direction control bit:

0: Output

1: Input

3.1.16 0x8F(P7CR): P7 Port control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	C7<1>	C7<0>

P7 direction control bit:

0: Output

1: Input

3.1.17 0x90(P5PHCR): P5 Pull-up Control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PH5<7>	PH5<6>	PH5<5>	PH5<4>	PH5<3>	PH5<2>	PH5<1>	PH5<0>

P5 Pull up control bit:

0: Enable

1: Forbidden

3.1.18 0x91(P6PHCR): P6 Pull-up Control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PH6<7>	PH6<6>	PH6<5>	PH6<4>	PH6<3>	PH6<2>	PH6<1>	PH6<0>

P6 Pull up control bit:

0: Enable

1: Forbidden

3.1.19 0x92(P7PHCR): P7 Pull-up Control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	PH7<1>	PH7<0>

P7 Pull up control bit:

0: Enable

1: Forbidden

3.1.20 0x93(P5PDCR): P5 Pull-down Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PD5<7>	PD5<6>	PD5<5>	PD5<4>	PD5<3>	PD5<2>	PD5<1>	PD5<0>

P5 Pull-down control bit:

0: Enable

1: Forbidden

3.1.21 0x94(P6PDCR): P6 Pull-down Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PD6<7>	PD6<6>	PD6<5>	PD6<4>	PD6<3>	PD6<2>	PD6<1>	PD6<0>

P6 Pull-down control bit:

0: Enable

1: Forbidden

3.1.22 0x95(P7PDCR): P7 Pull-down Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	PD7<1>	PD7<0>

P7 Pull-down control bit:

0: Enable

1: Forbidden

3.1.23 0x96(P6ODCR): P6 open-drain Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
P6OD<7>	P6OD<6>	P6OD<5>	P6OD<4>	P6OD<3>	P6OD<2>	P6OD<1>	P6OD<0>

P6 open drain output control bit:

0: Disable

1: Enable

3.1.24 0x97(P5IWE): P5 changes Interrupt and Wake up Enable Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
IWE5<7>	IWE5<6>	IWE5<5>	IWE5<4>	IWE5<3>	IWE5<2>	IWE5<1>	IWE5<0>

P5 Port status changes Wake up control bit:

0: Disable

1: Enable

3.1.25 0x98(P6IWE): P6 Change Interrupt, Wake Up Enable Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
IWE6<7>	IWE6<6>	IWE6<5>	IWE6<4>	IWE6<3>	IWE6<2>	IWE6<1>	IWE6<0>

P6 Port status change Wake up control bit:

0: Disable

1: Enable

3.1.26 0x99(P7IWE): P7 Changes Interrupt and Wake Up Enable Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	IWE7<1>	IWE7<0>

P7 Port status change Wake up control bit:

0: Disable

1: Enable

3.1.27 0x9A(P5HDCR): P5 High pull Current Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
HD5<7>	HD5<6>	HD5<5>	HD5<4>	HD5<3>	HD5<2>	HD5<1>	HD5<0>

P5 port pull current enhancement control bit:

0: Disable

1: Enable

3.1.28 0x9B(P6HDCR): P6 High pull Current Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
HD6<7>	HD6<6>	HD6<5>	HD6<4>	HD6<3>	HD6<2>	HD6<1>	HD6<0>

P6 port pull current enhancement control bit:

0: Disable

1: Enable

3.1.29 0x9C(P7HDCR): P7 High pull Current Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	HD7<1>	HD7<0>

P7 port pull current enhancement control bit:

0: Disable

1: Enable

3.1.30 0x9D(P5HSCR): P5 High Irrigation Current Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
HS5<7>	HS5<6>	HS5<5>	HS5<4>	HS5<3>	HS5<2>	HS5<1>	HS5<0>

P5 port irrigation current enhanced control bit:
0: Disable
1: Enable

3.1.31 0x9E(P6HSCR): P6 High Irrigation Current Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
HS6<7>	HS6<6>	HS6<5>	HS6<4>	HS6<3>	HS6<2>	HS6<1>	HS6<0>

P6 port irrigation current enhanced control bit:
0: Disable
1: Enable

3.1.32 0x9F(P7HSCR): P7 High Irrigation Current Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	HS7<1>	HS7<0>

P7 port irrigation current enhanced control bit:
0: Disable
1: Enable

3.1.33 0xA0(P5ADE): P5 AD input port Selection control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
ADE5<7>	ADE5<6>	ADE5<5>	ADE5<4>	ADE5<3>	ADE5<2>	ADE5<1>	ADE5<0>

P5 ADC input selection control bit:
0: The port is set to GPIO
1: The port is set as an analog input port

3.1.34 0xA1(P6ADE): P6 AD input port Selection control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
ADE6<7>	ADE6<6>	ADE6<5>	ADE6<4>	ADE6<3>	ADE6<2>	ADE6<1>	ADE6<0>

P6 ADC input selection control bit:
0: The port is set to GPIO
1: The port is set as an analog input port

3.1.35 0xA2(P7ADE): P7 AD input port Selection control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	ADE7<1>	ADE7<0>

P7 ADC input selection control bit:
0: The port is set to GPIO
1: The port is set as an analog input port

3.1.36 0xA3(ADDATA): ADC conversion result high 8-bit register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
AD<11>	AD<10>	AD<9>	AD<8>	AD<7>	AD<7>	AD<5>	AD<4>

read-only

3.1.37 0xA4(ADDATA1H): ADC conversion result high 4-bit register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	AD<11>	AD<10>	AD<9>	AD<8>

read-only

3.1.38 0xA5(ADDATA1L): Low 8-bit register of ADC conversion result

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
AD<7>	AD<6>	AD<5>	AD<4>	AD<3>	AD<2>	AD<1>	AD<0>

read-only

3.1.39 0xA6(ADIGS): ADC input and trigger source control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TRIGS<2>	TRIGS<1>	TRIGS<0>	ADIS<4>	ADIS<3>	ADIS<2>	ADIS<1>	ADIS<0>

Bit<7:5>:TRIGS<2: 0>-ADC 触发源选择位 （使能 ADTRS 有效）

TRIGS2	TRIGS1	TRIGS0	Trigger source selection
0	0	0	PWM0 Duty cycle
0	0	1	PWM0 period
0	1	0	PWM1 Duty cycle
0	1	1	PWM1 period
1	0	0	PWM2 Duty cycle
1	0	1	PWM2 cycle
1	1	0	PWM3 Duty cycle
1	1	1	PWM3 cycle

Bit<4:0>:ADIS<4:0>-ADC analog input channel selection

ADIS4	ADIS3	ADIS2	ADIS1	ADIS0	Analog input
0	0	0	0	0	ADIN0/P50
0	0	0	0	1	ADIN1/P51
0	0	0	1	0	ADIN2/P52
0	0	0	1	1	ADIN3/P53

0	0	1	0	0	ADIN4/P54
0	0	1	0	1	ADIN5/P55
0	0	1	1	0	ADIN6/P56
0	0	1	1	1	ADIN7/P57
0	1	0	0	0	ADIN8/P60
0	1	0	0	1	ADIN9/P61
0	1	0	1	0	ADIN10/P62
0	1	0	1	1	ADIN11/P63
0	1	1	0	0	ADIN12/P64
0	1	1	0	1	ADIN13/P65
0	1	1	1	0	ADIN14/P66
0	1	1	1	1	ADIN15/P67
1	0	0	0	0	ADIN16/P70
1	0	0	0	1	ADIN17/P71
1	0	0	1	0	ADIN18/1/4vdd
1	0	0	1	1	ADIN19/AMP0
1	0	1	0	0	ADIN20/AMP1

3.1.40 0xA7(ADOC): ADC Voltage and Compensation Calibration control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
VREFS	VREF<1>	VREF<0>	CALI	SIGN	VOF<2>	VOF<1>	VOF<0>

Bit<7> : VREFS-ADC reference voltage source selection

0: internal reference voltage, VDD as ADC reference voltage, P54 as GPIO

1: External reference voltage, P54 pin voltage as ADC reference voltage

Bit<6:5> : VREF<1:0> -ADC internal reference voltage selection

VREF1	VREF0	Internal reference voltage
0	0	VDD
0	1	4V
1	0	3V
1	1	2V

Bit<4> : CALi-ADc-Compensatory calibration enable bit

0: Disable

1: indicates that the function is enabled

Bit<3> : SIGN-ADC- compensates the voltage polarity selection bit

0: indicates the negative voltage

1: positive voltage

Bit<2:0> : VOF<2:0>- Compensatory voltage selection

VOF2	VOF1	VOF0	Range of compensation
0	0	0	0 LSB
0	0	1	2LSB
0	1	0	4 LSB
0	1	1	6LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

3.1.41 0xA8(ADCON): ADC control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
ADEN	ADRUN	-	ADTRS	ADSH<1>	ADSH<0>	ADCKR<1>	ADCKR<0>

Bit<7>:ADPD-ADC power enable bit

0: disables the ADC power supply

1: Enables the ADC power supply

Bit<6>:ADRUN-ADC start up control bit

0: ADC conversion ends, and the system automatically sets the bit, which cannot be reset by software

1: ADC conversion begins. This bit can be set by software

Bit<5>:not used

Bit<4>:ADTRS-ADC triggers source selection bits

0: The startup is enabled by the ADRUN software

1: is started by PWM duty ratio, period overflow, or ADRUN software

Bit<3:2>:ADSH<1:0> -ADC sampling and hold time selection (at least 4us is recommended, TAD:ADC running clock period)

ADSH1	ADSH0	TAD
0	0	2 * TAD
0	1	4 * TAD
1	0	8 * TAD
1	1	12 * TAD

Bit<1:0>:ADCKR<1:0> -ADC clock predivision selection

ADCKR1	ADCKR0	ADC clock division ratio
0	0	2 * TAD
0	1	4 * TAD
1	0	8 * TAD
1	1	12 * TAD

3.1.42 0xAD(CMPCON): Comparator and OP-amp control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
CMP<1>	CMP<0>	CIN1S	CIN0S	COS1<1>	COS1<0>	COS0<1>	COS0<0>

Bit<7>:CMP1-Output bit of comparator 1

Note: Read CMP1 before enabling CMP1IE or CMP1WE.

Bit<6>:CMP0-comparator 0 output bit

Note: Read CMP0 before enabling CMP0IE or CMP0WE.

Bit<5>:CIN1S-Comparator 1 or opamp 1CIN- Input selection

0:CIN1-Select P54 port

1:CIN1-Select the internal VREF reference voltage

Bit<4>:CIN0S-comparator 0 or opamp 0CIN- Input selection

0:CIN1-Select P71 port

1:CIN1-Select the internal VREF reference voltage

Bit<3:2>:COS1<1:0> -CMP/OP1 function selection bit

COS11	COS10	Function Description
0	0	Comparator 1 and op amp 1 are not used, and P53, P54 and P56 are used as normal IO pins
0	1	P53 and P54 serve as comparator 1 input pins, and P56 serves as ordinary IO pins
1	0	P53 and P54 serve as input pins for comparator 1, and P56 serves as output pins for comparator 1
1	1	P53 and P54 are input pins of op amp 1, and P56 is output pins of op amp 1

Bit<1:0>:COS0<1:0> -CMP/OP0 function selection bit

COS01	COS00	Function Description
0	0	Comparator 0 and op amp 0 are not used, P70, P71 and P55 are used as normal IO pins
0	1	P70 and P71 serve as comparator 0 input pins, and P55 serves as normal IO pins
1	0	P70 and P71 serve as input pins for comparator 0, and P55 serves as output pins for comparator 0
1	1	P70 and P71 are input pins of op amp 0, and P55 is output pins of op amp 0

3.1.43 0xAE(LVDCON): LVD control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
LVDEN	-	-	-	-	-	LVD<1>	LVD<0>

Bit<7>:LVDEN-Low voltage detection enable bit

0: Disable

1: Enable

Bit<6:2>:not used

Bit<1:0>:LVD<1:0> -Low voltage detection value selection

LVDEN	LVD<1:0>	LVD interrupt level	/LVD
1	11	VDD ≤ 2.2V	0
		VDD > 2.2V	1
1	10	VDD ≤ 3.3V	0
		VDD > 3.3V	1
1	01	VDD ≤ 4.0V	0
		VDD > 4.0V	1
1	00	VDD ≤ 4.5V	0
		VDD > 4.5V	1
0	XX	NA	1

3.1.44 0xAF(WDTCON): WDT control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
WDTE	-	-	-	PSWE	PSW<2>	PSW<1>	PSW<0>

Bit<7>:WDTE-Indicates the enable bit of the watchdog timer
0: Disable
1: Enable
Bit<6:4>:not used
Bit<3>:PSWE-watchdog pre-frequency division enable bit
0: Disable. The WDT frequency division ratio is 1:1
1: Enabled. WDT frequency division is set by Bit<2:0>
Bit<2:0>:PSW<2:0> -WDT Select the pre-division frequency ratio

PSW2	PSW1	PSW0	WDT frequency division ratio
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.45 0xB0(PWM0CON): T0/PWM0 control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T0EN	IPWM0A	PWM0A	IPWM0E	PWM0E	PST0<2>	PST0<1>	PST0<0>

Bit<7> : T0EN-PWM0 Indicates the timer enable bit
0: Disable

1: Enable

Bit<6> : IPWM0A-IPWM0 The output is inverted

0: indicates that the IPWM0 duty cycle is low

1: indicates that the IPWM0 duty cycle is high

Bit<5> : PWM0A-PWM0 The output is inverted

0: PWM0 The duty cycle is high

1: indicates that the PWM0 duty cycle is low

Bit<4> : IPWM0E-IPWM0 Indicates the output enable bit

0: indicates that IPWM0 is disabled

1: indicates that IPWM0 is enabled

Bit<3> : PWM0E-PWM0 Indicates the output enable bit

0: PWM0 Disable

1: PWM0 is enabled

Bit<2:0> : PST0<2:0> -T0 Select the clock divider

PST2	PST1	PST0	T0 frequency division ratio
0	0	0	1:1(default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.46 0xB1(PWM0RD): PWM0 period register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PRD0<7>	PRD0<6>	PRD0<5>	PRD0<4>	PRD0<3>	PRD0<2>	PRD0<1>	PRD0<0>

The time period (time basis) of PWM0. The frequency of PWM0 is the reciprocal of its period

3.1.47 0xB2(PWM0DT): PWM0 duty cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT0<7>	DT0<6>	DT0<5>	DT0<4>	DT0<3>	DT0<2>	DT0<1>	DT0<0>

Causes the output of PWM0 to remain high until its value matches a specific value of T0 content.

3.1.48 0xB3(TMR0): T0 timer register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T0<7>	T0<6>	T0<5>	T0<4>	T0<3>	T0<2>	T0<1>	T0<0>

read-only

3.1.49 0xB4(PWM1CON): T1/PWM1 control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T1EN	IPWM1A	PWM1A	IPWM1E	PWM1E	PST1<2>	PST1<1>	PST1<0>

Bit<7> : indicates the T1EN-PWM1 timer enablement bit
0: Disable
1: Enable
Bit<6> : IPWM1A-IPWM1 The output is inverted
0: IPWM1 duty cycle is low
1: IPWM1 duty cycle is high
Bit<5> : PWM1A-PWM1 The output is inverted
0: PWM1 duty cycle is high
1: PWM1 duty cycle is low
Bit<4> : IPWM1E-IPWM1 Indicates the output enablement bit
0: IPWM1 disabled
1: IPWM1 enabled
Bit<3> : PWM1E-PWM1 Indicates the output enable bit
0: PWM1 Disabled
1: PWM1 enabled
Bit<2:0>:PST1<2:0> -T1 Select the clock divider

PST12	PST11	PST10	T1 frequency division ratio
0	0	0	1:1(default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.50 0xB5(PWM1RD): PWM1 period register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PRD1<7>	PRD1<6>	PRD1<5>	PRD1<4>	PRD1<3>	PRD1<2>	PRD1<1>	PRD1<0>

The time period of PWM1 (time basis), the frequency of PWM1 is the reciprocal of its period

3.1.51 0xB6(PWM1DT): PWM1 duty cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT1<7>	DT1<6>	DT1<5>	DT1<4>	DT1<3>	DT1<2>	DT1<1>	DT1<0>

Keeps the output of PWM1 high until its value matches a specific value of T1 content.

3.1.52 0xB7(TMR1): T1 timer register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T1<7>	T1<6>	T1<5>	T1<4>	T1<3>	T1<2>	T1<1>	T1<0>

read-only

3.1.53 0xB8(PWM2CON): T2/PWM2 control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T2EN	IPWM2A	PWM2A	IPWM2E	PWM2E	PST2<2>	PST2<1>	PST2<0>

Bit<7> : indicates the T2EN-PWM2 timer enable bit
0: Disable
1: Enable
Bit<6> : IPWM2A-IPWM2 The output is inverted
0: indicates that the IPWM2 duty cycle is low
1: indicates that the IPWM2 duty cycle is high
Bit<5> : PWM2A-PWM2 The output is inverted
0: indicates that the PWM2 duty cycle is high
1: The PWM2 duty cycle is low
Bit<4> : IPWM2E-IPWM2 Indicates the output enablement bit
0: disables the IPWM2
1: indicates that IPWM2 is enabled
Bit<3> : PWM2E-PWM2 Indicates the output enablement bit
0: disables PWM2
1: The PWM2 function is enabled
Bit<2:0>:PST2<2:0> -T2 Select the clock divider

PST22	PST21	PST20	T2 frequency division ratio
0	0	0	1:1(default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.54 0xB9(PWM2RD): PWM2 period register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PRD2<7>	PRD2<6>	PRD2<5>	PRD2<4>	PRD2<3>	PRD2<2>	PRD2<1>	PRD2<0>

The time period of PWM2 (time basis), the frequency of PWM2 is the reciprocal of its period

3.1.55 0xBA(PWM2DT): PWM2 duty cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT2<7>	DT2<6>	DT2<5>	DT2<4>	DT2<3>	DT2<2>	DT2<1>	DT2<0>

Keeps the output of PWM2 high until its value matches a specific value of the contents of T2.

3.1.56 0xBB(TMR2): T2 timer register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T2<7>	T2<6>	T2<5>	T2<4>	T2<3>	T2<2>	T2<1>	T2<0>

read-only

3.1.57 0xBC(PWM3CON): T3/PWM3 control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T3EN	IPWM3A	PWM3A	IPWM3E	PWM3E	PST3<2>	PST3<1>	PST3<0>

Bit<7> : indicates the T3EN-PWM3 timer enablement bit
0: Disable
1: Enable
Bit<6> : IPWM3A-IPWM3 The output is inverted
0: indicates that the IPWM3 duty cycle is low
1: The IPWM3 duty cycle is high
Bit<5> : PWM3A-PWM3 The output is inverted
0: The PWM3 duty cycle is high
1: PWM3 duty cycle is low
Bit<4> : IPWM3E-IPWM3 Indicates the output enablement bit
0: disables IPWM3
1: IPWM3 is enabled
Bit<3> : PWM3E-PWM3 Indicates the output enable bit
0: disables PWM3
1: PWM3 is enabled
Bit<2:0>:PST3<2:0> -T3 Clock divider selection

PST32	PST31	PST30	T3 frequency division ratio
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.58 0xBD(PWM3RD): PWM3 period register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PRD3<7>	PRD3<6>	PRD3<5>	PRD3<4>	PRD3<3>	PRD3<2>	PRD3<1>	PRD3<0>

The time period (time basis) of PWM3. The frequency of PWM3 is the reciprocal of its period

3.1.59 0xBE(PWM3DT): PWM3 duty cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT3<7>	DT3<6>	DT3<5>	DT3<4>	DT3<3>	DT3<2>	DT3<1>	DT3<0>

Keeps the output of PWM3 high until its value matches a specific value for the contents of T3.

3.1.60 0xBF(TMR3): T3 timer register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T3<7>	T3<6>	T3<5>	T3<4>	T3<3>	T3<2>	T3<1>	T3<0>

read-only

3.1.61 0xC9(PWMCS): PWM Cascade and dead zone control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PWMCAS1	PWMCAS0	DEADT3E	DEADT2E	DEADT1E	DEADT0E	PSTD<1>	PSTD<0>

Bit<7> : PWMCAS1-PWM3 and PWM2 cascading mode is enabled
0: Disable, two independent 8-bit PWM
1: Enable, 16-bit PWM mode (cascaded by two 8-bit PWM)
Bit<6> : PWMCAS0-PWM1, PWM0 Cascading mode is enabled
0: Disable, two independent 8-bit PWM
1: Enable, 16-bit PWM mode (cascaded by two 8-bit PWM)
Bit<5> : DEADT3E-PWM3 Deadzone adjustment Enable control bit
0: Disable
1: Enable
Bit<4> : DEADT2E-PWM2 deadzone adjustment Enable control bit
0: Disable
1: Enable
Bit<3> : DEADT1E-PWM1 Deadzone adjustment Enables the control bit
0: Disable
1: Enable
Bit<2> : DEADT0E-PWM0 Deadzone adjustment Enable control bit
0: Disable
1: Enable
Bit<1:0>:PSTD<1:0> -Select a dead zone clock divider

PSTD1	PSTD0	Frequency division ratio
0	0	1:1 (default)

0	1	1:2
1	0	1:4
1	1	1:8

3.1.62 0xCA(PWMDEADT): PWM deadzone time control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DEADT<7>	DEADT<6>	DEADT<5>	DEADT<4>	DEADT<3>	DEADT<2>	DEADT<1>	DEADT<0>

Dead zone time setting, clock source with PWM (Fc)

3.1.63 0xCB(PWMIS1): PWM Port Mapping Control Register 1

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
IPWM1S<1>	IPWM1S<0>	PWM1S<1>	PWM1S<0>	IPWM0S<1>	IPWM0S<0>	PWM0S<1>	PWM0S<0>

Bit<7:6> : IPWM1S<7:6> -IPWM1 Indicates the port mapping selection

IPWM1S1	IPWM1S0	Mapping Port
0	0	P67 (default)
0	1	P65
1	0	none
1	1	none

Bit<5:4> : PWM1S <5:4> -PWM1 Indicates the port mapping selection

PWM1S1	PWM1S0	Mapping Port
0	0	P64 (default)
0	1	P63
1	0	P52
1	1	none

Bit<3:2> : IPWM0S <3:2> -IPWM0 Indicates the port mapping selection

IPWM0S1	IPWM0S0	Mapping Port
0	0	P66 (default)
0	1	P61
1	0	P55
1	1	P53

Bit<1:0> : PWM0S <1:0> -PWM0 Indicates the port mapping selection

PWM0S1	PWM0S0	Mapping Port
0	0	P63 (default)
0	1	P65
1	0	P60
1	1	none

3.1.64 0xCC(PWMIS2): PWM Port Mapping Control Register 2

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
IPWM3S<1>	IPWM3S<0>	PWM3S<1>	PWM3S<0>	IPWM2S<1>	IPWM2S<0>	PWM2S<1>	PWM2S<0>

Bit<7:6>:IPWM3S<7:6> -IPWM3 Indicates the port mapping selection

IPWM3S1	IPWM3S0	Mapping Port
0	0	P50(default)
0	1	none
1	0	none
1	1	none

Bit<5:4>:PWM1S <5:4> - PWM1 Indicates the port mapping selection

PWM3S1	PWM3S0	Mapping Port
0	0	P56(default)
0	1	P67
1	0	none
1	1	none

Bit<3:2>:IPWM0S <3:2> - IPWM0 Indicates the port mapping selection

IPWM2S1	IPWM2S0	Mapping Port
0	0	P71(default)
0	1	P60
1	0	none
1	1	none

Bit<1:0>:PWM0S <1:0> - PWM2 Indicates the port mapping selection

PWM2S1	PWM2S0	Mapping Port
0	0	P65(default)
0	1	P66
1	0	P56
1	1	none

3.1.65 0xD0(TC1CON): TC1 control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TC1EN	-	RELOAD	TC1HEN	PSTC1E	PSTC1<2>	PSTC1<1>	PSTC1<0>

Bit<7> : indicates the TC1EN-TC1 timer enablement bit
0: Disable
1: Enable
Bit<6> : not used
Bit<5> : RELOAD- Autoload enable bit in 8-bit mode
0: Disable
1: Enable
Bit<4> : TC1HEN- Indicates the 16-bit timer enablement bit
0: TC1 is an 8-bit timer
1: TC1 is a 16-bit timer
Bit<3> : indicates the PSTC1E-TC1 predivision enable bit
0: forbidden, TC1 frequency division ratio is 1:1
1: Enabled. TC1 frequency division is selected by Bit<2:0>
Bit<2:0>:PSTC1 <2:0> - TC1 predivision selection

PSTC1<2>	PSTC1<1>	PSTC1<0>	TC1 frequency division ratio
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.66 0xD1(TC1CH): TC1 high level counter and register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TC1<15>	TC1<14>	TC1<13>	TC1<12>	TC1<11>	TC1<10>	TC1<9>	TC1<8>

3.1.67 0xD2(TC1CL): TC1 low level counter and register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TC1<7>	TC1<6>	TC1<5>	TC1<4>	TC1<3>	TC1<2>	TC1<1>	TC1<0>

3.1.68 0xD5(EINTR): External Interrupt Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
NRE1	INTEG1	EXPS1	EIS1	NRE0	INTEG0	EXPS0	EIS0

Bit<7> : NRE1-INT1 Indicates the noise suppression enable bit
0: Disable
1: Enable, in low frequency crystal oscillator (LXT) mode or low speed mode, noise suppression circuit is always disabled
Bit<6> : INTEG1-INT1 indicates edge selection
0: Interrupt occurs at the rising edge of INT1 pin signal
1: Interrupt occurs at INT1 pin signal drop edge
Bit<5> : EXPS1-INT1 signal pin selection (do not switch between the two pins after EIS1 is enabled)
0: Select P65 as the INT1 signal pin
1: Select P50 as the INT1 signal pin
Bit<4> : EIS1-INT1 pin selection
0: P65/P50 indicates GPIO
1: P65/P50 is the external interrupt pin
Bit<3> : NRE0-INT0 Indicates the noise suppression enable bit
0: Disable
1: Enable, in low frequency crystal oscillator (LXT) mode or low speed mode, noise suppression circuit is always disabled
Bit<2> : INTEG0-INT0 indicates the edge selection of the signal

0: Interrupt occurs at the rising edge of the INT0 pin signal
1: Interrupt occurs at the drop edge of INT0 pin signal
Bit<1> : EXPS0-INT0 pin selection (do not switch between the two pins after EIS0 is enabled)
0: Select P67 for INT0 signal pin
1: Select P51 for INT0 signal pin
Bit<0> : EIS0-INT0 pin selection
0: P67/P51 indicates GPIO
1: P67/P51 are external interrupt pins

3.1.69 0xD6(IMR1): Interrupts Enable control register 1

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TC1IE	CMP1IE	CMP0IE	ADIE	EX1IE	EX0IE	ICIE	TC0IE

Bit<7> : TC1IE - TC1 interrupt enable bit
Bit<6> : CMP1IE - CMP1 interrupt enable bit
Bit<5> : CMP0IE - CMP0 interrupt enable bit
Bit<4> : ADIE - ADC interrupt enable bit
Bit<3> : EX1IE -int1 interrupt enable bit
Bit<2> : EX0IE -int0 interrupt enable bit
Bit<1> : ICIE - IC interrupt enable bit
Bit<0> : TC0IE - TC0 interrupt enable bit
0: Disable
1: Enable

3.1.70 0xD7(IMR2): Interrupts Enable control register 2

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT3IE	DT2IE	DT1IE	DT0IE	PWM3IE	PWM2IE	PWM1IE	PWM0IE

Bit<7> : DT3IE -DT3 interrupt enable bit
Bit<6> : DT2IE - DT2 interrupt enable bit
Bit<5> : DT1IE - DT1 interrupt enable bit
Bit<4> : DT0IE - DT0 interrupt enable bit
Bit<3> : PWM3IE - PWM3 interrupt enable bit
Bit<2> : PWM2IE - PWM2 interrupt enable bit
Bit<1> : PWM1IE - PWM1 interrupt enable bit
Bit<0> : PWM0IE - PWM0 interrupt enable bit
0: Disable
1: Enable

3.1.71 0xDA(ISR1): Interrupt flag register 1

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TC1IF	CMP1IF	CMP0IF	ADIF	EX1IF	EX0IF	ICIF	TC0IF

Bit<7>:TC1IF - TC1 interrupt flag bit
Bit<6>:CMP1IF - CMP 1interrupt flag bit, set when comparator 1 output changes

Bit<5>:CMP0IF - CMP0 interrupt flag bit, set when comparator 0 output changes
Bit<4>:ADIF - ADC interrupt flag bit
Bit<3>:EX1IF - INT1 interrupt flag bit
Bit<2>:EX0IF - INT0 interrupt flag bit
Bit<1>:ICIF - IC interrupt flag bit
Bit<0>:TC0IF - TC0 interrupt flag bit
0: No interrupt is triggered
1: Triggers an interrupt

3.1.72 0xDB(ISR2): Interrupt flag register 2

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT3IF	DT2IF	DT1IF	DT0IF	PWM3IF	PWM2IF	PWM1IF	PWM0IF

Bit<7>:DT3IF - DT3 interrupt flag bit
Bit<6>:DT2IF - DT2 interrupt flag bit
Bit<5>:DT1IF - DT1 interrupt flag bit
Bit<4>:DT0IF - DT0 interrupt flag bit
Bit<3>:PWM3IF - PWM3 interrupt flag bit
Bit<2>:PWM2IF - PWM2 interrupt flag bit
Bit<1>:PWM1IF - PWM1 interrupt flag bit
Bit<0>:PWM0IF - PWM0 interrupt flag bit
0: No interrupt is triggered
1: Triggers an interrupt

3.1.73 0xDE(WECR): Wakes up the enable control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
WDTWE	CMP1WE	CMP0WE	ADWE	EX1WE	EX0WE	ICWE	TMRWE

Bit<7>:WDTWE - WDT Wake up enable bit
0: disables WDT wake up
1: Enable WDT wake up (After enabling WDT wake up, WDT reset fails, and the wake up period is half of the WDT reset time)
Bit<6>:CMP1WE - CMP1 Wake up enable bit
0: disables CMP1 from waking up
1: Enable CMP1 wake up
Bit<5>:CMP0WE - CMP0 Wake up enable bit
0: disables CMP0 wake-up
1: Enable CMP0 wake up
Bit<4>:ADWE - ADC Wake up enable bit
0: disables ADC wake up
1: Enable ADC wake up
Bit<3>:EX1WE - INT1 Wake up enable bit
0: disables INT1 from waking up
1: enables INT1 to wake up
Bit<2>:EX0WE - INT0 Wake up enable bit

0: disables INT0 from waking up
1: enables INT0 to wake up

Bit<1>:ICWE - IC Wake up enable bit
0: Disable IC wake up
1: Enable IC wake up

Bit<0>:TMRWE - PWM/DT/TC0/TC1 Wake up enable bit
0: disables PWM/DT/TC0/TC1 from waking up
1: Enable PWM/DT/TC0/TC1 wake up

3.1.74 0xE0(EEPCON): EP2 Read/Write Control Register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	EE_WRERR	EEREAD	EEWRIT

Bit<7:3>:未使用

Bit<2>:EE_WRERR - EEPROM write error flag bit
0: The EEPROM is written correctly
1: EEPROM write error, software clear 0

Bit<1>:EEREAD - EEPROM Read enable bit
0: The EEPROM reading is disabled
1: Enable EEPROM reading (TBRD R instruction)

Bit<0>:EEWRIT - EEPROM write enable bit
0: Disable EEPROM writing
1: Enable EEPROM write (After the write operation is complete, the hardware automatically clears 0 bits)

3.1.75 0xE1(EEPDAT): EEPROM write data register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
EEDIN<7>	EEDIN<6>	EEDIN<5>	EEDIN<4>	EEDIN<3>	EEDIN<2>	EEDIN<1>	EEDIN<0>

3.1.76 0xFF(IAR): Indirection address register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
IAR<7>	IAR<6>	IAR<5>	IAR<4>	IAR<3>	IAR<2>	IAR<1>	IAR<0>

The indirection register is not an actual register; its main function is to serve as a pointer to indirection.Any instruction that uses RFF as a pointer actually addresses the data pointed to by R80 (RAM selection register) RSR<7:0>.

3.2 GPIO Function Module

The JZ8M8003 has three sets of two-way I/O ports with a total of 18 inputs and 18 outputs. Most of the I/O can be reused for other functions.
18 programmable pull-up I/O pins: P50 ~ P57, P60 ~ P67, P70 ~ P71;
18 programmable pull-down I/O pins: P50 ~ P57, P60 ~ P67, P70 ~ P71;
18 programmable drive enhanced I/O pins: P50 ~ P57, P60 ~ P67, P70 ~ P71;
8 programmable drain open circuit I/O pins: P60 ~ P67;
The port input feature table is as follows (for reference only) :

3.2.1 GPIO Register Description

0x8A(PORT5): P5 port data register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
P5<7>	P5<6>	P5<5>	P5<4>	P5<3>	P5<2>	P5<1>	P5<0>

0x8B(PORT6): P6 port data register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
P6<7>	P6<6>	P6<5>	P6<4>	P6<3>	P6<2>	P6<1>	P6<0>

0x8C(PORT7): P7 port data register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	P7<1>	P7<0>

0x8D(P5CR): P5 port control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
C5<7>	C5<6>	C5<5>	C5<4>	C5<3>	C5<2>	C5<1>	C5<0>

P5 direction control bit:
0: Output
1: Input

0x8E(P6CR): P6 port control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
C6<7>	C6<6>	C6<5>	C6<4>	C6<3>	C6<2>	C6<1>	C6<0>

P6 direction control bit:
0: Output
1: Input

0x8F(P7CR): P7 port control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	C7<1>	C7<0>

P7 direction control bit:
0: Output
1: Input

0x90(P5PHCR): P5 Pull-up control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PH5<7>	PH5<6>	PH5<5>	PH5<4>	PH5<3>	PH5<2>	PH5<1>	PH5<0>

P5 Pull up control bit:

0: Enable

1: Forbidden

0x91(P6PHCR): P6 Pull-up control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PH6<7>	PH6<6>	PH6<5>	PH6<4>	PH6<3>	PH6<2>	PH6<1>	PH6<0>

P6 Pull up control bit:

0: Enable

1: Forbidden

0x92(P7PHCR): P7 Pull-up control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	PH7<1>	PH7<0>

P7 Pull up control bit:

0: Enable

1: Forbidden

0x93(P5PDCR): P5 Pull-down control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PD5<7>	PD5<6>	PD5<5>	PD5<4>	PD5<3>	PD5<2>	PD5<1>	PD5<0>

P5 Pull down control bit:

0: Enable

1: Forbidden

0x94(P6PDCR): P6 Pull-down control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PD6<7>	PD6<6>	PD6<5>	PD6<4>	PD6<3>	PD6<2>	PD6<1>	PD6<0>

P6 Pull down control bit:

0: Enable

1: Forbidden

0x95(P7PDCR): P7 Pull-down control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	PD7<1>	PD7<0>

P7 Pull down control bit:

0: Enable

1: Forbidden

0x96(P6ODCR): P6 drain open control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
P6OD<7>	P6OD<6>	P6OD<5>	P6OD<4>	P6OD<3>	P6OD<2>	P6OD<1>	P6OD<0>

P6 open drain output control bit:

0: Disable

1: Enable

0x9A(P5HDCR): P5 High pull current control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
HD5<7>	HD5<6>	HD5<5>	HD5<4>	HD5<3>	HD5<2>	HD5<1>	HD5<0>

P5 port pull-current enhancement control bit:

0: Disable

1: Enable

0x9B(P6HDCR): P6 High pull current control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
HD6<7>	HD6<6>	HD6<5>	HD6<4>	HD6<3>	HD6<2>	HD6<1>	HD6<0>

P6 port pull-current enhancement control bit:

0: Disable

1: Enable

0x9C(P7HDCR): P7 high pull current control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	HD7<1>	HD7<0>

P7 port pull-current enhancement control bit:

0: Disable

1: Enable

0x9D(P5HSCR): P5 High irrigation current control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
HS5<7>	HS5<6>	HS5<5>	HS5<4>	HS5<3>	HS5<2>	HS5<1>	HS5<0>

P5 port irrigation current enhanced control bit:

0: Disable

1: Enable

0x9E(P6HSCR): P6 high irrigation current control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
HS6<7>	HS6<6>	HS6<5>	HS6<4>	HS6<3>	HS6<2>	HS6<1>	HS6<0>

P6 port irrigation current enhanced control bit:

0: Disable

1: Enable

0x9F(P7HSCR): P7 high irrigation current control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	HS7<1>	HS7<0>

P7 port irrigation current enhanced control bit:

0: Disable

1: Enable

3.2.2 Wake Up when the Port Status Changes

The JZ8F8003 contains 18 programmable ports to wake up I/O with state changes: P50 to P57, P60 to P67, and P70 to P71. The chip executes the "SLEEP" command to enter the sleep mode or idle mode. At this point, the system clock stops and the CPU does not execute instructions. When the port status changes, the program can choose to continue the original process (DI before SLEEP) or execute the corresponding jump (EI before SLEEP), and open the corresponding enable control bit to jump to the interrupt subroutine.

Port status changes Query mode Wake up Settings:

1. PORT Port status changes. The wake port is set to input.
2. You can select the internal pull up or pull down of the wake up port according to your needs;
3. Enable port status change to wake up control P5IWE /P6IWE /P7IWE;
4. Set the ICWE bit of register RDE to 1 to enable the wake up function;
5. Run the DI command without entering the interrupt address interface;
6. Execute the "SLEEP" command, IDLE=0 to enter the sleep mode or IDLE=1 to enter the idle mode;
7. After wake up, execute the next instruction of SLEEP;

Port status changes Interrupt mode Wake up Settings:

1. PORT Port status changes. The wake port is set to input.
2. You can select the internal pull up or pull down of the wake up port according to your needs;
3. Enable port status change to wake up control P5IWE /P6IWE /P7IWE;
4. Set the ICWE bit of register RDE to 1 to enable the wake up function
5. Enable port status change to interrupt ICIE;
6. Execute the "EI" command and wait to enter the interrupt address port;

7. Execute the "SLEEP" command, IDLE=0 to enter the sleep mode or IDLE=1 to enter the idle mode;

8. After waking up, it will enter the interrupt address port. After exiting the interrupt, execute the next instruction of SLEEP;

3.3 Timer

3.3.1 TC0 timing counter

The TC0 timing counter provides an 8-bit pre-divider. The PSTC0E bit of the TC0CON register determines whether the divider can be enabled or disabled. The PSTC0<2:0> three-bit determines the pre-divider ratio. In TC0 mode, each time TC0 is written to a value, the pre-split register is cleared to zero.

TC0 is an 8Bit upstream counter that works as long as there is a clock. The clock source can be either internal clock Fc (optional Fm/Fs via TIMERSC) or external clock (input by P67 pin, trigger along optional). If there is no frequency division control, each clock (Fm/Fs) cycle (select internal clock) or each external clock cycle (external clock) arrives, the counter implementation adds 1.

TC0 count overflow can form interrupt signals.

In IDLE mode, TC0 interrupt can wake up the circuit. After wake up, you can choose to interrupt or continue to execute the original program. For the method, refer to the port state change to wake up. In sleep mode, the TC0 set to P67 external input clock can interrupt the overflow and wake up the circuit.

3.3.1.1 TC0 Timing Settings

1. Assign an initial value to the TC0C register;

2, set the value of the TC0CON register (select as a timer or counter and pre-division frequency ratio);

3. For counter use, it is necessary to select the TC0 external signal as positive edge or negative edge plus 1 in the TC0CON register;

4. Enable TC0IE of IMR1 register to enable interrupt and execute EI instruction;

5. The interrupt program will automatically save ACC, STATUS and RSR, and clear the TC0 interrupt flag bit after the execution of RETI instruction;

3.3.1.2 TC0 Timing Calculation Description

The TC0 timing function assigns an initial value to the timer by writing the value to the TC0C register. The timer accumulates from the initial value position until the timer overflows and generates an interrupt.

TC0 timing time calculation formula (select internal system clock):

TC0 timing time = (1/Fc)*(TC1 frequency division)*(256-TC1L initial value)

For example:

Fc=Fm(TIMERSC=1)=8 MHz, TC0 frequency division selection =8 frequency division, TC0C initial value =156;

TC0 timing time= (1/8) *(8)*(256-156)=100us

TC0 timing time calculation formula (select external input clock):

TC0 timing time = (1/ external input clock)*(TC0 frequency division)*(256-TC0C initial value)

For example:

External input clock = 1MHz, TC0 frequency division selection =4 frequency division, TC0C initial value =156;

TC0 timing time= (1/1) *(4)*(256-156)=400us

3.3.1.3 TC0 Wake Up in Idle Mode

In idle mode, the program stops execution, the module with the wake-up function and the low speed oscillator work properly, and other functions are disabled.

TC0 can wake up idle mode, set TIMERSC Bit4 of R88/CPUCON register to 0, and select TC0 clock source as secondary clock. Enable the TC0IE, IDLE = 1+ SLEEP command. The system enters the idle mode and the TC0 timer works normally. When the TC0 timer overflows, the system wakes up and enters the low-speed mode. If EI is enabled, it will wake up and enter the interrupt. If DI is executed, it will wake up and execute the next instruction.

3.3.2 TC1 timing counter

The TC1 timing counter provides an 8-bit pre-divider. The PSTC1E bit of the TC1CON register determines whether the divider can be enabled or disabled. The PSTC1<2:0> three-bit determines the pre-divider ratio. In TC01 mode, each time TC1 is written to a value, the pre-split register is cleared to zero.

TC1 is an 8Bit/16Bit upstream counter that works in 8-bit counting mode by default. The 8-bit counter mode has an auto-load function. By enabling RELOAD, TC1 1h to TC1L is automatically loaded after TC1 overflows. TC1 can work in 16Bit counter mode by enabling TC1HEN without auto-loading. The TC1 timer can only work if TC1EN is enabled. The clock source is the internal clock Fc (optional Fm/Fs via TIMERSC).

When each clock cycle comes, the counter is increased by 1.TC1 count overflows to form an interrupt signal, and the system jumps to the corresponding interrupt vector address.

In IDLE mode, TC1 interrupt can wake up the circuit. After wake up, you can choose to interrupt or continue to execute the original program. For the method, refer to the port state change to wake up.

3.3.2.1 TC1 8Bit Timing Settings

1. Assign an initial value to the TC1L register;
2. If automatic loading is enabled, TC1H register needs to be set, and TC1H value will be automatically loaded after TC1 counter overflow;
3. Set the TC1CON register, enable automatic loading on demand, and configure the pre-division ratio;
4. Enable TC1EN and open the TC1 timer to count;
5. Enable TC1IE of RD6/IMR1 register to enable interrupt and execute EI instruction;
6. The interrupt program will automatically save ACC, STATUS and RSR, and clear the TC1 interrupt flag bit after the execution of RETI instruction;

3.3.2.2 TC1 16Bit Timing Settings

1. Assign initial values to the TC1L and TC1H registers;
2. Set the value of TC1CON register, enable TC1HEN and set the pre-division ratio;
3. Enable TC1IE, open the TC1 timer count;
4. Enable TC1IE of RD6/IMR1 register to open interrupt and execute EI instruction;
5. The interrupt program will automatically save ACC, STATUS and RSR, and clear the TC1 interrupt flag bit after executing RETI instruction;

3.3.2.3 TC1 Timing Calculation Description

The TC1 timing function assigns an initial value to the timer by writing the value to the TC1L and TC1H registers. The timer accumulates from the initial value position until the timer overflows and generates an interrupt.

TC1 timing time calculation formula (select 8Bit counter mode) :

TC1 timing time = (1/Fc)*(TC1 frequency division)*(256-TC1L initial value)

For example:

Fc=Fm(TIMERSC=1)=8 MHz, TC1 frequency division selection =8 frequency division, TC1L initial value =156;

TC1 timing time = (1/8)*(8)*(256-156)=100us

TC1 timing time calculation formula (select 16Bit counter mode) :

TC1 timing time = (1/Fc)* (TC1 frequency division)*[65536-(TC1H+TC1L initial value)]

For example:

Fc=Fm(TIMERSC=1)=1 MHz, TC1 frequency division selection =4 frequency division, TC1 initial value =5536(TC1H=0X15+TC1L=0XA0);

TC1 timing time = (1/1)*(4)*(65536-5536)=60ms

3.3.2.4 TC1 Wake Up in Idle Mode

TC1 can wake up idle mode and enable RDE/WECR register TMRWE to turn on wake up function. Set the Bit4 TIMERSC of the R88/CPUCON register to 0 and select the TC1 clock source as the secondary clock. The TC1IE, IDLE = 1+ SLEEP command was enabled. The system entered the idle mode and the TC1 timer worked normally. When the TC1 timer overflows, the system wakes up and enters the low-speed mode. If EI is enabled, it will wake up and enter the interrupt. If DI is executed, it will wake up and execute the next instruction.

3.4 LVD Function Module

The JZ8F8003 features Low Voltage detection (LVD) with a total of four programmable voltage values.When the operating voltage of the CPU drops below the set value, the Bit5 of the R83/STATUS register is set to 0;When the CPU operating voltage increases from below the set value to above the set value, the Bit5 of the R83/STATUS register is changed to 1.

LVD voltage detection:

LVD<1>	LVD<0>	Voltage selection
0	0	4.5v
0	1	4.0v
1	0	3.3v
1	1	2.2v

3.4.1 LVD Voltage Detection Settings

1. Set LVD voltage value (LVD<1:0> bit of RAE/LVDCON register);
2. Enable LVD function (LVDEN bit of RAE/LVDCON register);
3. Determine the Bit5 bit of the R83/STATUS register, if it is lower than the set value is 0, if it is higher than the set value or if it is not enabled to be 1;

3.5 ADC Function Module

JZ8F8003 ADC module consists of three 18-channel analog channel selection registers, three controllers (RA6/ADIGS, RA7/ADOC, RA8/ADCON), and three data registers (RA3/ADDATA, RA4/ADDATA1H, RA5/ Addata 1L) and a 12-bit precision AD converter. The following shows the AD conversion function diagram.

ADC module adopts the successive approximation to convert the analog signal into digital value, and the result is stored in the ADDATA, AdData 1H, AdData 1L result register. Through the ADC control register, channel selection, trigger source selection, internal and external reference voltage source, sampling clock, ADC start and ADC power consumption are set.

After the AD conversion is complete, you can enter the interrupt, or you can query the ADRUN bit of RA8/ADCON to determine.

If the AD wake up function is enabled, you can wake up the AD conversion from sleep mode or idle mode.

AD sampling time calculation method:

From setting ADRUN=1, time to complete an AD sampling =**ADC sampling hold period +AD conversion time**

AD conversion time:

It takes a TAD (TAD) to convert a bit from the AD. The chip has a built-in AD of 12 bits, so the conversion time is 12 TAD (TAD).

Calculation method of AD sampling voltage value:

ADC sampling voltage = sampling value /4096* reference voltage

For example, the reference voltage is internal reference 2v and the sampling value is 0x400=1024

ADC sampling voltage =1024/4096*2=0.5v

3.5.1 ADC Register

0xA0(P5ADE): P5 AD input port selection control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
ADE5<7>	ADE5<6>	ADE5<5>	ADE5<4>	ADE5<3>	ADE5<2>	ADE5<1>	ADE5<0>

P5 ADC input selection control bit:

0: The port is set to GPIO

1: The port is set as an analog input port

0xA1(P6ADE): P6 AD input port selection control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
ADE6<7>	ADE6<6>	ADE6<5>	ADE6<4>	ADE6<3>	ADE6<2>	ADE6<1>	ADE6<0>

P6 port ADC input selection control bit:

0: The port is set to GPIO

1: The port is set as an analog input port

0xA2(P7ADE): P7 AD input port selection control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	-	-	ADE7<1>	ADE7<0>

P7 port ADC input selection control bit:

0: The port is set to GPIO

1: The port is set as an analog input port

0xA3(ADDATA): high 8-bit register of ADC conversion result

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
AD<11>	AD<10>	AD<9>	AD<8>	AD<7>	AD<7>	AD<5>	AD<4>

read-only

0xA4(ADDATA1H): ADC conversion result high 4 bit register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
-	-	-	-	AD<11>	AD<10>	AD<9>	AD<8>

read-only

0xA5(ADDATA1L): Low 8-bit register of ADC conversion result

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
AD<7>	AD<6>	AD<5>	AD<4>	AD<3>	AD<2>	AD<1>	AD<0>

read-only

0xA6(ADIGS): ADC input and trigger source control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TRIGS<2>	TRIGS<1>	TRIGS<0>	ADIS<4>	ADIS<3>	ADIS<2>	ADIS<1>	ADIS<0>

Bit<7:5>:TRIGS<2: 0>-trigger source selection bit (enables ADTRS to work)

TRIGS2	TRIGS1	TRIGS0	Trigger source selection
0	0	0	PWM0 Duty cycle
0	0	1	PWM0 period
0	1	0	PWM1 Duty cycle
0	1	1	PWM1 period
1	0	0	PWM2 Duty cycle
1	0	1	PWM2 period
1	1	0	PWM3 Duty cycle
1	1	1	PWM3 period

Bit<4:0>:ADIS<4:0>-ADC analog input channel selection

ADIS4	ADIS3	ADIS2	ADIS1	ADIS0	Analog input
0	0	0	0	0	ADIN0/P50
0	0	0	0	1	ADIN1/P51
0	0	0	1	0	ADIN2/P52

0	0	0	1	1	ADIN3/P53
0	0	1	0	0	ADIN4/P54
0	0	1	0	1	ADIN5/P55
0	0	1	1	0	ADIN6/P56
0	0	1	1	1	ADIN7/P57
0	1	0	0	0	ADIN8/P60
0	1	0	0	1	ADIN9/P61
0	1	0	1	0	ADIN10/P62
0	1	0	1	1	ADIN11/P63
0	1	1	0	0	ADIN12/P64
0	1	1	0	1	ADIN13/P65
0	1	1	1	0	ADIN14/P66
0	1	1	1	1	ADIN15/P67
1	0	0	0	0	ADIN16/P70
1	0	0	0	1	ADIN17/P71
1	0	0	1	0	ADIN18/1/4vdd
1	0	0	1	1	ADIN19/AMP0
1	0	1	0	0	ADIN20/AMP1

0xA7(ADOC): ADC voltage and compensation calibration control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
VREFS	VREF<1>	VREF<0>	CALI	SIGN	VOF<2>	VOF<1>	VOF<0>

Bit<7> : VREFS-ADC reference voltage source selection

0: internal reference voltage, VDD as ADC reference voltage, P54 as GPIO

1: External reference voltage, P54 pin voltage as ADC reference voltage

Bit<6:5> : VREF<1:0> -ADC internal reference voltage selection

VREF1	VREF0	Internal reference voltage
0	0	VDD
0	1	4V
1	0	3V
1	1	2V

Bit<4> : CALI-ADc-Compensatory calibration enable bit

0: Disable

1: indicates that the function is enabled

Bit<3> : SIGN-ADC- compensates the voltage polarity selection bit

0: indicates the negative voltage

1: positive voltage

Bit<2:0> : VOF<2:0>- Compensatory voltage selection

VOF2	VOF1	VOF0	Range of compensation
0	0	0	0 LSB
0	0	1	2LSB
0	1	0	4 LSB
0	1	1	6LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

0xA8(ADCON): ADC control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
ADEN	ADRUN	-	ADTRS	ADSH<1>	ADSH<0>	ADCKR<1>	ADCKR<0>

Bit<7>:ADPD-ADC power enable bit

0: Disable

1: Enable

Bit<6>:ADRUN-ADC start up control bit

0: ADC conversion ends, and the system automatically sets the bit, which cannot be reset by software

1: ADC conversion begins. This bit can be set by software

Bit<5>:not used

Bit<4>:ADTRS-ADC triggers source selection bits

0: The startup is enabled by the ADRUN software

1: is started by PWM duty ratio, period overflow, or ADRUN software

Bit<3:2>:ADSH<1:0> -ADC sampling and hold time selection (at least 4us is recommended, TAD:ADC running clock period)

ADSH1	ADSH0	TAD
0	0	2 * TAD
0	1	4 * TAD
1	0	8 * TAD
1	1	12 * TAD

Bit<1:0>:ADCKR<1:0> -ADC clock predivision selection

ADCKR1	ADCKR0	ADC clock division ratio
0	0	2 * TAD
0	1	4 * TAD
1	0	8 * TAD
1	1	12 * TAD

3.5.2 ADC analog-to-digital conversion Settings

1. Enable ADC input port and select analog channel, set P5/6/7ADE and ADIGS registers;

2. Select ADC reference voltage source and reference voltage, and set ADOC register;

3. ADC clock source Fc can be Fm/Fs, clock pre-division is selected, CPUCON and ADCON registers are set;

4. Select ADC trigger source, trigger start with PWM cycle and duty cycle, set ADCON and ADIGS registers

5. If interrupt function is needed, set ADIE=1 and execute "EI" instruction;

6. Set "ADPD=1" to start the AD supply voltage;

7. Call AD accuracy correction subroutine;

8. Select IDLE/SLEEP mode and set AD wake up function, ADWE=1;

9. Set "ADRUN=1" to start AD conversion or PWM to trigger AD conversion;

10. Wait for interruption or ADRUN to be cleared to 0. If AD interruption occurs, ADIF shall be cleared to 0 when leaving the interrupt program;

11. Save the result of the conversion.If multiple AD conversions are required, skip to Step 9.

3.5.3 ADC analog-to-digital conversion Settings

1. Enable ADC compensation calibration CALI based on steps 1 to 5 in 3.5.1 ADC Analog-to-Digital Conversion Setting Description;

2. Set ADC compensation voltage polarity SIGN, first correct ADC positive voltage, then correct ADC negative voltage, and correct each time 2LSB compensation range;

3. Cyclic detection of AD value. If the result is "0", AD accuracy correction is finished and the "CALI" position of ADC is set to 0;

3.6 PWM Function Module

The JZ8F8003 has four built-in 8Bit PWM channels, which can be mapped to complementary output ports, and can be cascades into two 16Bit PWM channels. The PWM module has four built-in 8Bit pre-dividers, which can be configured through the PWM0/1/2/3 control register. The PWM clock source is the Fc clock, which can be used to double the frequency through the R88/CPUCON register DB_EN.

PWM has a period overflow interrupt and a duty cycle matching interrupt. After being enabled, you can jump to the interrupt subroutine.

In IDLE mode, enable TMRWE + PWM0IE, PWM1IE, PWM2IE, PWM3IE, DT0IE, DT1IE, DT2IE, and DT3IE to wake up the system.

3.6.1 PWM Register

0xB0(PWM0CON): T0/PWM0 control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T0EN	IPWM0A	PWM0A	IPWM0E	PWM0E	PST0<2>	PST0<1>	PST0<0>

Bit<7> : T0EN-PWM0 Indicates the timer enable bit
0: Disable
1: Enable
Bit<6> : IPWM0A-IPWM0 The output is inverted
0: IPWM0 duty cycle is low
1: IPWM0 duty cycle is high
Bit<5> : PWM0A-PWM0 The output is inverted
0: PWM0 duty cycle is high
1: PWM0 duty cycle is low
Bit<4> : IPWM0E-IPWM0 Indicates the output enable bit
0: IPWM0 is disable
1: IPWM0 is enabled
Bit<3> : PWM0E-PWM0 Indicates the output enable bit
0: PWM0 Disable
1: PWM0 enabled
Bit<2:0> : PST0<2:0> -T0 Select the clock divider

PST2	PST1	PST0	T0 frequency division ratio
0	0	0	1:1(default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128

1	1	1	1:256

0xB1(PWM0RD): PWM0 period register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PRD0<7>	PRD0<6>	PRD0<5>	PRD0<4>	PRD0<3>	PRD0<2>	PRD0<1>	PRD0<0>

The time period (time basis) of PWM0. The frequency of PWM0 is the reciprocal of its period

0xB2(PWM0DT): PWM0 duty cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT0<7>	DT0<6>	DT0<5>	DT0<4>	DT0<3>	DT0<2>	DT0<1>	DT0<0>

Causes the output of PWM0 to remain high until its value matches a specific value of T0 content.

0xB4(PWM1CON): T1/PWM1 control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T1EN	IPWM1A	PWM1A	IPWM1E	PWM1E	PST1<2>	PST1<1>	PST1<0>

Bit<7> : T1EN-PWM1 timer enable bit
0: Disable
1: Enable
Bit<6> : IPWM1A-IPWM1 The output is inverted
0: IPWM1 duty cycle is low
1: IPWM1 duty cycle is high
Bit<5> : PWM1A-PWM1 The output is inverted
0: PWM1 duty cycle is high
1: PWM1 duty cycle is low
Bit<4> : IPWM1E-IPWM1 output enable bit
0: IPWM1 disabled
1: IPWM1 enabled
Bit<3> : PWM1E-PWM1 output enable bit
0: PWM1 Disabled
1: PWM1 enabled
Bit<2:0>:PST1<2:0> -T1 Select the clock divider

PST12	PST11	PST10	T1 frequency division ratio
0	0	0	1:1(default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128

1	1	1	1:256

0xB5(PWM1RD): PWM1 cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PRD1<7>	PRD1<6>	PRD1<5>	PRD1<4>	PRD1<3>	PRD1<2>	PRD1<1>	PRD1<0>

The time period of PWM1 (time basis), the frequency of PWM1 is the reciprocal of its period

0xB6(PWM1DT): PWM1 duty cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT1<7>	DT1<6>	DT1<5>	DT1<4>	DT1<3>	DT1<2>	DT1<1>	DT1<0>

Keeps the output of PWM1 high until its value matches a specific value of T1 content.

0xB8(PWM2CON): T2/PWM2 control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T2EN	IPWM2A	PWM2A	IPWM2E	PWM2E	PST2<2>	PST2<1>	PST2<0>

Bit<7> : T2EN-PWM2 timer enable bit
0: Disable
1: Enable
Bit<6> : IPWM2A-IPWM2 The output is inverted
0: IPWM2 duty cycle is low
1: IPWM2 duty cycle is high
Bit<5> : PWM2A-PWM2 The output is inverted
0: PWM2 duty cycle is high
1: PWM2 duty cycle is low
Bit<4> : IPWM2E-IPWM2 output enable bit
0: Disable
1: Enable
Bit<3> : PWM2E-PWM2 output enable bit
0: Disable
1: Enable
Bit<2:0> : PST2<2:0> -T2 Select the clock divider

PST22	PST21	PST20	T2 frequency division ratio
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

0xB9(PWM2RD): PWM2 period register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PRD2<7>	PRD2<6>	PRD2<5>	PRD2<4>	PRD2<3>	PRD2<2>	PRD2<1>	PRD2<0>

The time period of PWM2 (time basis), the frequency of PWM2 is the reciprocal of its period

0xBA(PWM2DT): PWM2 duty cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT2<7>	DT2<6>	DT2<5>	DT2<4>	DT2<3>	DT2<2>	DT2<1>	DT2<0>

Keeps the output of PWM2 high until its value matches a specific value of the contents of T2.

0xBC(PWM3CON): T3/PWM3 control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
T3EN	IPWM3A	PWM3A	IPWM3E	PWM3E	PST3<2>	PST3<1>	PST3<0>

Bit<7> : T3EN-PWM3 timer enable bit
0: Disable
1: Enable
Bit<6> : IPWM3A-IPWM3 The output is inverted
0: IPWM3 duty cycle is low
1: IPWM3 duty cycle is high
Bit<5> : PWM3A-PWM3 The output is inverted
0: PWM3 duty cycle is high
1: PWM3 duty cycle is low
Bit<4> : IPWM3E-IPWM3 output enable bit
0: Disable
1: Enable
Bit<3> : PWM3E-PWM3 output enable bit
0: Disable
1: Enable
Bit<2:0> : PST3<2:0> -T3 Clock divider selection

PST32	PST31	PST30	T3 frequency division ratio
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

0xBD(PWM3RD): PWM3 cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PRD3<7>	PRD3<6>	PRD3<5>	PRD3<4>	PRD3<3>	PRD3<2>	PRD3<1>	PRD3<0>

The time period (time basis) of PWM3. The frequency of PWM3 is the reciprocal of its period

0xBE(PWM3DT): PWM3 duty cycle register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT3<7>	DT3<6>	DT3<5>	DT3<4>	DT3<3>	DT3<2>	DT3<1>	DT3<0>

Keeps the output of PWM3 high until its value matches a specific value for the contents of T3.

0xC9(PWMCS): PWM cascade and dead zone control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
PWMCAS1	PWMCAS0	DEADT3E	DEADT2E	DEADT1E	DEADT0E	PSTD<1>	PSTD<0>

Bit<7> : PWMCAS1-PWM3 and PWM2 cascading mode is enabled
0: Disable, two independent 8-bit PWM
1: Enable, 16-bit PWM mode (cascaded by two 8-bit PWM)
Bit<6> : PWMCAS0-PWM1, PWM0 Cascading mode is enabled
0: Disable, two independent 8-bit PWM
1: Enable, 16-bit PWM mode (cascaded by two 8-bit PWM)
Bit<5> : DEADT3E-PWM3 Deadzone adjustment Enable control bit
0: Disable
1: Enable
Bit<4> : DEADT2E-PWM2 deadzone adjustment Enable control bit
0: Disable
1: Enable
Bit<3> : DEADT1E-PWM1 Deadzone adjustment Enables the control bit
0: Disable
1: Enable
Bit<2> : DEADT0E-PWM0 Deadzone adjustment Enable control bit
0: Disable
1: Enable
Bit<1:0>:PSTD<1:0> -Select a dead zone clock divider

PSTD1	PSTD0	Frequency division ratio
0	0	1:1 (default)
0	1	1:2
1	0	1:4
1	1	1:8

0xCA(PWMDEADT): PWM deadzone time control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DEADT<7>	DEADT<6>	DEADT<5>	DEADT<4>	DEADT<3>	DEADT<2>	DEADT<1>	DEADT<0>

Dead zone time setting, clock source with PWM (Fc)

0xCB(PWMIS1): PWM port mapping control register 1

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
IPWM1S<1>	IPWM1S<0>	PWM1S<1>	PWM1S<0>	IPWM0S<1>	IPWM0S<0>	PWM0S<1>	PWM0S<0>

Bit<7:6> : IPWM1S<7:6> -IPWM1 Indicates the port mapping selection

IPWM1S1	IPWM1S0	Mapping Port
0	0	P67 (default)
0	1	P65
1	0	none
1	1	none

Bit<5:4> : PWM1S <5:4> -PWM1 Indicates the port mapping selection

PWM1S1	PWM1S0	Mapping Port
0	0	P64 (default)
0	1	P63
1	0	P52
1	1	none

Bit<3:2> : IPWM0S <3:2> -IPWM0 Indicates the port mapping selection

IPWM0S1	IPWM0S0	Mapping Port
0	0	P66 (default)
0	1	P61
1	0	P55
1	1	P53

Bit<1:0> : PWM0S <1:0> -PWM0 Indicates the port mapping selection

PWM0S1	PWM0S0	Mapping Port
0	0	P63 (default)
0	1	P65
1	0	P60
1	1	none

0xCC(PWMIS2): PWM port mapping control register 2

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
IPWM3S<1>	IPWM3S<0>	PWM3S<1>	PWM3S<0>	IPWM2S<1>	IPWM2S<0>	PWM2S<1>	PWM2S<0>

Bit<7:6>:IPWM3S<7:6> -IPWM3 Indicates the port mapping selection

IPWM3S1	IPWM3S0	Mapping Port
0	0	P50(default)
0	1	none

1	0	none
1	1	none

Bit<5:4>:PWM1S <5:4> - PWM1 Indicates the port mapping selection

PWM3S1	PWM3S0	Mapping Port
0	0	P56(default)
0	1	P67
1	0	none
1	1	none

Bit<3:2>:IPWM0S <3:2> - IPWM0 Indicates the port mapping selection

IPWM2S1	IPWM2S0	Mapping Port
0	0	P71(default)
0	1	P60
1	0	none
1	1	none

Bit<1:0>:PWM0S <1:0> - PWM2 Indicates the port mapping selection

PWM2S1	PWM2S0	Mapping Port
0	0	P65(default)
0	1	P66
1	0	P56
1	1	none

3.6.2 PWM Period and Duty Cycle

PWM0, PWM1, PWM2 and PWM3 each provide a clock counter with 8bit programmable pre-division as the baudrate clock generator of PWM module. The counter function can be enabled by enabling TxEN in the PWM control register. With the PSTx<2:0> control bit, the pre-division of the counter can be set. PWMxA and IPWMxA control outputs are reversed. PWMxE and IPWMxE enable the output function of I/O ports respectively.

The PWM cycle is written to the PWMxRD cycle register (PRD). When the counter value is equal to the PRD value, the following events occur in the next increment cycle:

- Counter clear to zero;
- The corresponding PWM output pin is set to high level (IPWM pin is set to low level);
- Generates PWM cycle overflow interrupt (if enabled).
- The PWM duty cycle is latched from the PWMxDT register to the DT/TIMER comparison register.

Calculation formula of PWM cycle:

PWM period = (PRD) * (1/Fc) * (PWM frequency division)

For example:

PWMxRD=100, Fc=Fm(TIMERSC=1)=8 MHz, PWM frequency division selection =2 frequency division;

PWM period = (100) * (1/8) * (2) =25us

The PWM duty cycle is written to the PWM duty cycle register. When the counter value overflows to clear, the PWMxDT value is locked to the DT/TIMER comparison register. When the value of the DT/TIMER comparison register equals the value of the TIMER counter, the PWM output pin is set to low. The value of PWMxDT can be written at any time, but the value of the DT/TIMER comparison register is written only when the period overflows:

Formula for calculating PWM duty ratio:

PWM duty cycle = (DT) * (1/Fc) * (PWM frequency division)

For example:

PWMxDT=50, Fc=Fm(TIMERSC=1)=8 MHz, PWM frequency division selection =2 frequency division;

PWM duty cycle = (50) * (1/8) * (2) =12.5us

3.6.3 Cascade 16-Bit PWM

The PWM cascade mode combines two 8Bit PWM functions into one 16Bit PWM. PWM0, PWM1, PWM2, and PWM3 can be combined into two 16Bit PWM pairs. In this mode, the necessary parameters are redefined as shown in the following table:

16 Bit PWM1	DT (Duty cycle)	PRD (period)	TIME (timer)
High 8 bits	DT1	PRD1	TMR1
Lower 8 bits	DT0	PRD0	TMR0

16 Bit PWM2	DT (Duty cycle)	PRD (period)	TIME (timer)
High 8 bits	DT3	PRD3	TMR3
Lower 8 bits	DT2	PRD2	TMR2

The frequency division ratio of 16-bit PWM1 uses the frequency division ratio of TMR0, the interrupt overflow bits are PWM0IE and DT0IE, and the output pins reuse PWM0 and IPWM0. The frequency division ratio of 16-bit PWM2 uses the frequency division ratio of TMR2, the interrupt overflow bit is PWM2IE and DT2IE, and the output pin multiplexes PWM2 and IPWM2.

3.6.4 PWM Deadzone Control Description

PWM0, PWM1, PWM2, and PWM3 have deadzone control function. By configuring the bit<0:1> of the deadzone control register RC9/PWMCS, configuring the frequency division option of the deadzone clock, and setting the appropriate deadzone clock. Enable dead zone functions of PWM0, PWM1, PWM2, and PWM3 using DEADT0E, DEADT1E, DEADT2E, and DEADT3E. IPWMxA inverts the IPWMx output and PWMxA inverts the PWMx output. RCA/PWMDEADT is the deadzone register and assigns a value to the deadzone register. When the deadzone counter counts to the given value, the PWM high and low level conversion operation is executed, which is the actual deadzone time.

3.6.5 Wake Up in Idle Mode of PWM

In idle mode, the program stops execution, the module with the wake-up function and the low speed oscillator work properly, and other functions are disabled.

PWM can wake up idle mode, set TMRWE wake up enable, select Fc clock source as Fs. Set the corresponding period or duty cycle interrupt enable, IDLE = 1+ SLEEP command system enters idle mode, PWM timer works normally.

When the corresponding interrupt condition is met, the system wakes up and enters either low or high mode (depending on the system mode before entering idle mode). If EI is enabled, it will wake up and enter the interrupt; if DI is enabled, it will wake up and execute the next instruction.

3.6.6 PWM Setting Description

1. Set the Fc clock source (R88/CPUCON: TIMERSC) as required, select the corresponding pre-division frequency ratio, complementary output port, port inverse, enable the corresponding interrupt type, etc.
2. Write the value of PWM cycle register;
3. Write the value of PWM duty ratio register;
4. Enable the corresponding timer (TxEN);
5. After the interrupt is triggered, if "EI" is enabled, the chip jumps to the address of the interrupt vector; if "DI" instruction is enabled, the next instruction is executed;

3.7 CMP/OP Function Module

The JZ8F8003 has 2 sets of operational amplifiers/comparators. If a feedback resistor is connected between the input and output, the comparator can be used as an operational amplifier. The function of an operational amplifier is suitable for the amplification of small signals. The result change of the comparator can trigger an interrupt (enable CMP0IE/CMP1IE), and enable CMP0WE/CMP1WE to wake the sleep/idle mode.

3.7.1 CMP/OP Register

0xAD(CMPCON): Comparator and OP amp control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
CMP<1>	CMP<0>	CIN1S	CIN0S	COS1<1>	COS1<0>	COS0<1>	COS0<0>

Bit<7>:CMP1-Output bit of comparator 1

Note: Read CMP1 before enabling CMP1IE or CMP1WE.

Bit<6>:CMP0-comparator 0 output bit

Note: Read CMP0 before enabling CMP0IE or CMP0WE.

Bit<5>:CIN1S-Comparator 1 or opamp 1CIN- Input selection

0:CIN1-Select P54 port

1:CIN1-Select the internal VREF reference voltage

Bit<4>:CIN0S-comparator 0 or opamp 0CIN- Input selection

0:CIN1-Select P71 port

1:CIN1-Select the internal VREF reference voltage

Bit<3:2>:COS1<1:0> -CMP/OP1 function selection bit

COS11	COS10	Function Description
0	0	Comparator 1 and op amp 1 are not used, and P53, P54 and P56 are used as normal IO pins
0	1	P53 and P54 serve as comparator 1 input pins, and P56 serves as ordinary IO pins
1	0	P53 and P54 serve as input pins for comparator 1, and P56 serves as output pins for comparator 1
1	1	P53 and P54 are input pins of op amp 1, and P56 is output pins of op amp 1

Bit<1:0>:COS0<1:0> -CMP/OP0 function selection bit

COS01	COS00	Function Description
0	0	Comparator 0 and op amp 0 are not used, P70, P71 and P55 are used as normal IO pins
0	1	P70 and P71 serve as comparator 0 input pins, and P55 serves as normal IO pins
1	0	P70 and P71 serve as input pins for comparator 0, and P55 serves as output pins for comparator 0
1	1	P70 and P71 are input pins of op amp 0, and P55 is output pins of op amp 0

3.7.2 CMP Setting Instructions

1. Set CIN+ and CIN- ports as input ports;

2, set RAD/ADCMP register CIN0S/CIN1S select input source for IO or internal reference voltage;

2, set RAD/ADCMP register COS0<1:0>/COS1<1:0> select CMP or OP function;

3. CMP0IE/CMP1IE interrupt can be enabled according to requirements, and the "EI" instruction can be executed. When the output result of the comparator changes, the interrupt will be triggered;

4. CMP0WE/CMP1WE can also be enabled to wake up sleep mode and idle mode according to needs;

Note:

1. The comparator wake up and interrupt are enabled. If the comparator output state changes, the program will first wake up from the SLEEP/idle mode, execute the interrupt program, and then run the next statement of "sleep";

2. The compensating voltage of the comparator is 10mV;

3.7.3 OP Setting Instructions

1. Set CIN+ and CIN- as input ports, and OPOUT0/ OPOUT1 as output ports;

2. set the RAD/ADCMP register COS0<1:0>/COS1<1:0>, used as an operational amplifier.

3.8 Interrupt Function Module

JZ8F8003 has 16 interrupt sources, no matter which one of them is used, the total interrupt must be enabled, that is, the "EI" instruction. The following are the characteristics, interrupt address, and interrupt priority of each interrupt:

中断源	中断标志	中断向量	优先级
TC0 溢出中断	TC0IF	003H	1
端口输入变化中断	ICIF	006H	2
INT0 外部中断	EX0IF	009H	3
INT1 外部中断	EX1IF	00CH	4
ADC 转换完成中断	ADIF	00FH	5
CMP0 中断	CMP0IF	012H	6
CMP1 中断	CMP1IF	015H	7
TC1 溢出中断	TC1IF	018H	8
PWM0 周期溢出中断	PWM0IF	01BH	9
PWM1 周期溢出中断	PWM1IF	01EH	10
PWM2 周期溢出中断	PWM2IF	021H	11
PWM3 周期溢出中断	PWM3IF	024H	12
PWM0 占空比溢出中断	DT0IF	027H	13
PWM1 占空比溢出中断	DT1IF	02AH	14
PWM2 占空比溢出中断	DT2IF	02DH	15
PWM3 占空比溢出中断	DT3IF	030H	16

RDA(ISR1)/RDB(ISR2) are interrupt status flag registers. They record the interrupt flag bits when an interrupt generates an interrupt request.

RD6(IMR1)/RD7(IMR2) sets registers for interrupt enablement. Interrupt permit and disable are set in these registers. Total interrupts are allowed by the "EI" instruction, and total interrupts are forbidden by the "DI" instruction. When an interrupt is generated, the execution of its next instruction is executed from the interrupt vector address. The corresponding interrupt flag bit must be cleared before leaving the interrupt service routine, so as to avoid the wrong action of interrupt.

3.8.1 Interrupt Register

0xD5(EINTR): External Interrupt control register

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
NRE1	INTEG1	EXPS1	EIS1	NRE0	INTEG0	EXPS0	EIS0

Bit<7> : NRE1-INT1 Indicates the noise suppression enable bit
0: Disable
1: Enable, in low frequency crystal oscillator (LXT) mode or low speed mode, noise suppression circuit is always disabled
Bit<6> : INTEG1-INT1 indicates edge selection
0: Interrupt occurs at the rising edge of INT1 pin signal
1: Interrupt occurs at INT1 pin signal drop edge
Bit<5> : EXPS1-INT1 signal pin selection (do not switch between the two pins after EIS1 is enabled)
0: Select P65 as the INT1 signal pin
1: Select P50 as the INT1 signal pin
Bit<4> : EIS1-INT1 pin selection
0: P65/P50 indicates GPIO
1: P65/P50 is the external interrupt pin
Bit<3> : NRE0-INT0 Indicates the noise suppression enable bit
0: Disable
1: Enable, in low frequency crystal oscillator (LXT) mode or low speed mode, noise suppression circuit is always disabled
Bit<2> : INTEG0-INT0 indicates the edge selection of the signal
0: Interrupt occurs at the rising edge of the INT0 pin signal
1: Interrupt occurs at the drop edge of INT0 pin signal
Bit<1> : EXPS0-INT0 pin selection (do not switch between the two pins after EIS0 is enabled)
0: Select P67 for INT0 signal pin
1: Select P51 for INT0 signal pin
Bit<0> : EIS0-INT0 pin selection
0: P67/P51 indicates GPIO
1: P67/P51 are external interrupt pins

0xD6(IMR1): Interrupt enable control register 1

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TC1IE	CMP1IE	CMP0IE	ADIE	EX1IE	EX0IE	ICIE	TC0IE

Bit<7>: TC1IE - TC1 interrupt enable bit
Bit<6>: CMP1IE - CMP1 interrupt enable bit
Bit<5>: CMP0IE - CMP0 interrupt enable bit
Bit<4>: ADIE - ADC interrupt enable bit
Bit<3>: EX1IE -int1 interrupt enable bit
Bit<2>: EX0IE -int0 interrupt enable bit
Bit<1>: ICIE - IC interrupt enable bit
Bit<0>: TC0IE - TC0 interrupt enable bit

0: Disable
1: Enable

0xD7(IMR2): Interrupts enable control register 2

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT3IE	DT2IE	DT1IE	DT0IE	PWM3IE	PWM2IE	PWM1IE	PWM0IE

Bit<7>: DT3IE -DT3 interrupt enable bit
Bit<6>: DT2IE - DT2 interrupt enable bit
Bit<5>: DT1IE - DT1 interrupt enable bit
Bit<4>: DT0IE - DT0 interrupt enable bit
Bit<3>: PWM3IE - PWM3 interrupt enable bit
Bit<2>: PWM2IE - PWM2 interrupt enable bit
Bit<1>: PWM1IE - PWM1 interrupt enable bit
Bit<0>: PWM0IE - PWM0 interrupt enable bit
0: Disable
1: Enable

0xDA(ISR1): Interrupt flag register 1

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
TC1IF	CMP1IF	CMP0IF	ADIF	EX1IF	EX0IF	ICIF	TC0IF

Bit<7>:TC1IF - TC1 interrupt flag
Bit<6>:CMP1IF - CMP 1interrupt flag, set when comparator 1 output changes
Bit<5>:CMP0IF - CMP0 interrupt flag, set when comparator 0 output changes
Bit<4>:ADIF - ADC interrupt flag
Bit<3>:EX1IF - INT1 interrupt flag
Bit<2>:EX0IF - INT0 interrupt flag
Bit<1>:ICIF - IC interrupt flag
Bit<0>:TC0IF - TC0 interrupt flag
0: No interrupt is triggered
1: Triggers an interrupt

0xDB(ISR2): Interrupt flag register 2

BIT<7>	BIT<6>	BIT<5>	BIT<4>	BIT<3>	BIT<2>	BIT<1>	BIT<0>
DT3IF	DT2IF	DT1IF	DT0IF	PWM3IF	PWM2IF	PWM1IF	PWM0IF

Bit<7>:DT3IF - DT3 interrupt flag
Bit<6>:DT2IF - DT2 interrupt flag
Bit<5>:DT1IF - DT1 interrupt flag
Bit<4>:DT0IF - DT0 interrupt flag
Bit<3>:PWM3IF - PWM3 interrupt flag
Bit<2>:PWM2IF - PWM2 interrupt flag
Bit<1>:PWM1IF - PWM1 interrupt flag
Bit<0>:PWM0IF - PWM0 interrupt flag
0: No interrupt is triggered
1: Triggers an interrupt

3.8.2 Interrupting On-site Protection

In the process of responding to interrupt, the hardware has its own interrupt protection function, which saves the contents of ACC, R3 and R4. When leaving the interrupt subroutine, the saved values will be reloaded into ACC, R3 and R4. In this way, the values of ACC, R3 and R4 will be changed by instructions when executing the interrupt subroutine. Causes an error to occur when returning to the main program. As shown below:

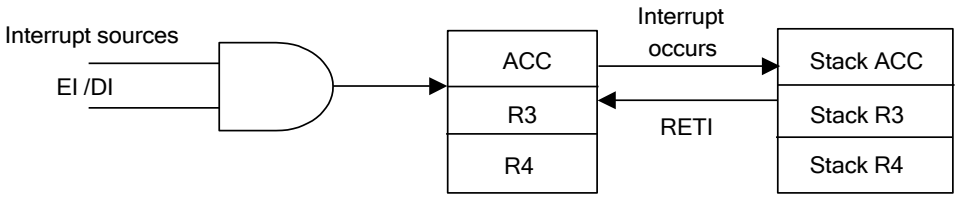


Diagram of interrupt site protection

3.9 Reset Function Module

3.9.1 Overview

The JZ8F8003 system provides four reset modes:

- The POR is powered on and reset
- RESET pin input low level reset
- WDT watchdog overflows reset
- LVR low voltage reset

When any of the above reset occurs, all system registers are initialized to the reset value, the program stops running, and the program counter PC clears to zero. After the reset is complete, the system restarts at 0000H vector.

Any reset situation requires a certain response time, and the system reset mechanism can ensure the reliable reset of MCU. Different types of oscillators, the time required to complete the reset is also different. Therefore, the rising speed of VDD and the starting time of different oscillators are not fixed. The RC oscillator has the shortest starting time, while the crystal oscillator has a longer starting time. When using the user terminal, pay attention to the requirements of application scenarios on the power-on and reset time.

3.9.2 Restarting the POR

Power-on reset is closely related to LVR operations. The power-on process of the system shows a gradual upward curve, and it takes a certain time for the system to reach the normal level.

- Power-on: The system detects that the power supply voltage increases and waits for it to stabilize
- External reset (only external reset pin enabled state) : The system detects the status of the external reset pin. If it is not high, the system remains reset until the external reset pin is released
- System initialization: All system registers are set to their initial values
- Oscillator starts working: The oscillator starts providing the system clock
- Program execution: After the power-on is complete, the program starts to run

Power-on reset setup time:

SUT	Reset setup time
1	18ms
0	4.5 ms

3.9.3 WDT Reset

Watchdog reset is a protection setting of the system. Under normal conditions, the watchdog timer is reset by the program. If an error occurs, the system is in an unknown state, the watchdog timer overflows, and the system resets. After the watchdog is reset, the system restarts and enters the normal state.

- Watchdog timer status: The system checks whether the watchdog timer overflows. If it overflows, the system resets.
- System initialization: All system registers are set to the initialization default values.
- Oscillator starts working: The oscillator starts providing the system clock;
- Execution program: After power-on, the program starts to run;

Instructions for wdt wake-up:

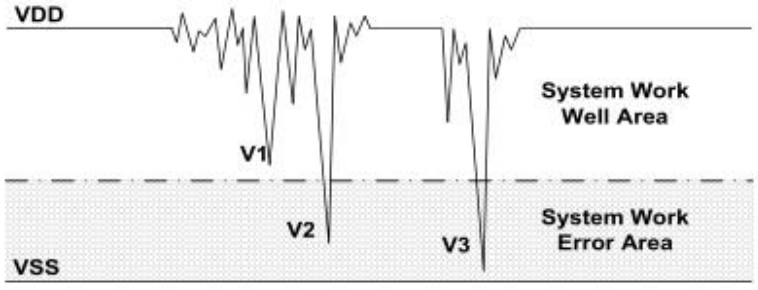
After the system is reset, the program starts to execute from address 0X00. The user can judge the time overflow bit of R83 (STATUS) register Bit4 at program address 0X83. If it is WDT overflow, it can be judged as watchdog reset and the corresponding wake up subroutine is executed. Note that watchdog awakening is essentially a special application of watchdog reset.

Note on application of watchdog timer:

- Checking the status of the I/O port and the contents of RAM before zeroing out the watchdog enhances program reliability;
- Do not zero out the watchdog during an interrupt, otherwise the main program will not be detected.
- The program should only have one watchdog action in the main program. This architecture can maximize the protection function of the watchdog.

3.9.4 LVR Low-voltage Reset

Power-off reset The system voltage drops due to external factors (such as interference or changes in external loads). Power-off may cause abnormal system operating status or program execution errors.



Brown Out Reset Diagram

Voltage drop may enter the system dead zone. The system dead zone means that the power supply cannot meet the minimum operating voltage requirements of the system. Above is a typical power failure reset diagram. In the figure, VDD is seriously disturbed and the voltage drop is very low. Above the dotted line, the system works normally. Below the dotted line, the system enters an unknown working state. This area is called the dead zone. When VDD drops to V1, the system is still in normal state. When the VDD drops to V2 or V3, the system enters the dead zone, which may cause errors. The system may enter the dead zone if:

DC in use:

DC generally uses battery power supply. When the battery voltage is too low or the MCU drives the load, the system voltage may drop and enter the dead zone. At this point, the power supply does not drop further to the LVR detection voltage, so the system remains in the dead zone.

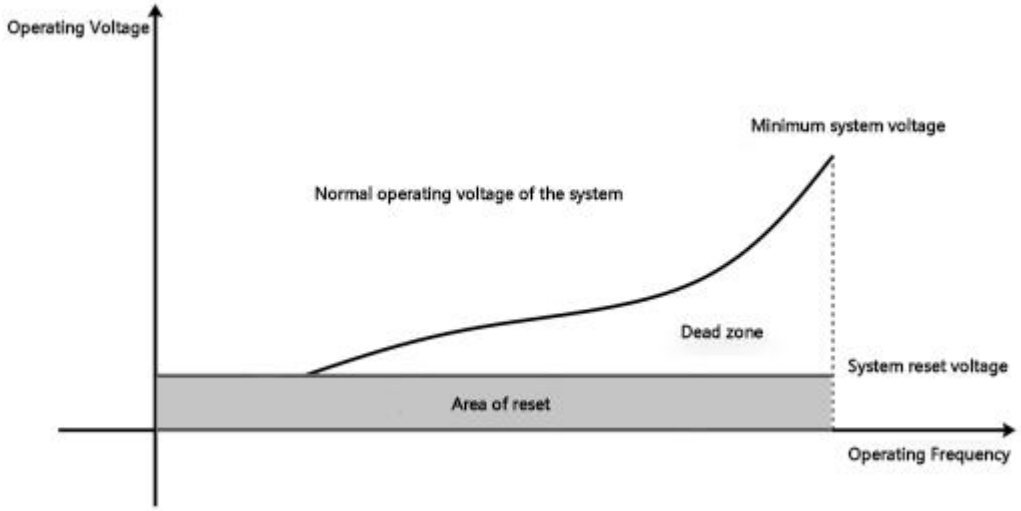
AC in use:

When the system uses AC power supply, the DC voltage is affected by the noise in the AC power supply. When external loads are too high, such as when driving a motor, interference from the load action also affects the DC power supply. If the VDD falls below the minimum working voltage due to interference, the system may enter an unstable working state. When the AC is used, the system takes a long time to power on and off. The power-on time sequence protection enables the system to power on normally, but the power-off process is similar to that in DC operation. After AC power is turned off, the VDD voltage is easy to enter the dead zone in the process of slow decline.

3.9.5 Operating frequency and LVR Low voltage reset

In order to improve the reset performance of the system after power failure, the minimum operating voltage of the system must be defined first. The minimum operating

voltage of the system is related to the execution speed of the system, and the minimum operating voltage value is different under different execution speeds.



As shown in the figure above, the normal operating voltage area of the system is generally higher than the system reset voltage, and the reset voltage is determined by the low voltage detection (LVR) level. When the system execution speed increases, the minimum operating voltage of the system also increases correspondingly. However, since the reset voltage of the system is fixed, there will be a voltage region between the minimum operating voltage of the system and the reset voltage of the system. The system cannot work normally and will not be reset.

To avoid voltage dead zone occurs, to select the appropriate reset voltage LVR point (Fcpu = oscillator frequency / clocks dividing; e.g. IRC frequency = 4M, clocks divider = 2 Clocks, then Fcpu = 2M;).

Fcpu	LVR
Fcpu<=2M	No less than 1.8V
2M<Fcpu<=4M	No less than 2.7V
4M<Fcpu<=6M	No less than 3.5V
Fcpu>6M	Must 4.0V

Note: The corresponding value of the operating frequency and LVR reset voltage point is only the recommended value. Users can adjust the reset voltage point appropriately according to the specific application in the process of use.

3.10 System Clock Function Module

The JZ8F8003 is integrated with 7 kinds of oscillators, which can be configured with OPTION. See the table below for details:

Type of oscillator	instructions
IRC (built-in RC oscillator)	The RCM can be used to select 1M, 4M, 8M or 16M
ERC (external RC oscillator)	P55: ERCIN
LXT1 (Low speed crystal oscillator)	100K to 1M
HXT1 (High speed crystal oscillator)	12M to 16M
LXT2 (Low speed crystal oscillator)	32.768 KHz
HXT2 (High speed crystal oscillator)	6M to 12M
XT (Crystal oscillator)	1M to 6M

3.10.1 Internal RC oscillator

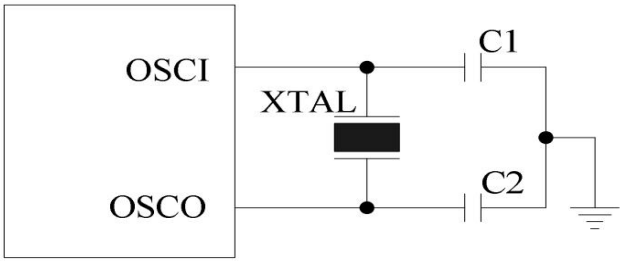
The JZ8F8003 provides internal RC mode with a frequency of 4MHz by default.

The internal RC oscillation mode contains four frequency values of 1M/4M/8M/16MHz. IRC operating frequency can be selected by setting the configuration bit of OPTION. The following is their corresponding relationship:

Clocks	Clocks frequency division
2clock	2clock
4clock	4clock
8clock	8clock
16clock	16clock

3.10.2 External crystal/ceramic oscillator

In most applications, pin OSCO and OSCI can be connected to crystal or ceramic resonators to generate oscillations. The circuit diagram below applies to both HXT and LXT modes. The recommended values for C1 and C2 are shown in the table. Due to the different characteristics of each resonator, users should refer to its specifications to select the appropriate values of C1 and C2.



Crystal oscillator application circuit

Crystal oscillator or ceramic oscillator capacitance selection reference:

Mode of oscillator	Mode of frequency	frequency	C1(pF)	C2(pF)
Ceramic oscillator	LXT1 (100K～1M)	100 KHz	60	60
		200 KHz	60	60
		455 KHz	40	40
		1 MHz	30	30
	XT (1M～6M)	1 MHz	30	30
		2 MHz	30	30
		4 MHz	20	20
Crystal oscillator	LXT2 (32.768K)	32.768 KHz	40	40
	LXT1 (100K～1M)	100 KHz	60	60
		200 KHz	60	60
		455 KHz	40	40
		1 MHz	30	30
	XT (1M～6M)	1 MHz	30	30
		2 MHz	30	30
		4 MHz	20	20
		6 MHz	30	30
	HXT2 (6M～12M)	6 MHz	30	30
		8 MHz	20	20
		12 MHz	30	30
	HXT1 (12M～16M)	12 MHz	30	30
		16 MHz	20	20

Note: The above data is for reference only, all subject to the actual test

3.11 Working Mode

The JZ8F8003 can operate at different clock frequencies in four operating modes that control the operation of the oscillator, the execution of the program, and the functional loss of the analog circuit.

- High speed: Select the internal high speed clock, but the low speed clock works properly
- Low speed: Select the internal low speed clock for the system clock, and stop the high speed clock
- Idle mode: low speed clock to work properly, other parts of the system into sleep (TC0, TC1 and PWM clock can continue to work and can arouse system), but by TMRWE ICWE, EXOWE, EX1WE, ADWE, CMPOWE, CMP1WE, WDTWE awake
- Sleep mode: All functions stop working, the system enters sleep, can be via TC0 (P67 input), ICWE, EXOWE, ADWE EX1WE, CMPOWE CMP1WE, WDTWE awake

Function module	High speed mode	Low speed mode	Idle mode	Sleep mode
IHRC	run	stop	stop	stop
ILRC	run	run	run	stop
CPU instruction	perform	perform	stop	stop
TC0	To work	To work	To work	Working (P67 input counting clock)
TC1	To work	To work	To work	stop
PWM	To work	To work	To work	stop
Internal interruption	All valid	All valid	All valid	TC0IE, ICIE, ADIE, CMP0IE, CMP1IE,
External interruption	effective	effective	effective	effective
Wake up function	-	-	TMRWE, ICWE, EXOWE, EX1WE, ADWE, CMPOWE, CMP1WE, WDTWE	TMRWE(only TC0 external inputs work), ICWE, EXOWE, EX1WE, ADWE, CMPOWE, CMP1WE, WDTWE
WDT timer	WDT option control	WDT option control	WDT option control	WDT option control

3.11.1 High-speed Mode

The high speed mode is the system high speed clock working mode, the system clock source is provided by the high speed RC oscillator. The program is executed. After the power-on reset or any of the reset triggers, the system enters the high-speed mode to execute the program. In high speed mode, the high speed oscillator works normally and the power consumption is maximum.

- The program is executed and all functions are controlled
- The system speed is high
- Both the high speed oscillator and the internal low speed oscillator are working properly
- The high-speed mode can be switched to the low-speed mode
- Go from high speed mode to sleep mode, wake up and return to high speed mode
- Go from high speed mode to idle mode, wake up and return to high speed mode

3.11.2 Low-speed Mode

Low-speed mode indicates the system low-speed clock working mode. The system clock source is provided by an internal low speed RC oscillator. The low speed mode is controlled by the CPUS of the system clock and the status control register. When CPUS=1, the system is in high speed mode. When CPUS=0, the system enters the low-speed mode. After entering the low - speed mode, the high - speed oscillator is automatically disabled.

- The program is executed and all functions are controlled
- The system speed is low
- The internal low speed oscillator works normally and the high speed oscillator stops working
- The low mode can be switched to the high mode
- Go from low mode to sleep mode, wake up and return to low mode
- Go from low mode to idle mode, wake up and return to low mode

3.11.3 Idle Mode

Idle mode is another ideal state. In sleep mode, all functions and hardware devices are disabled, but in idle mode, the system's low speed clock keeps working, and the power consumption in idle mode is greater than that in sleep mode. In idle mode, no program is executed, but INT0, INT1, P5/P6/P7IC with wake up function (port change), TC0, TC1, PWM(period and duty cycle interrupt overflow), ADC, CMP0, CMP1, WDT still work

normally. Timer TC0,TC1 and PWM clock sources are the system's low speed clocks that are still working.The IDLE bit of the system clock and the status control register determines whether to enter the IDLE mode. When IDLE=1, the idle mode is entered after the execution of SLEEP.

- The program stops execution and all functions are disabled
- The module with the wake up function works properly
- Low - speed oscillator works normally, other oscillators stop working
- Enter idle mode from high speed mode and return to high speed mode after being awakened
- Enter idle mode from low mode and return to low mode after being awakened
- Idle mode of sensei TMRWE, ICWE, EXOWE, EX1WE, ADWE, CMPOWE, CMP1WE, WDTWE
- The TC0, TC1, and PWM functions are still available in idle mode

3.11.4 Sleep Mode

Sleep mode is the ideal state of the system, where no program is executed and the oscillator stops working.The entire chip consumes less than 1uA.Sleep patterns can be made by TC0 (P67 input TC0 count clock), ICWE, EXOWE, EX1WE, ADWE, CMPOWE, CMP1WE, WDTWE sensei.Go to sleep from high or low speed mode and return to the corresponding mode when you wake up.The IDLE bit of the system clock and the status control register controls whether to enter the SLEEP mode. When IDLE=0, the sleep mode is entered after execution.

- The program stops execution and all functions are disabled.
- All oscillators, including external high speed oscillators, internal high speed oscillators, and internal low speed oscillators stop working;
- Power consumption is less than 1uA;
- From high speed mode to sleep mode, wake up to return to high speed mode;
- From low mode to sleep mode, wake up to return to low mode;
- Wake up way for TC0 sleep mode (P67 input), ICWE, EXOWE, EX1WE, ADWE, CMPOWE, CMP1WE, WDTWE;

3.12 EEPROM Live erasable Programmable memory

The JZ8F8003 has a 128 * 8Bit EEPROM with the address 0X00-0X7F (R87/TBRDL register).EEPROM memory contents can not be mapped directly to the register, through the R87/TBRDL address register map EEPROM address, through the TBRD table lookup instruction to read it, through the RE1/EEPDAT register assign the corresponding write data, enable the write operation, the chip automatically write data.EEPROM function module has 2 SFR registers for read and write control:

- RE0/EEPCON (EEPROM Read/write control register)
- RE1/EEPDAT (EEPROM write data register)

Note: Keep the power supply voltage above 2.6v during the write operation. During the write operation, the chip executes sleep.

3.12.1 EEPROM Application Description

Data read operation

- Set the address to be read to the R87/TBRDL register
- Set the read enable EEREAD to 1
- The "TBRD R" command reads the data to ACC

  Note: The value of the R register will still be overwritten and the data will be random, please pay attention in use.
- Disable data reading after data reading is complete Enable EEREAD

Write data operation

- Set the address to write to the R87/TBRDL register
- Set the data to be written to the RE1/EEPDAT register
- Set the write operation to enable the EEWRIT bit to 1 and reset the hardware after the write is complete
- Wait until the write is complete. If a write operation error occurs, the EE_WRERR flag bit is set to 1, and the software can clear the 0

4 CODE OPTION Configuration table

CODE OPTION	Option	Function Description
WDT	Enable	WDT Enable
	Disable	WDT Disable
P52 Port	RESET	P52 serves as an external RESET
	GPIO	P52 as GPIO
External interrupt filtering (NR)	8Fosc	Filtering time 8Fosc
	32Fosc	The filtering time is 32Fosc
LVR	1.8 V	LVR select 1.8V
	2.9 V	LVR select 2.9V
	3.7 V	LVR select 3.7V
	4.2 V	LVR select 4.2V
System clock warm up	8 Fosc	System clock warm-up time selection 8Fosc
	32 Fosc	System clock warm-up time selection 32Fosc
Reset time	4.5ms	System setup time select 4.5ms
	18ms	System setup time select 18ms
Oscillation mode	IRC mode	Oscillation mode select internal RC oscillation
	ERC mode	Oscillation mode select external RC oscillation
	LXT1 mode	External crystal frequency select 100K～1M
	LXT2 mode	External crystal frequency select 32.768K
	HXT1 mode	External crystal frequency select 12M～16M
	HXT2 mode	External crystal frequency select 6M～12M
	XT mode	External crystal frequency select 1M～6M
P61 Port	GPIO	P61 as GPIO
	Command cycle output	P61 as the command cycle output,RCOUT open leakage output is prohibited
	Command cycle output	P61 as the command cycle output,RCOUT enable leakage output
IRC frequency	1M	RC select 1M
	4M	RC select 4M
	8M	RC select 8M
	16M	RC select 16M
Clocks division	2Clocks	Instruction cycle select 2Clocks(not recommended)
	4Clocks	Instruction cycle select 4Clocks
	8Clocks	Instruction cycle select 8Clocks
	16Clocks	Instruction cycle select 16Clocks
Fs clock selection	128KHz	Fs select 128KHz
	16KHz	Fs select 16KHz

Power selection	High speed and high power consumption	Fcpu>=2M selecting (Fcpu = oscillator frequency / clocks division)
	Normal	Fcpu< 2M selecting (Fcpu = oscillator frequency / clocks division)
The ADC sampling value is forcibly raised by 14 least significant bits	ban	The 14 least significant bits cannot be increased
	Can make	Enable to raise the 14 least significant bits (Applicable only when the AD port sampling is less than 5mV).
RTC	Disable	The RTC clock is disabled
	Enable	The RTC clock was enabled
System clock filtering	Disable	Prohibited (must be prohibited when the oscillator clock frequency is 8M or 16M)
	Enable	The system clock filtering function is enabled
Full film erase	Disable	Forbidden (Recommended)
	Enable	Enable (longer burning time)
OS Testing	Disable	OS test forbidden (only for board burning)
	Enable	OS test enable (chip is placed on burner to burn)

5 Electrical characteristics

5.1 IC Limiting Characteristics

Temperature under bias (℃):	(√) E:-40-85;
Storage temperature (℃):	(√) -65～+150
Limit voltage (V)	(√) -0.3～6
Input voltage (V)	(√) GND-0.3～VDD+0.5;
Output voltage (V)	(√) GND-0.3～VDD+0.5;

5.2 DC Electrical Characteristics

(T=25℃, VDD=5V,GND=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ERC	External resistance capacity oscillation	R: 5.1 K Ω, C: 100 pf	0.76	0.95	1.14	MHz
IRC1	IRC1 (after correction)	OPTION Selects 16MHz		16		MHz
IRC2	IRC2 (after correction)	OPTION Select 8MHz		8		MHz
IRC3	IRC3 (after correction)	OPTION Selects 4MHz		4		MHz
IRC4	IRC4 (after correction)	OPTION Selects 1MHz		1		MHz
VIH1	Input high level	P5, P6, P70, P71	0.6＊VDD		VDD	V
VIL1	Input low level	P5, P5, P70, P71	0.3 V		0.4 ＊ VDD	V
IOH1	Output high level drive	IOH = VDD - 0.6 V	3.5	4.5	4.7	mA
IOH2	Output high level drive enhancement	IOH = VDD - 0.6 V	7	10	12	mA
IOL1	I/O output low level drive	IOL = GND + 0.6 V	15	19	21	mA
IOL2	IO output low drive enhancement	IOL = GND + 0.6 V	40	45	50	mA
RPH1	Pull-up resistor (@3v)		-	130	-	K Ω
RPH2	Pull-up resistor (@5v)		-	65	-	K Ω
RPL1	Pull-down resistor (@3v)		-	130	-	K Ω
RPL2	Pull-down resistance (@5v)		-	70	-	K Ω
Isb1	Sleep Current 1 (regular sleep)	All inputs are connected to VDD, output is suspended, WDT and LVD are disabled	0.5	1	2	μA
Isb2	Sleep Current 2(WDT wake up)	All input is connected to VDD, output is suspended, WDT is		10	12	μA

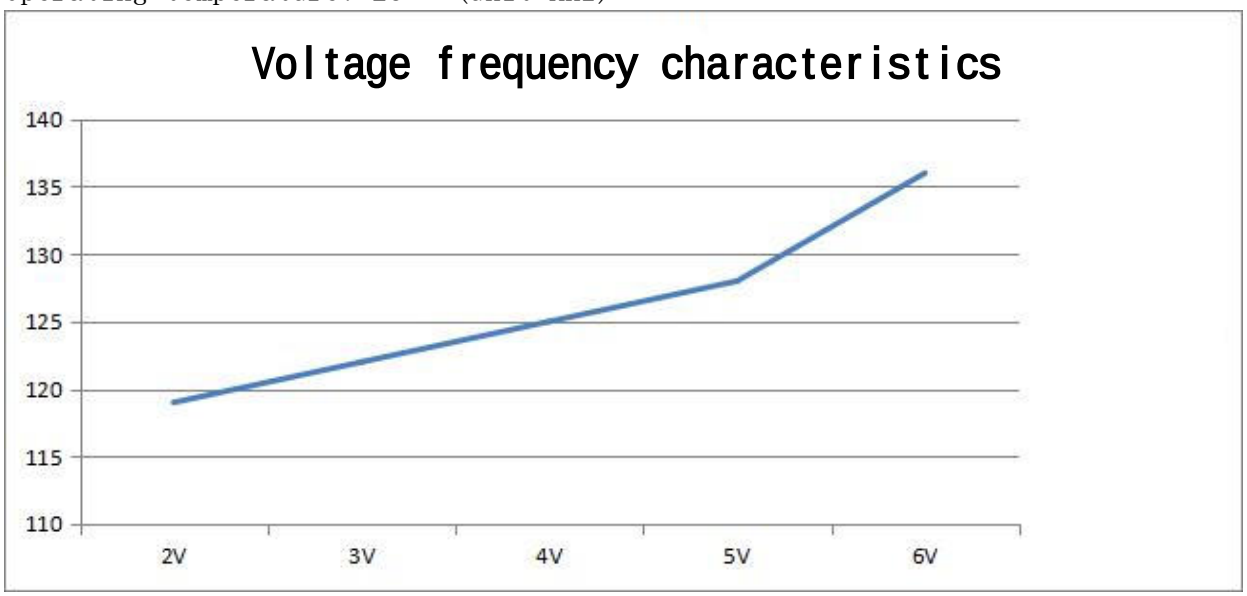
		enabled, LVD is disabled				
Isb3	Sleep current 3(RTC wake up)	All input is connected to VDD, output is suspended, WDT is disabled, LVD is disabled		8	10	μA
Isb4	Sleep current 4	All input is connected to VDD, output is suspended, LVD is enabled, WDT is disabled		5	6	μA
Iop1	Operating current 1 (high power mode)	4MHz, 2clks, 5v		2.1	2.5	mA
Iop2	Operating current 2 (normal mode)	4MHz, 2clks, 5v		1.6	1.8	mA
Iop3	Operating current 3 (High power mode)	16MHz, 2clks, 5v		3.2	3.5	mA
Iop4	Operating current 4 (normal mode)	16MHz, 8clks, 5v		2	2.5	mA
LVR	Low voltage reset voltage	Select the Vlvr reset point	Vlvr - 0.2 -	Vlvr	Vlvr + 0.2	V
LVD	Low voltage detection voltage	Select Vlvd as the detection point	Vlvd - 0.2 -	Vlvd	Vlvd + 0.2	V
Note: The above parameters are for reference only. Please refer to the measured data of the target prototype.						

5.3 Feature Curve

The graphs listed in this chapter are for reference only. Some data may exceed the specified working range of the chip. To ensure the normal working of the chip, strictly refer to the electrical characteristics.

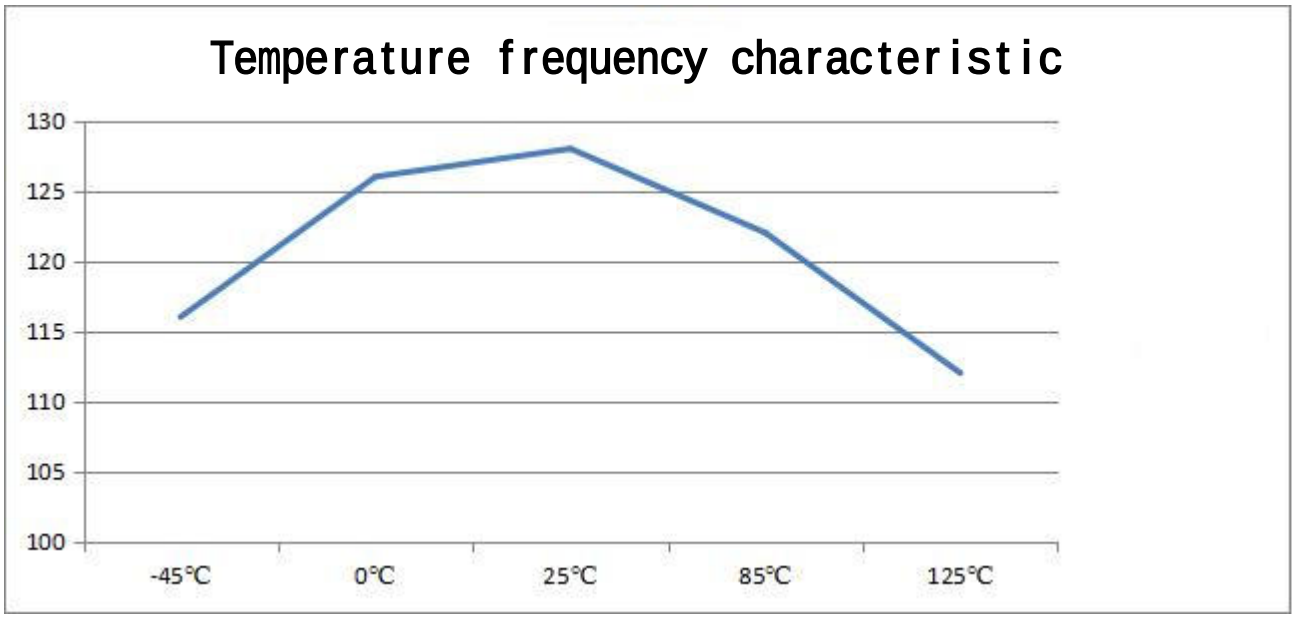
5.3.1 Internal low speed 128K RC oscillator - voltage frequency characteristic curve

Operating temperature: 25℃ (unit Khz)



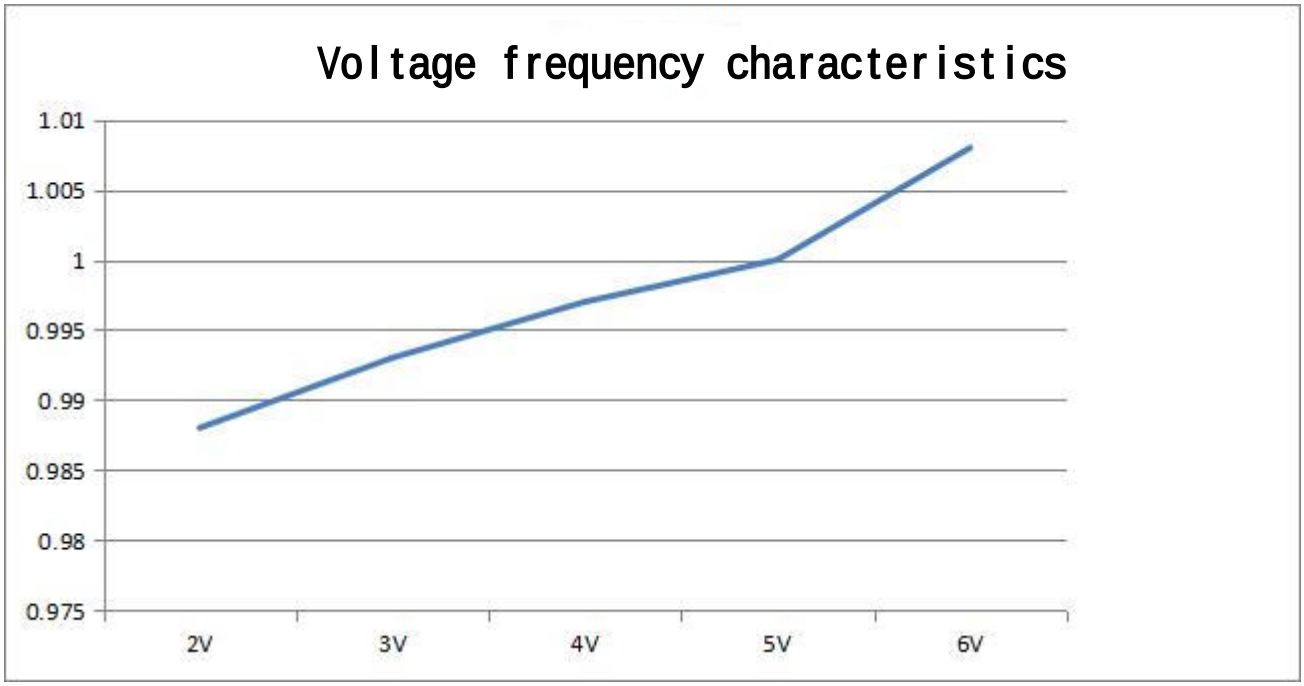
5.3.2 Internal low speed 128K RC oscillator -- temperature-frequency characteristic curve

Operating voltage at 5V: (unit Khz)



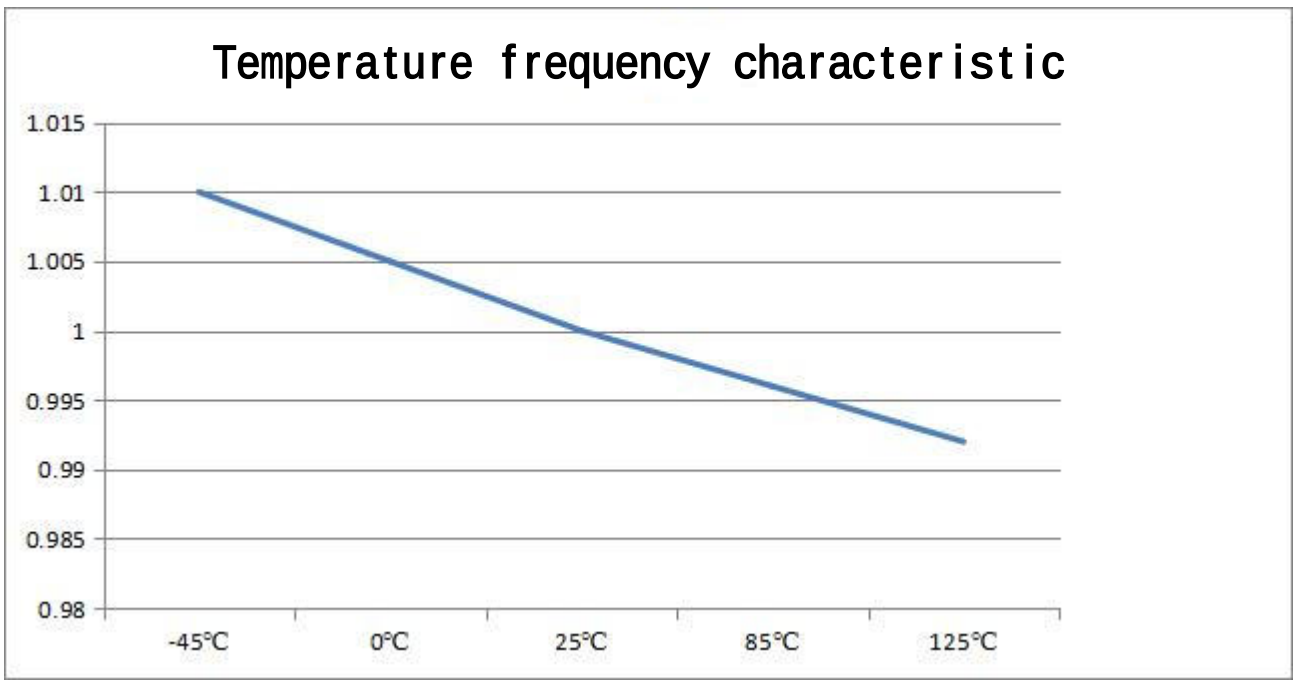
5.3.3 Internal 1Mhz RC oscillator - voltage frequency characteristic curve

Operating temperature: 25℃ (unit Mhz)



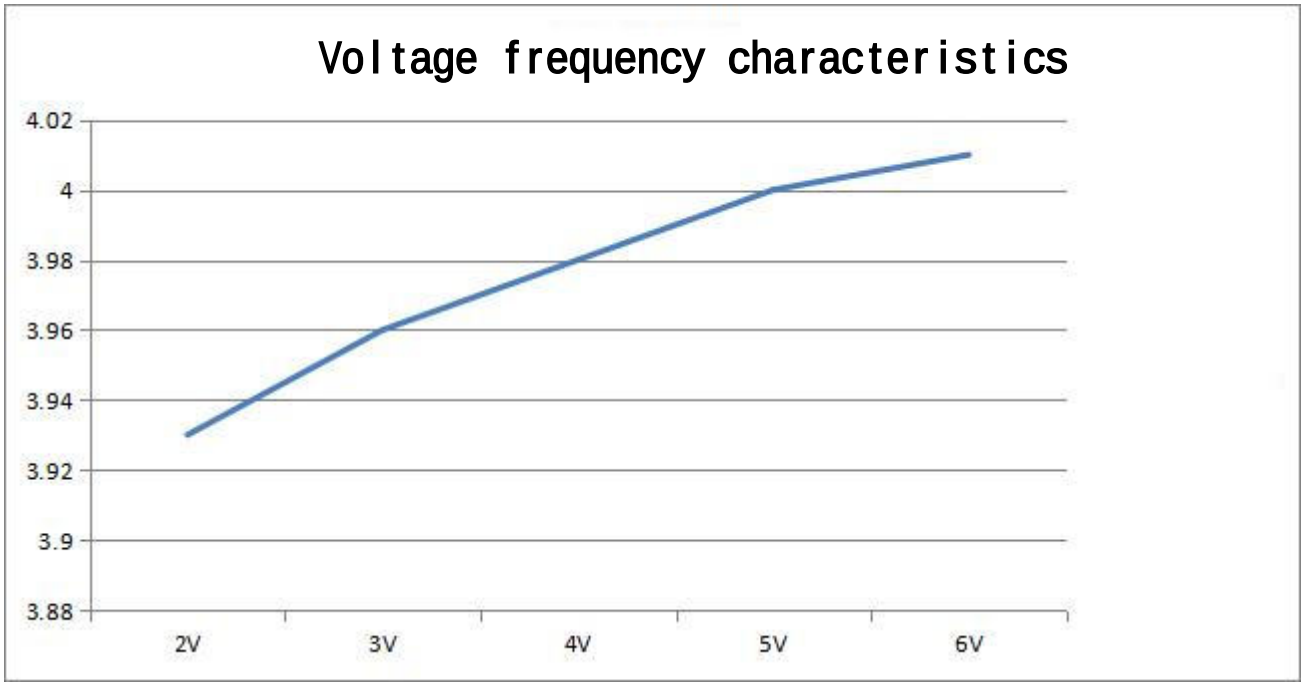
5.3.4 Internal 1Mhz RC oscillator - temperature-frequency characteristic curve

Operating voltage at 5V: (unit Mhz)



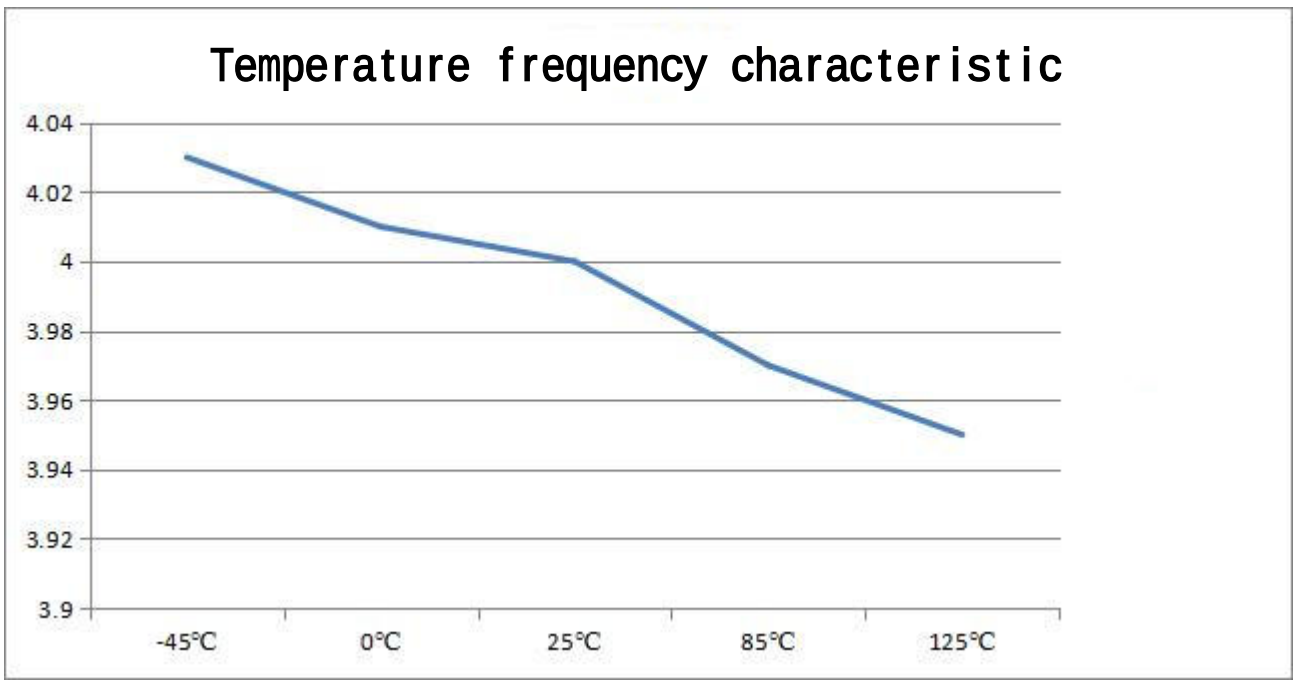
5.3.5 Internal 4Mhz RC oscillator - voltage frequency characteristic curve

Operating temperature: 25℃ (unit Mhz)



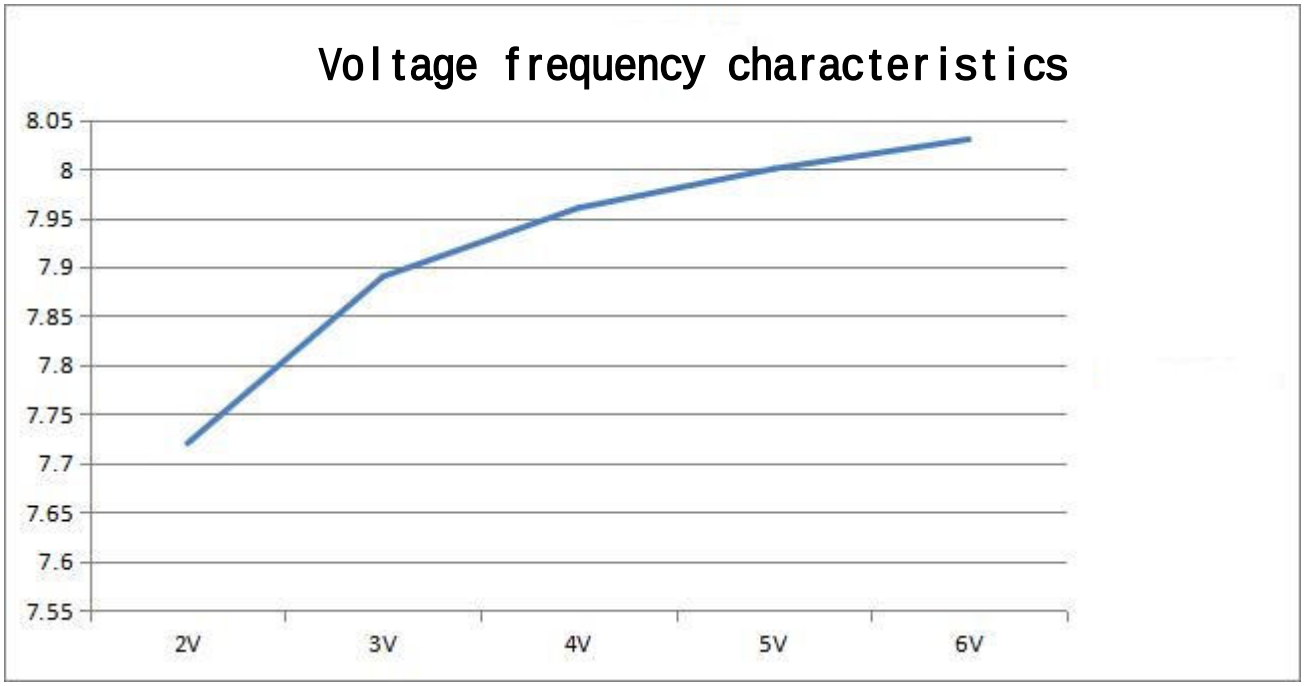
5.3.6 Internal 4Mhz RC oscillator -- temperature-frequency characteristic curve

Operating voltage at 5V: (unit Mhz)



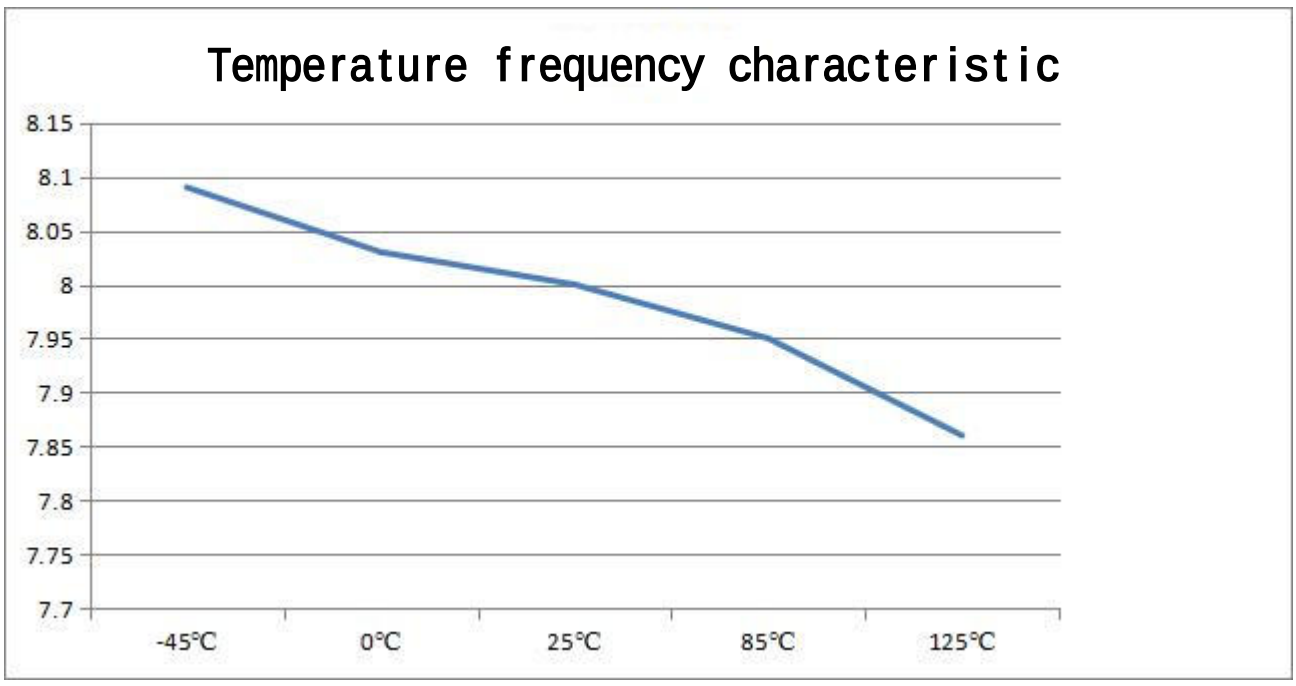
5.3.7 Internal 8Mhz RC oscillator - voltage frequency characteristic curve

Operating temperature: 25℃ (unit Mhz)



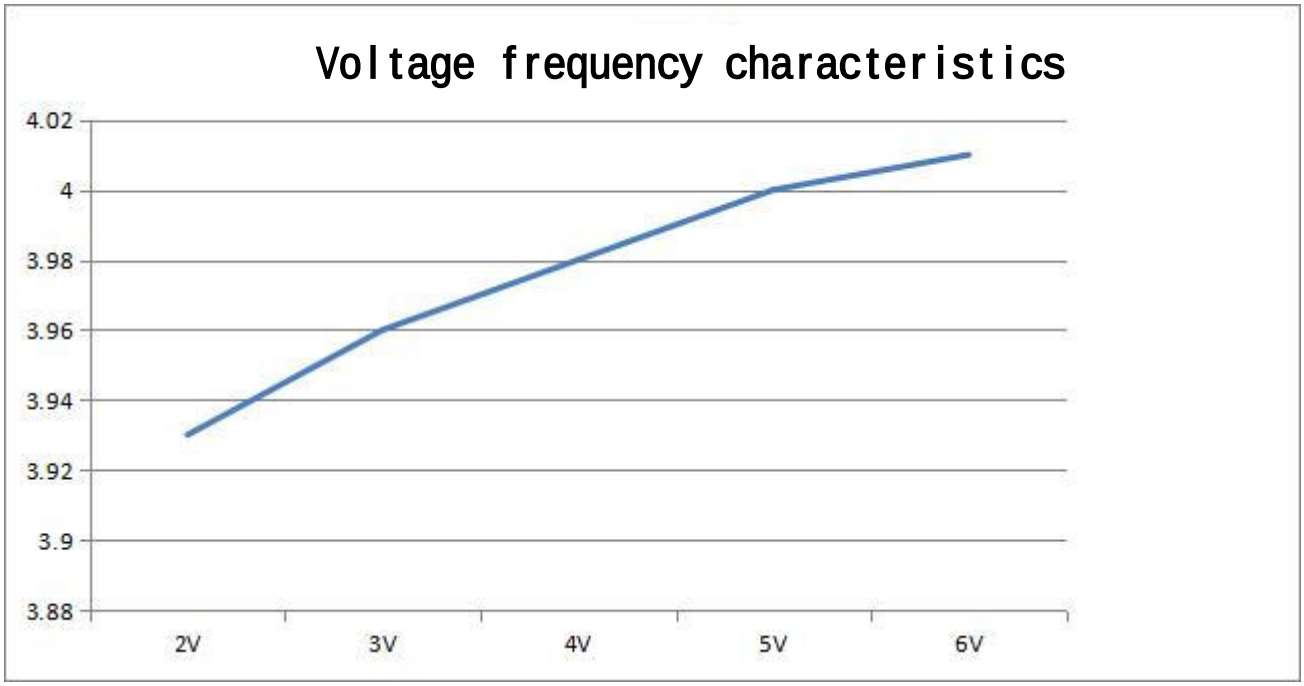
5.3.8 Internal 8Mhz RC oscillator -- temperature-frequency characteristic curve

Operating voltage at 5V: (unit Mhz)



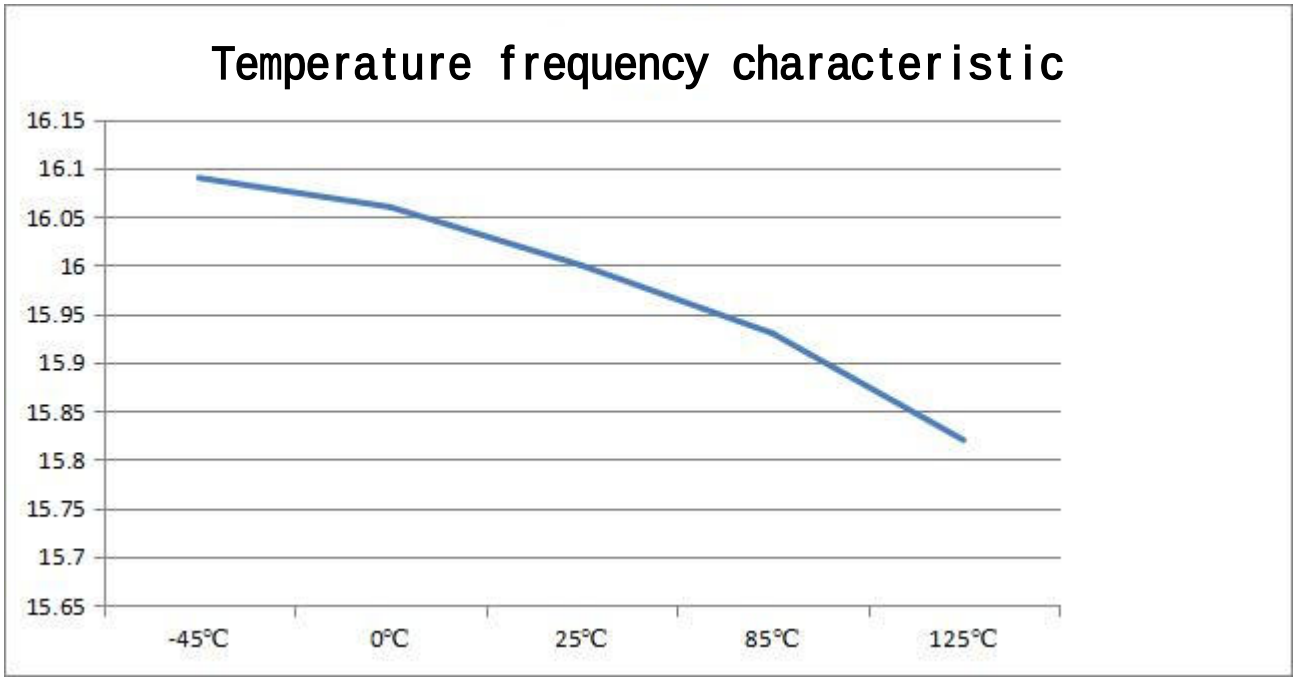
5.3.9 Internal 16Mhz RC oscillator - voltage frequency characteristic curve

Operating temperature: 25℃ (unit Mhz)



5.3.10 Internal 16Mhz RC oscillator -- temperature-frequency characteristic curve

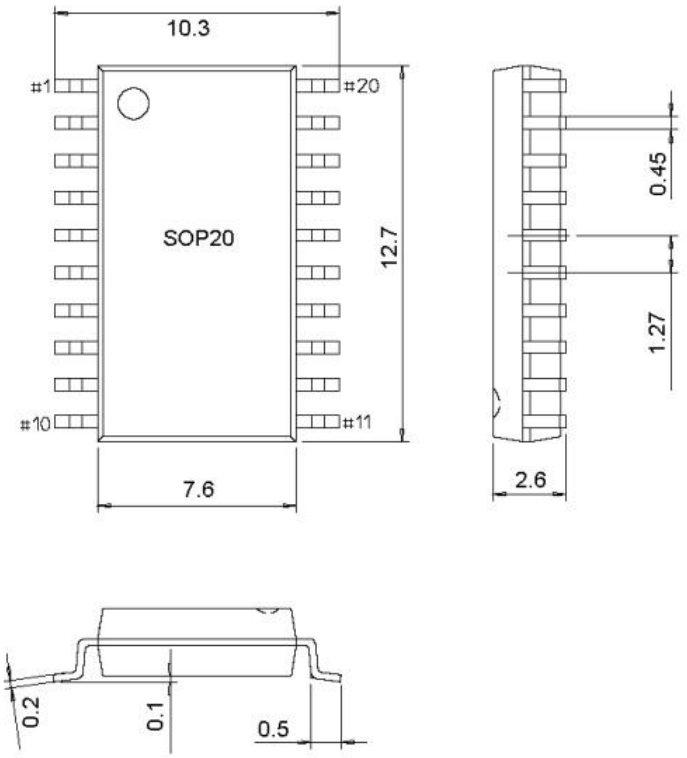
Operating voltage at 5V: (unit Mhz)



6 Packaging Configuration

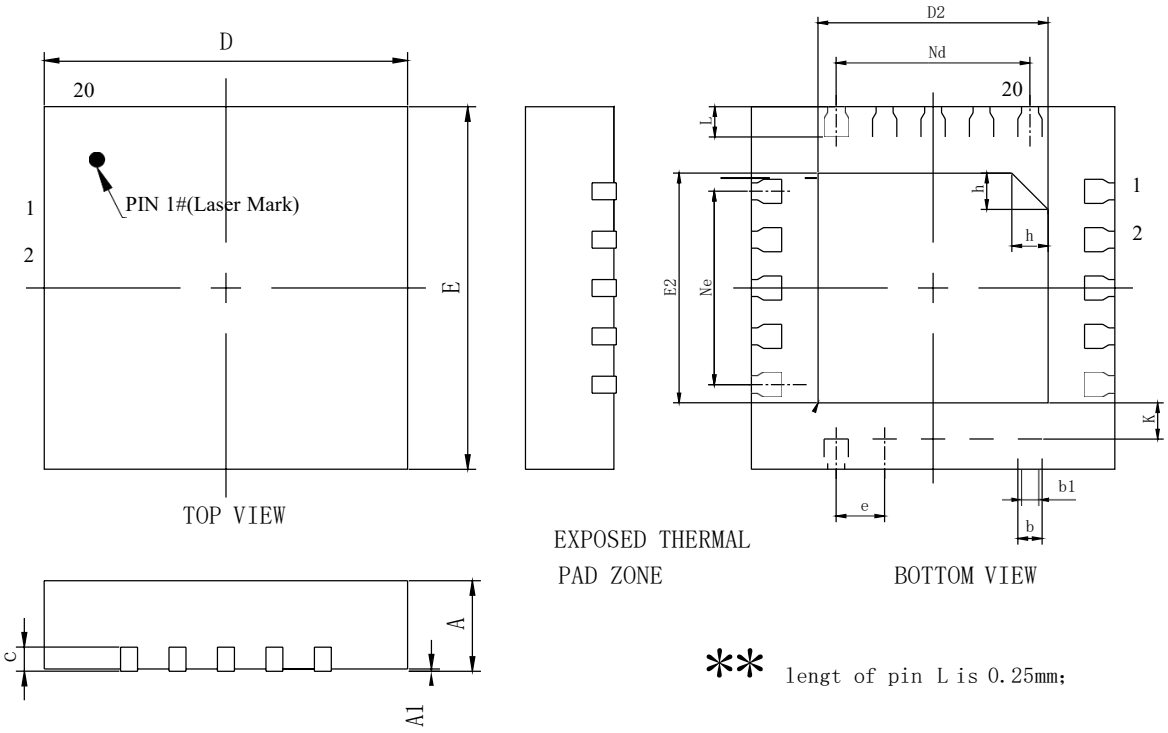
6.1 SOP20PIN Packaging

（unit:mm）



SOP20 package size

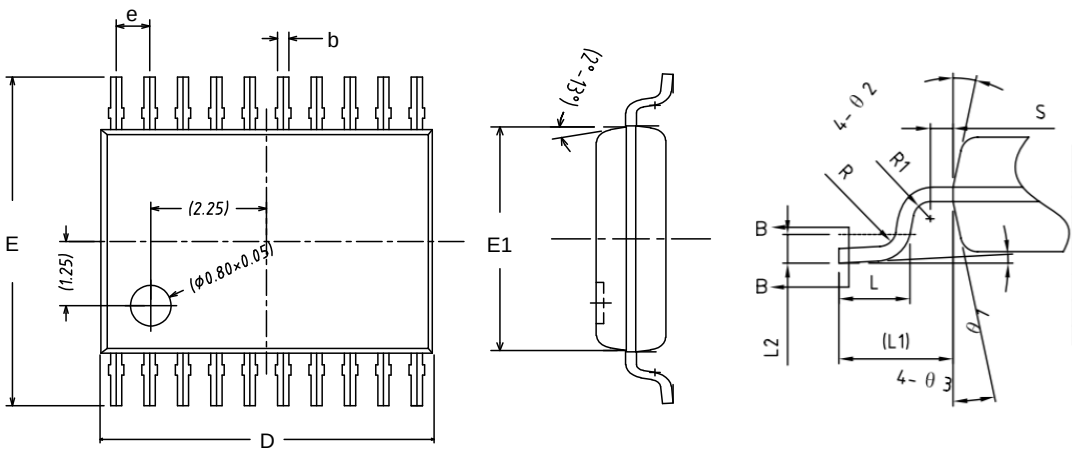
6.2 QFN20 Packaging

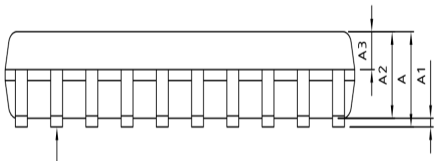


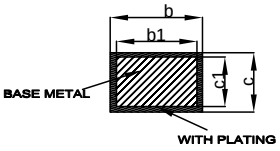
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.203REF		
D	2.90	3.00	3.10
D2	1.80	1.90	2.00
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
L	0.20	0.25	0.30
h	0.25	0.30	0.35
K	0.30REF		

** lengt of pin L is 0.25mm;

6.3 TSSOP20 Packaging







SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.0	----	1.10
A1	0.05	----	0.15
A2	0.90	0.95	1.0
A3	0.39	----	0.40
b	0.20	0.22	0.24
c	0.10	----	0.19
c1	0.10		0.15
D	6.40	6.45	6.50
E	6.25	6.40	6.55
E1		4.35	4.40
L	0.50	0.60	0.70
e	0.55	0.65	0.75
L2	0.25BSC		
R	0.09		
L1	1.0REF		
θ1	0°	----	8°

7 ESD performance description

Test Categor	Test Condition	Remarks
ESD(HBM)	>|±3KV| (TA=25℃)	IO TO IO (+) IO TO IO (-) All other pins to VCC (-) All other pins to VCC (+) All other pins to VSS (-) All other pins to VSS (+)
ESD(MM)	>|±500V| (TA=25℃)	
ESD(CDM)	>|±500V| (TA=25℃)	

*The test is based on ANSI-ESDA-JEDEC-JS-002-2018