JZ8M4600

8-bit MTP Microcontroller

User Data Manual

Version V1.5

Modification Record Description

Version Number	Modification Description	Remarks
V0.0	Draft	
V0.1	Release initial version	
V1.0	Revised relevant descriptions and updated electrical characteristic waveforms	
V1.1	Revised erroneous descriptions	
V1.2	Corrected the pin diagram erroneous descriptions	
V1.3	Revised erroneous descriptions, added T20B pin diagram and dot matrix distribution schematic	
V1.4	Revise error descriptions and add E2 writing notes	
V1.5	Revised erroneous descriptions	

Notes:

1、Do not use TC0 and TC3 as clock sources for IIC/SPI;

2、Do not use TC0 as a clock source for UART.

3. SPI mode prohibits the use of Mode 1 (CPOL=0, CPHA=1);

4. The AD reference must be set to VDD before sleep, otherwise there will be power consumption;

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1. Chip Introduction

1.1 Functional Features

CPU Configuration

- 4K×16-Bit MTP ROM
- 256×16-Bit EEPROM
- 256×8-Bit SRAM
- 8-level stack space
- 8-level programmable voltage reset (LVR)
  1.8V, 1.9V, 2.1V, 2.3V
  2.7V, 3.0V, 3.5V, 4.0V
- Operating current < 2 mA (8MHz/5V)
- Operating current < 10 uA (36KHz/5V)
- Sleep current < 1 uA (sleep mode)

I/O configuration

- 3 groups of 18 bi-directional IO ports: P5, P6, P7
- Wake-up ports: P5, P6, P7
- 18 programmable pull-up I/O pins
- 18 programmable drop-down I/O pins
- External interrupts:
  INT0: P50/P54 INT1: P60/P65

Operating voltage

- Operating voltage range:
  V_{LVR}3.0V～5.5V | Fcpu=0～8MHz
  V_{LVR}2.3V～5.5V | Fcpu=0～4MHz
  V_{LVR}1.9V～5.5V | Fcpu=0～2MHz

Operating frequency range

- Internal IHRC oscillator circuit: 32MHz/16MHz/8MHz/4MHz/1MHz
- Internal ILRC Oscillation Circuit: 36KHz
- Clock Cycle Division Selection: 2T, 4T, 8T, 16T, 32T

Peripheral Modules

- 18-channel 12Bit ADC Converter
- 1 External 1/4 ADC Sampling EXV/4
- 1 DAC with Output, Comparison, and Sampling Functions
- 8 Bit Timer Counter TC0
- 16 Bit Timer Counter TC3
- 3 12Bit-PWM Channels (a pair of complementary)
- 4 channels 1 group 12Bit-PWM (a pair of complementary)
- 1 UART/IIC/SPI3-in-1 interface
- 1 comparator CMP
- 1 port level capture (4 ports options)
- PWM can trigger AD sampling
- 2 channels RGB LED cascading controllers (for driving RGB lights)
- LED dot matrix driver supports up to 8*8

Interrupt Sources

- TC0/TC1/TC2/TC3 timer interrupt
- External Interrupt 1
- External Interrupt 0
- P7 Port Input Change Interrupt
- P6 Port Input Change Interrupt
- P5 Port Input Change Interrupt
- ADC Conversion Complete Interrupt
- PWM7 Duty Cycle Match Interrupt
- CMP State Change Interrupt
- E2P Write Complete Interrupt
- UART Receive/SPI Completion Interrupt
- UART Send/IIC Completion Interrupt

Features

- Programmable WDT Timer
- Four Working Mode Switches
- Two Groups of Programming Ports Available
- Supports Type-C Port Upgrade, Supports Live Programming

Package Type

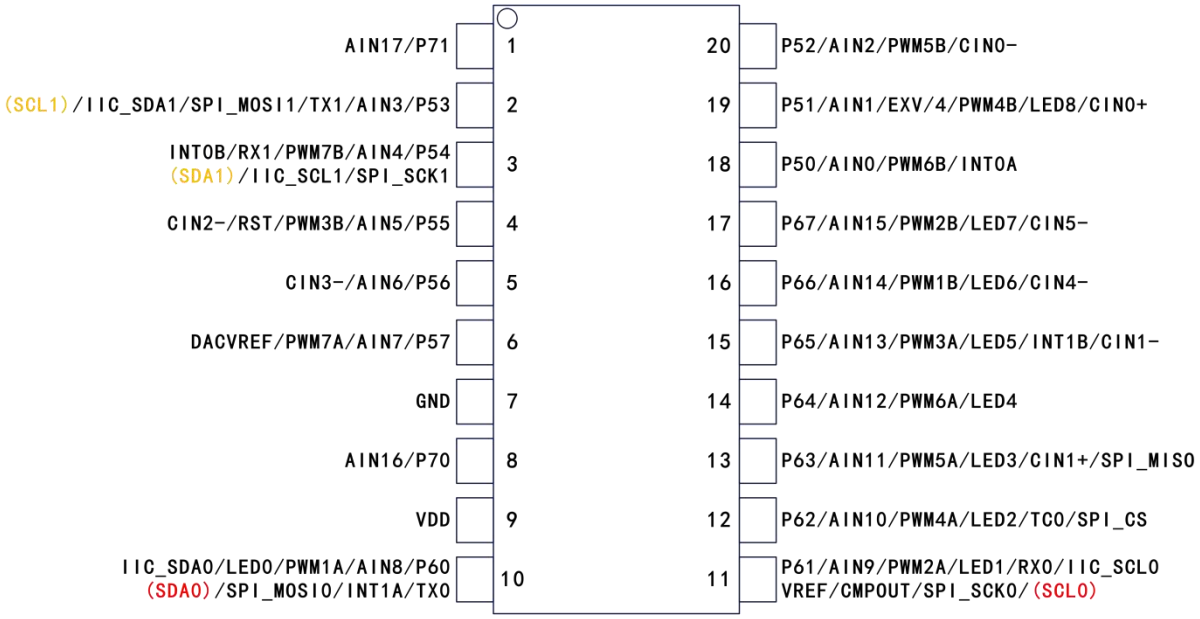
- JZ8M4600-TSSOP20/QFN20
- JZ8M4600-SOP16/QFN16
- JZ8M4600-SOP8

1.2 Model Description

PRODUCT	ROM	RAM	EEPROM	I/O	ADC	UART	IIC	SPI	DAC	Dot Matrix	PACKAGE
JZ8M4600T20	4K*16	256*8	256*16	18	18	Y	Y	Y	Y	8*8	TSSOP20
JZ8M4600T20B	4K*16	256*8	256*16	18	18	Y	Y	Y	Y	8*8	TSSOP20
JZ8M4600Q20	4K*16	256*8	256*16	18	18	Y	Y	Y	Y	8*8	QFN20
JZ8M4600S16	4K*16	256*8	256*16	14	14	Y	Y	Y	Y	8*8	SOP16
JZ8M4600Q16	4K*16	256*8	256*16	14	14	Y	Y	Y	Y	8*8	QFN16
JZ8M4600S08	4K*16	256*8	256*16	6	6	Y	Y	-	-	-	SOP8

1.3 Pin Allocation

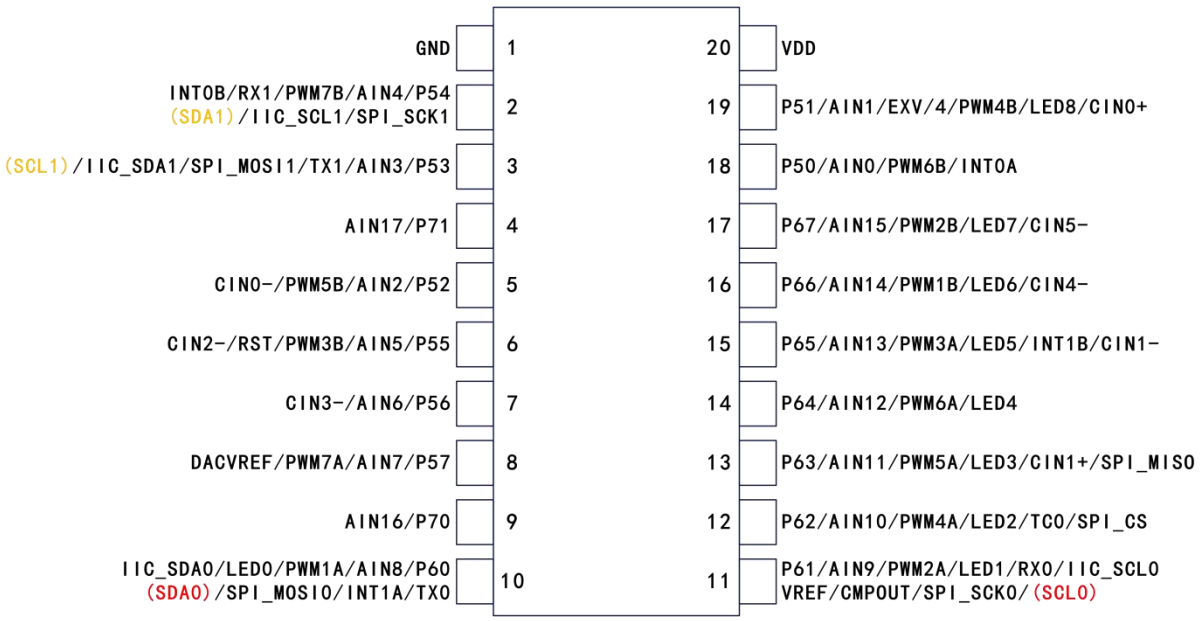
Model: JZ8M4600T20 (Main Recommendation)



TSSOP20 Pin Diagram

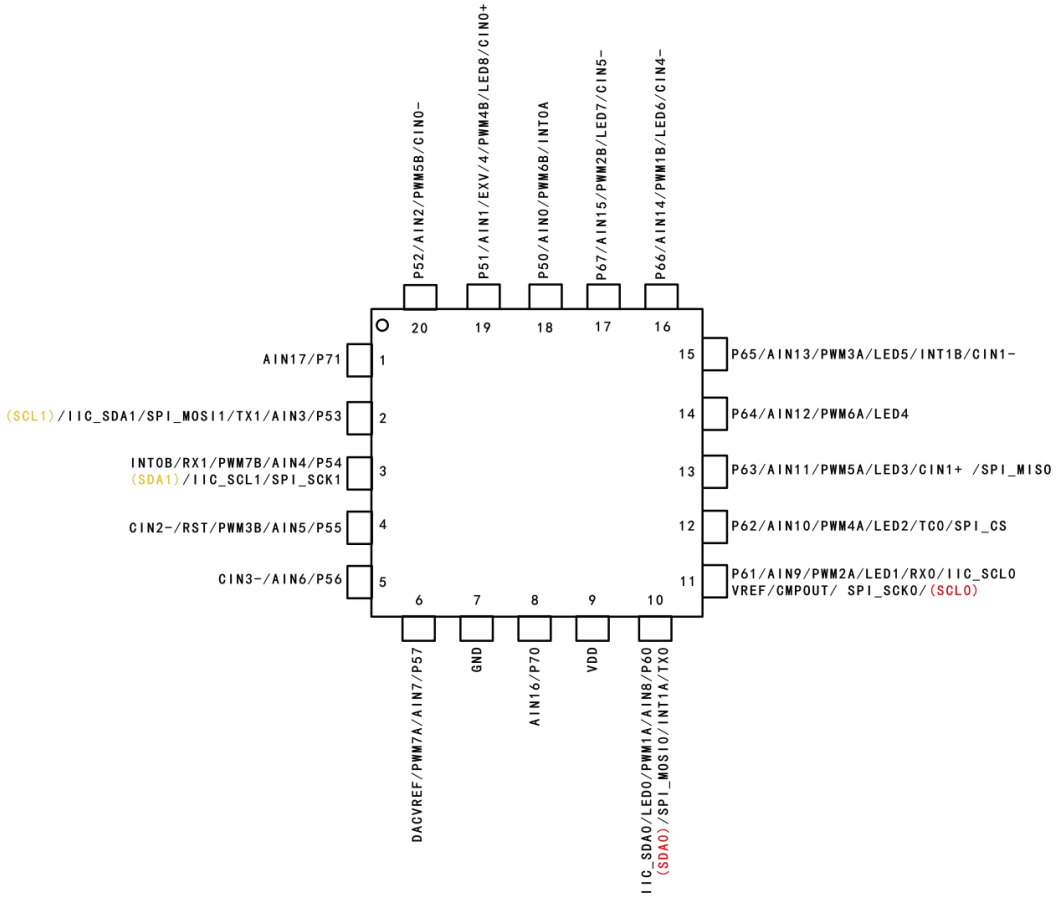
JZ8M4600 simulation download and programming port: P60 (SDA0), P61 (SCL0) or P53 (SCL1), P54 (SDA1)

Model: JZ8M4600T20B



TSSOP20 Pin Diagram

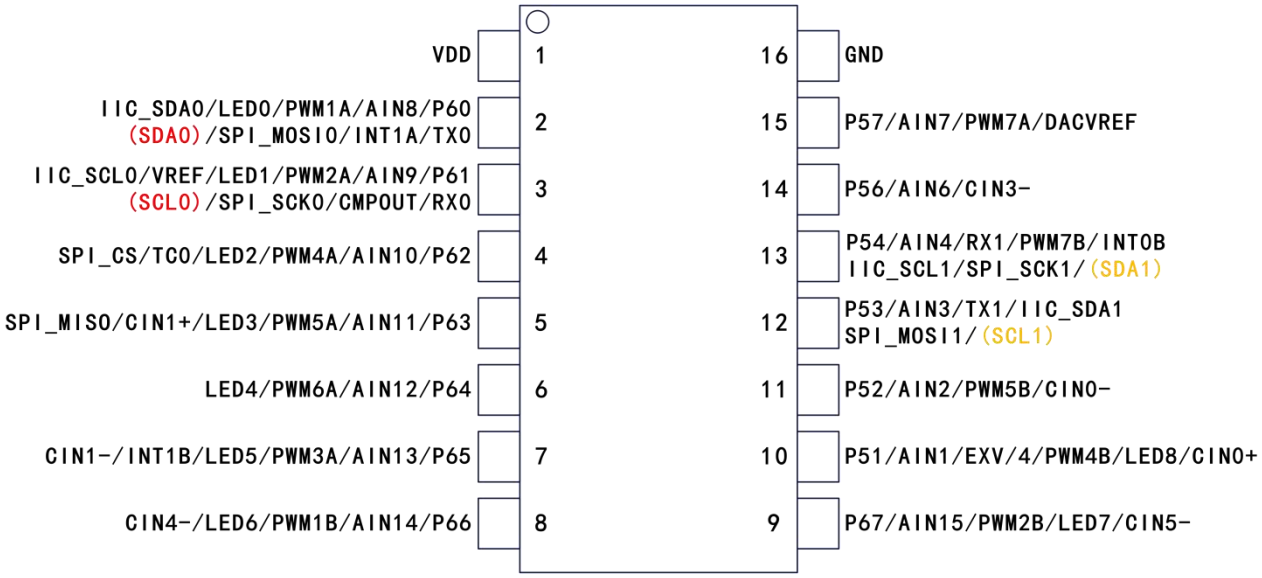
Model: JZ8M4600Q20



QFN20 pin diagram

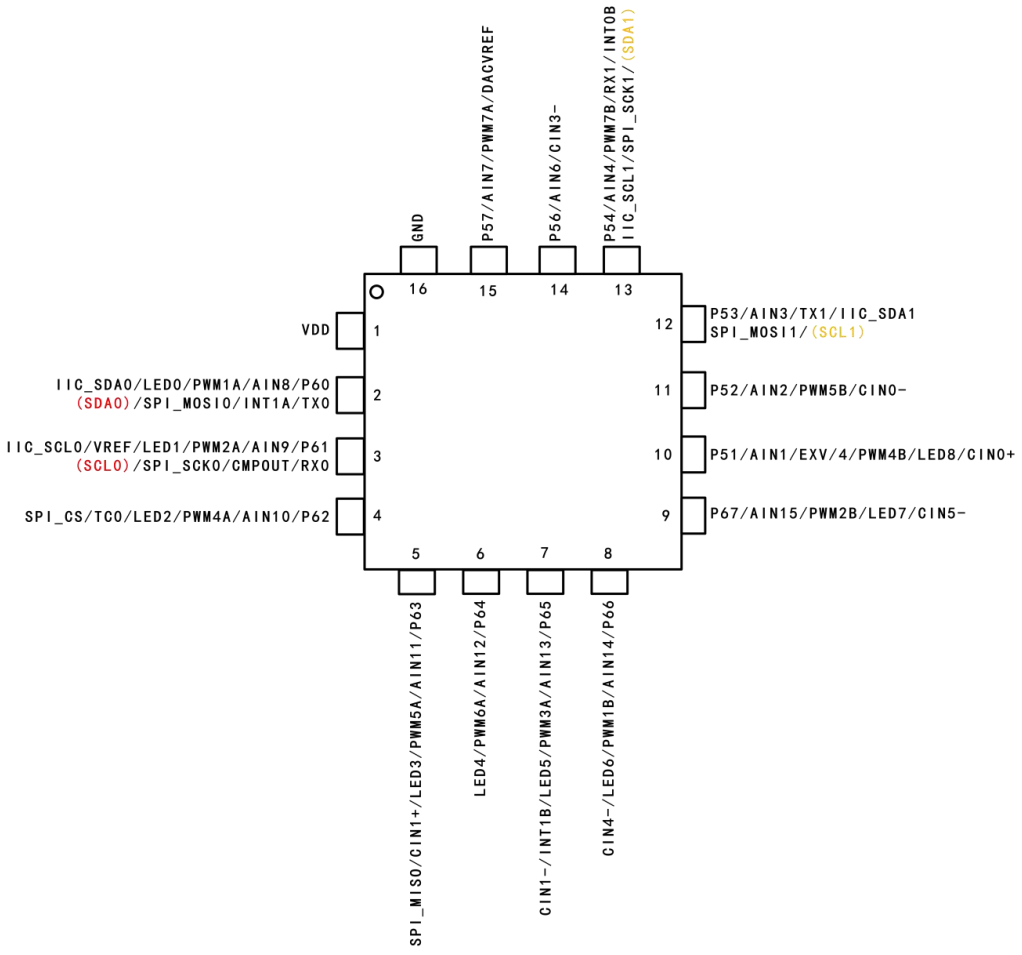
JZ8M4600 simulation download and programming port: P60 (SDA0), P61 (SCL0) or P53 (SCL1), P54 (SDA1)

Model: JZ8M4600S16



SOP16 pin diagram

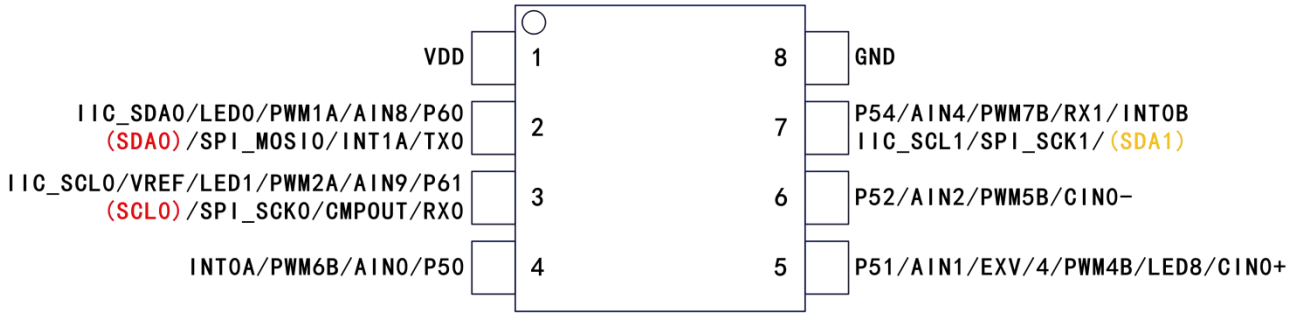
Model: JZ8M4600Q16



QFN16 pin diagram

JZ8M4600 simulation download and programming port: P60 (SDA0), P61 (SCL0) or P53 (SCL1), P54 (SDA1)

Model: JZ8M4600S08



SOP8 pin diagram

JZ8M4600 simulation download and programming port: P60 (SDA0), P61 (SCL0) or P53 (SCL1), P54 (SDA1)

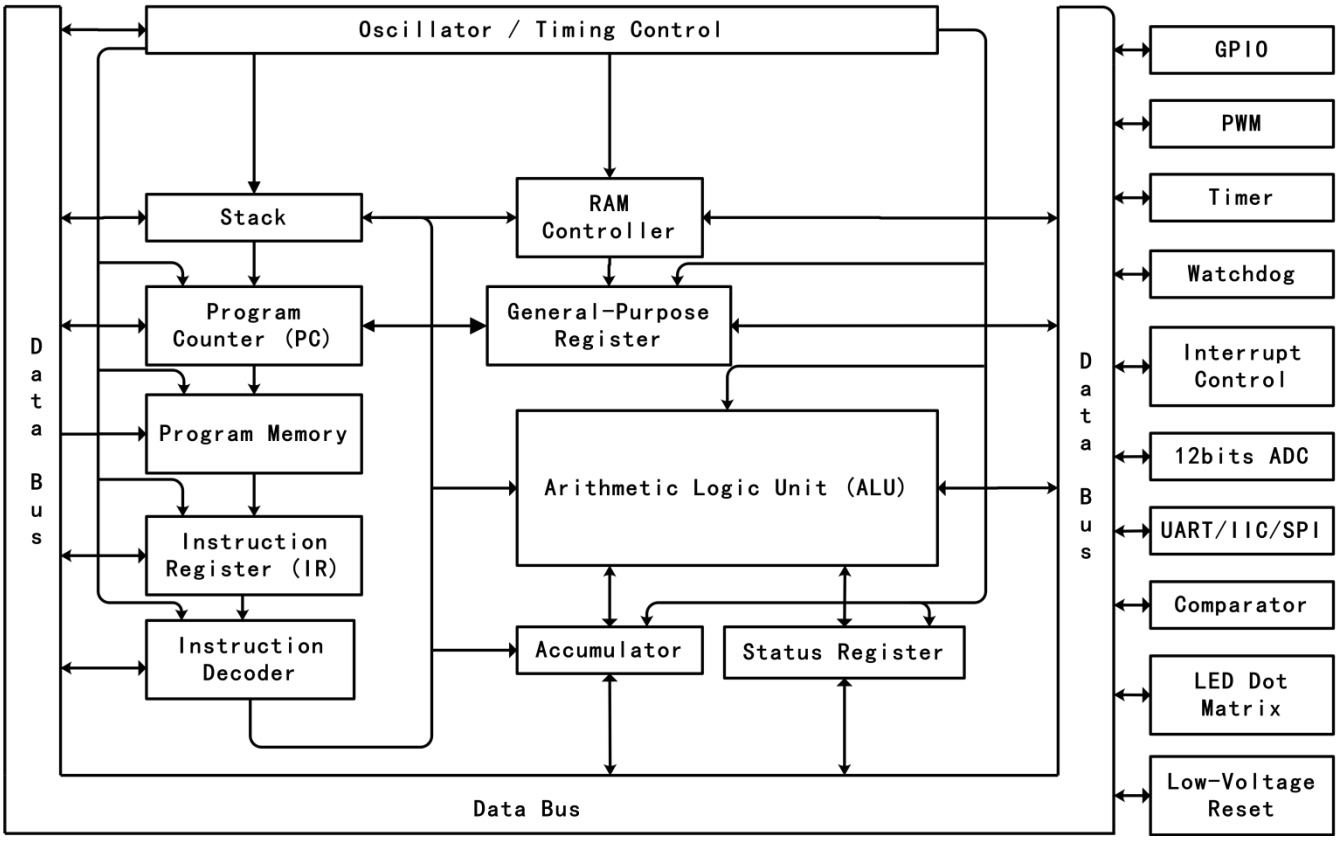
1.4 Pin Description

Number	Pin Name	I/O	Function Description
P50	P50	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN0	AN	Analog Input Channel 0
	PWM6B	O	PWM6B output
	INT0A	I	External interrupt INT0 input port
P51	P51	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN1	AN	AIN analog input channel 1
	PWM4B	O	PWM4B output
	LED8	O	LED drive port 8
	EXV/4	AN	External 1/4 ADC Sampling
	CIN0+	AN	Comparator Positive Input
P52	P52	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN2	AN	AIN Analog Input Channel 2
	PWM5B	O	PWM5B Output
	CIN0-	AN	Comparator Negative Input
P53	P53	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN3	AN	AIN Analog Input Channel 3
	TX1	O	UART Transmit Port
	IIC_SDA1	O	IIC Data Port
	SPI_MOSI1	I/O	SPI Master Output, Slave Input Data Port
	(SCL1)	I	Burning Timing Port 1
P54	P54	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN4	AN	AIN Analog Input Channel 4
	INT0B	I	External interrupt INT0 input port
	PWM7B	O	PWM7B Output
	RX1	I	UART Receive Port
	IIC_SCL1	I/O	IIC Clock Port
	SPI_SCK1	O	SPI Master Mode Clock Pin
	(SDA1)	I	Burning Timing Port 1
P55	P55	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN5	AN	AIN Analog Input Channel 5
	PWM3B	O	PWM3B Output
	RST	I	External Reset Input Port
	CIN2-	AN	Comparator Negative Input

P56	P56	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN6	AN	AIN Analog Input Channel 6
	CIN3-	AN	Comparator Negative Input
P57	P57	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN7	AN	AIN Analog Input Channel 7
	PWM7A	O	PWM7A Output
	DACVREF	O	DAC reference voltage output port
P60	P60	I/O	GPIO, programmable pull-up/pull-down, port wake-up, optional enhanced level 2 drive
	AIN8	AN	AIN analog input channel 8
	PWM1A	O	PWM1A output
	INT1A	I	External interrupt 1 input port
	LED0	O	LED driver port 0
	TX0	O	UART Transmit Port
	IIC_SDA0	O	IIC Data Port
	SPI_MOSI0	I/O	SPI Master Output, Slave Input Data Port
	(SDA0)	I	Programming Timing Port 0
P61	P61	I/O	GPIO, programmable pull-up/pull-down, port wake-up, optional enhanced level 2 drive
	AIN9	AN	AIN Analog Input Channel 9
	PWM2A	O	PWM2A Output
	LED1	O	LED Driver Port 1
	VREF	AN	ADC External Reference Voltage Input Port
	RX0	I	UART Communication Receive Port
	IIC_SCL0	O	IIC Clock Port
	SPI_SCK0	O	SPI Master Mode Clock Pin
	CMPOUT	O	Comparator Result Output Port
	(SCL0)	I	Programming Timing Port 0
P62	P62	I/O	GPIO, programmable pull-up/pull-down, port wake-up, optional enhanced level 2 drive
	AIN10	AN	AIN Analog Input Channel 10
	PWM4A	O	PWM4A Output
	LED2	O	LED Driver Port 2
	TC0	I	TC0 External Clock Input Port
	SPI_CS	I	SPI Slave Chip Select Control Port
P63	P63	I/O	GPIO, programmable pull-up/pull-down, port wake-up, optional enhanced level 2 drive
	AIN11	AN	AIN Analog Input Channel 11
	PWM5A	O	PWM5A Output
	LED3	O	LED Driver Port 3
	CIN1+	AN	Comparator Positive Input

	SPI_MISO	I/O	SPI master input, slave data output
P64	P64	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN12	AN	AIN Analog Input Channel 12
	PWM6A	O	PWM6A Output
	LED4	O	LED Driver Port 4
P65	P65	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN13	AN	AIN Analog Input Channel 13
	PWM3A	O	PWM3A Output
	INT1B	I	External interrupt 1 input port
	CIN1-	AN	Comparator Negative Input
	LED5	O	LED Driver Port 5
P66	P66	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN14	AN	AIN Analog Input Channel 14
	PWM1B	O	PWM1B Output
	CIN4-	AN	Comparator Negative Input
	LED6	O	LED Driver Port 6
P67	P67	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN15	AN	AIN Analog Input Channel 15
	PWM2B	O	PWM2B Output
	CIN5-	AN	Comparator Negative Input
	LED7	O	LED Driver Port 7
P70	P70	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN16	AN	AIN Analog Input Channel 16
P71	P71	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN17	AN	AIN Analog Input Channel 17
	VDD	--	Power Supply
	GND	--	Ground

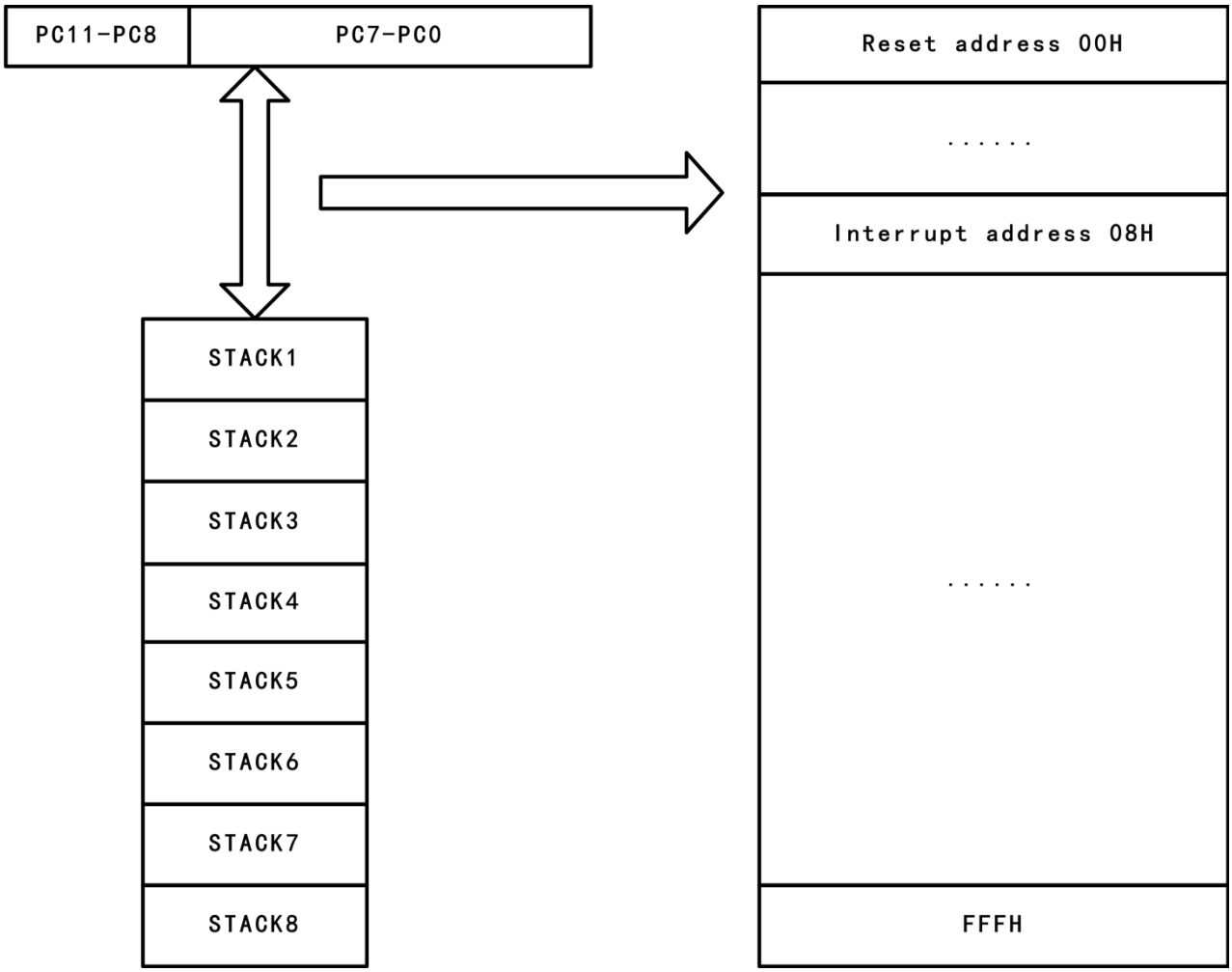
1.5 System Block Diagram



System Circuit Block Diagram

2. Central Processing Unit

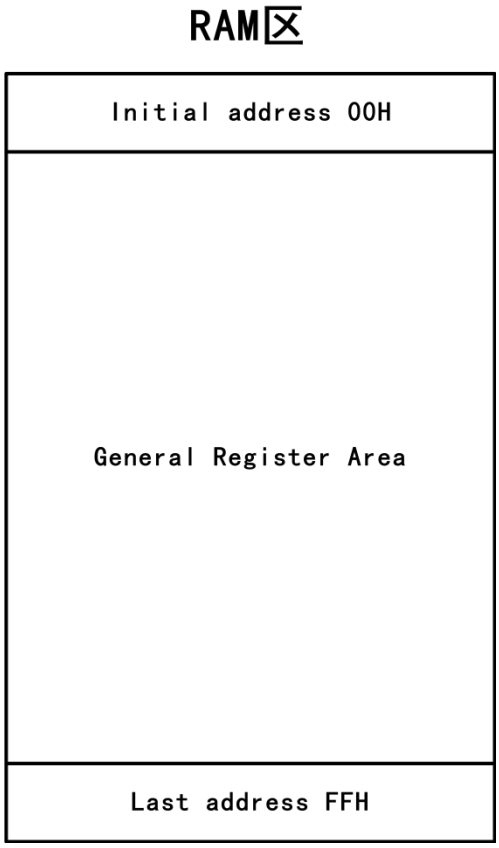
2.1 Program Storage Area Structure



Program Storage Area Structure Diagram

2.2 Data Storage Area

2.2.1 Data Storage Area Structure



Data Storage Area

2.2.2 Overview of Special Function Registers

Address	0X18_	0X19_	0X1A_	0X1B_	0X1C_	0X1D_	0X1E_	0X1F_
0	RSR	P5PH	P5AE	TC1CON	TC0CON		E2PCON	LEDRAM0
1	PCH	P6PH	P6AE	TC1PRDL	TC0C		E2PDATL	LEDRAM1
2	PCL	P7PH	P7AE	PWM1DTL	PWM7DTL		E2PDATH	LEDRAM2
3	STATUS	P5PD	ADATH	PWM2DTL	PWM7CON/DTH		SSICON0	LEDRAM3
4		P6PD	ADATL	PWM3DTL			SSICON1	LEDRAM4
5		P7PD	DACON	TC1PRDTH			I2CADDR	LEDRAM5
6	TBRDH		ADCON0	PWM21DTH		INTE0	SSIBUF	LEDRAM6
7	TBRDL		ADCON1	PWMCON1		INTE1	SSISR0	LEDRAM7
8	CPUCON			TC2CON	TC3CON		SSISR1	LEDCON0
9	IHRCCAL			TC2PRDL	TC3CL			LEDDT
A (10)	P5			PWM4DTL	TC3CH	INTF0	CMPCON0	
B(11)	P6			PWM5DTL		INTF1	CMPCON1	
C(12)	P7	P5IWE	VREFCAL	PWM6DTL				
D(13)	P5CON	P6IWE	TPRE	TC2PRDTH				
E(14)	P6CON	P7IWE	EXINTCON	PWM54DTH				
F(15)	P7CON		WDTCON	PWMCON2				IAR

2.3 Special System Registers

2.3.1 Indirect Addressing

Data memory can be addressed directly or indirectly, and indirect addressing operations can be achieved through the IAR register.

The RSR register works with the R1FF register to implement indirect addressing operations. Users can place the address corresponding to a certain SRAM into the RSR register, and then access the indirect addressing register R1FF. At this point, the address will point to the SRAM at the corresponding address in the RSR.

The IAR is not an actual register; its main function is to serve as a pointer for indirect addressing. Any instruction that uses R1FF (IAR) as a pointer actually corresponds to the data pointed to by R180 (RAM Selection Register) RSR<7:0>.

Example: Indirectly accessing RAM (0x00～0xff)

```
MOV    A,@0X00
MOV    RSR,A       // Indirect addressing pointer points to 00H
CLR    IAR         // Clear the data pointed to by the address 00H
INC    RSR         // Address +1
MOV    A,RSR
XOR    A,@0XFF
JBTS   STATUS,2
JMP    $-5         // Go back 5 instructions, continuously clearing until RSR
                       points to FFH
CLR    0XFF        // Clear the data pointed to by the address FFH
```

2.3.1.1 R180/RSR (RAM selection register)

0X180	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSR	RSR<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

RSR<7:0> is used to select the SRAM address in indirect addressing mode (addressing range: 0X00 to 0XFF).

2.3.1.2 R1FF/IAR (Indirect Addressing Register)

0X1FF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAR	IAR<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

The indirect addressing register is not a physically existing register; its main function is to serve as a pointer for indirect addressing. Any instruction using R1FF

as a pointer actually corresponds to the data in the SRAM pointed to by the R180 (RAM Selection Register) RSR<7:0>.

2.3.2 Lookup Table

2.3.2.1 Jump Table

The program counter (PC) controls the execution order of program instructions, addressing the entire ROM range. The PC increments by 1 after executing an instruction, always pointing to the address of the next instruction. When performing operations such as jumps, conditional jumps, PCL assignments, subroutine calls, interrupts, and returns, the PC automatically loads the address related to the instruction rather than the address of the next instruction.

The jump table can achieve multi-address jump functionality, obtaining a new PCL value by adding the PCL and ACC values for multi-address jumping. For example, if ACC=1, it means the current address is PCL+1. It is important to note that jumps should not exceed the allowed range to avoid functional anomalies.

Example 1: Jump table returns the value 0X4F

```
MOV    A,@0X03
ADD    PCL,A
RETL   @0X3F //0
RETL   @0X06 //1
RETL   @0X5B //2
RETL   @0X4F //3
RETL   @0X66 //4
```

Example 2: Jump to program LOOP2

```
MOV    A,@0X02
ADD    PCL,A
JMP    LOOP0  //0
JMP    LOOP1  //1
JMP    LOOP2  //2
JMP    LOOP3  //3
```

2.3.2.1.1 R181/PCH (Program Counter High Register)

0X181	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCH	-	-	-	-	PC<11:8>			
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

2.3.2.1.2 R182/PCL (Program Counter Low Register)

0X182	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCL	PC<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

The Program Counter (PC) is a pointer used to record the instructions that the CPU needs to process in each instruction cycle. During the CPU operation cycle, the PC advances the instruction pointer to the program memory, and then the pointer increments by 1 to enter the next cycle. The JZ8M4600 has a 12-bit wide Program Counter (PC), with its low byte coming from the readable and writable PCL register, and the high byte coming from the readable PCH register.

The stack is used to record the instruction pointer returned by the program. When calling a subroutine, the PC pushes the instruction pointer onto the stack. When executing the return instruction, the stack sends the instruction pointer back to the PC, allowing the original process to continue. The JZ8M4600 has an 8-level stack that occupies neither program storage space nor data storage space, and the stack pointer cannot be read or written.

The program counter (PC) and stack are detailed as follows:

(1) Both the PC register and the built-in 8-level stack are 12 bits wide, used for addressing the 4K×16Bit MTP ROM.

(2) In general, the PC increments by one; upon reset, all bits of the PC are cleared to zero.

(3) The instruction "JMP" allows direct loading of a 12-bit address, and then pushes PC+1 onto the stack. Therefore, the JMP instruction allows the PC to jump to any location in the program.

(4) The instruction "CALL" allows loading of the 12-bit address of the PC, and then pushes PC+1 onto the stack. Thus, the entry address of the subroutine can be located at any position in the program.

(5) Executing the "RET" instruction sends the top data of the stack to the PC.

(6) Executing the "ADD PCL,A" instruction adds a relative address to the current PC, incrementing the ninth bit and above of the PC subsequently.

(7) Executing the "MOV PCL,A" instruction loads an address from the "A" register into the low 8 bits of the PC, while keeping the ninth bit and above of the PC unchanged.

(8) Any instruction that writes a value to PCL (except for the "ADD PCL,A" instruction, such as "MOV PCL,A," "BTC PCL,1") will keep the ninth and tenth bits of the

PC unchanged.

(9) The operation of the stack is similar to a circular buffer; that is, after pushing onto the stack 8 times, the data pushed in during the 9th push will overwrite the data from the 1st push, and the data from the 10th push will overwrite the data from the 2nd push, and so on.

2.3.3 ROM area lookup

The TBRDH and TBRDL registers can work with the TBRD instruction to query data at the ROM area addresses. The high 8 bits of the queried data are saved to a custom register, while the low 8 bits are saved to ACC.

Example 1: The 16-bit data for the ROM address 0X00F3 is 0X339E

```
    MOV     A,@0x00
    MOV     TBRDH,A
    MOV     A,@0xF3
    MOV     TBRDL,A
    TBRD    reg_tempH       // Saves the high 8 bits to reg_tempH; the low 8 bits
                               are saved to ACC
    MOV     reg_tempL,A     // Saves the value in ACC to reg_tempL
Table:
ORG     0X00F0              // The fixed ROM program starting address is 0X00F0
    DW      0X00F3 // 0
    DW      0X1103 // 1
    DW      0X22BC // 2
    DW      0X339E // 3
    DW      0X444E // 4
```

Example 2: Unknown address, query data 0X1103 by label

```
    MOV     A,@Table/256    // High address data
    MOV     TempH,A         // Save high 8 bits of data in TempH
    MOV     A,@Table+1      // Low address data
    MOV     TempL,A         // The lower 8 bits of the data are stored in TempL
Table:
    DW      0X00F3      // 0
    DW      0X1103      // 1
    DW      0X22BC      // 2
    DW      0X339E      // 3
    DW      0X444E      // 4
```

2.3.3.1 R186/TBRDH (Table Pointer High Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	PWM4_LEDEN	PWM1_LEDEN	MTP_POWER	VDD_POWER	RBIT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<3:0>: RBIT<11:8> - High 4 bits of TBRD pointer address.(bit5/4 must be set to 1)

2.3.3.2 R187/TBRDL (Table Pointer Low Register)

0X187	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDL	RBIT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: RBIT<7:0> - TBRD pointer address lower 8 bits.

1. RBIT <7:0> is used to select the lower 8 bits of the address of the lookup ROM in the table lookup method.
2. RBIT <7:0> is used to select the EEPROM address in EEPROM read/write.

2.3.4 Status Register

2.3.4.1 R183/STATUS (Status Flag Register)

0X183	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	RST	GIE	-	T	P	Z	DC	C
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	1	1	X	X	X

Bit<7>: RST - Reset or wake-up flag
0: Other reset types
1: Wake-up triggered by pin state change
Bit<6>: GIE - Interrupt enable flag
0: Masked by DIT instruction or hardware interrupt
1: Interrupt enabled by EIT/RTI instruction
Bit<5>: Not used
Bit<4>: T - Time overflow bit
0: WDT overflow
1: Executed "SLEEP" and "CWDT" instructions or low voltage reset
Bit<3>: P-power-down flag
0: Execute the "SLEEP" command
1: Power-on reset or execute the "CWDT" command
The events that affect T/P are shown in the table below:

Type	RST	T	P
Power-on reset	0	1	1
Press RESET in working mode	0	Hold	Hold
RESET wake-up	0	1	0
WDT overflow in working mode	0	0	Hold
WDT overflow wake-up	0	0	0
Port input change wake-up	1	1	0
Execute CWDT instruction	Hold	1	1
Execute SLEEP instruction	Hold	1	0

Bit<2>: Z - Set to "1" when the result of arithmetic or logical operation is zero

0: When the result of arithmetic or logical operation is not zero

1: When the result of arithmetic or logical operation is zero

Bit<1>: DC - Auxiliary carry flag

0: No carry from the lower four bits during addition; / borrow from the lower four bits during subtraction

1: Carry from the lower four bits during addition; / no borrow from the lower four bits during subtraction

Bit<0>: C - Carry flag

0: When performing addition, no carry is generated in the high four bits; / When performing subtraction, a borrow is generated in the high four bits.

1: When performing addition, a carry is generated in the high four bits; / When performing subtraction, no borrow is generated in the high four bits.

2.3.5 Power domain

MTP and VDD provide two types of power domain selections to enhance anti-interference capabilities, allowing users to configure whether to enable enhanced anti-interference capabilities.

2.3.5.1 R186/TBRDH (Table Pointer High Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	PWM4_LEDEN	PWM1_LEDEN	MTP_POWER	VDD_POWER	RBIT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<5>: MTP_POWER - MTP power domain selection (must be set to 1)

0: High interference immunity

1: High performance

Bit<4>: VDD_POWER - VDD power domain selection (must be set to 1)

0: High interference immunity

1: High performance

3. IO ports

JZ8M4600 has 3 sets of bidirectional I/O ports, totaling 18 inputs and 18 outputs, most of which can be reused for other functions.

18 programmable pull-up I/O pins: P50～P57, P60～P67, P70～P71;

18 programmable I/O pins: P50 to P57, P60 to P67, P70 to P71;

18 optional enhanced I/O pins: P50 to P57, P60 to P67, P70 to P71;

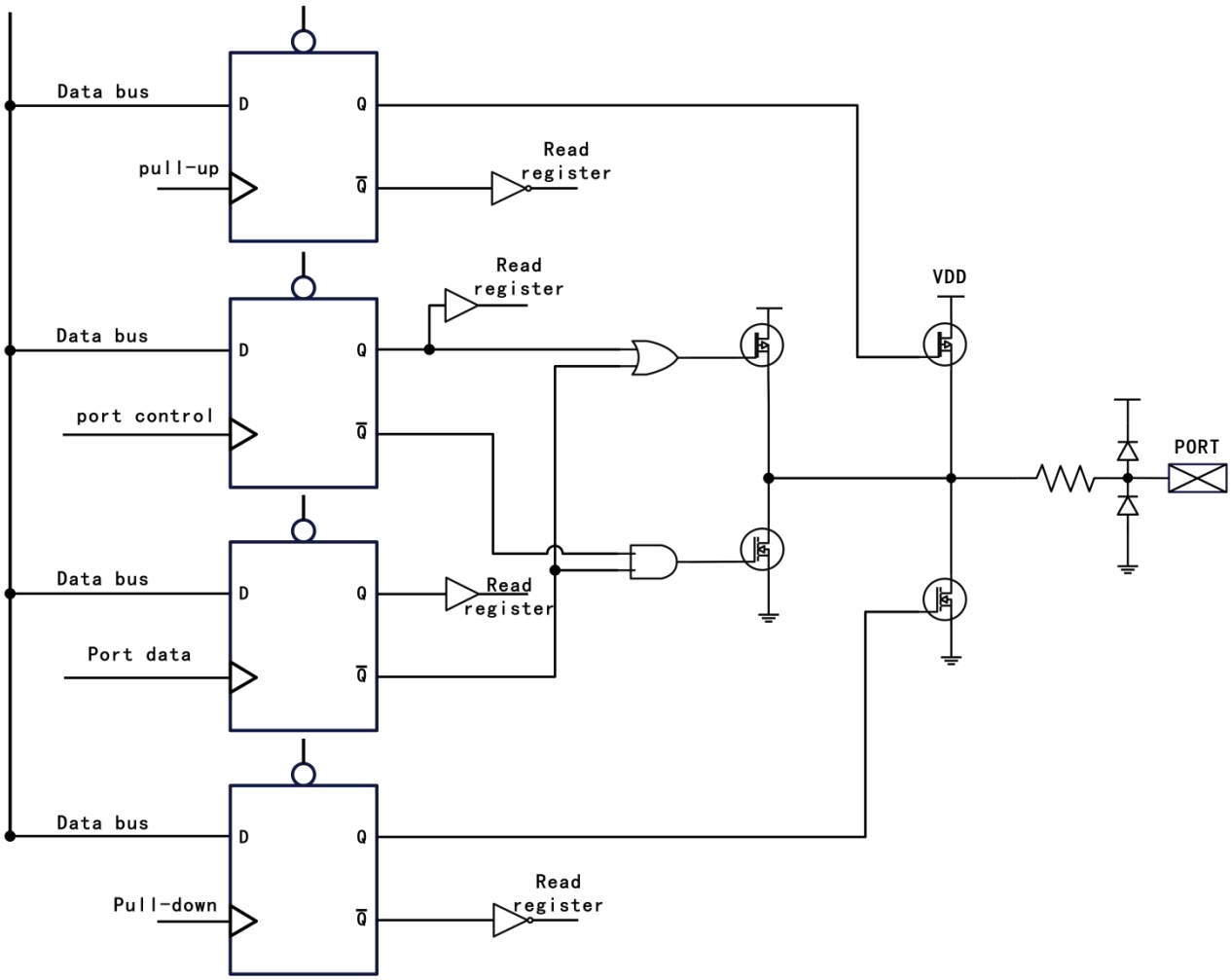
9 optional secondary enhanced I/O pins: P60 to P67, P51;

18 programmable wake-up I/O pins: P50 to P57, P60 to P67, P70 to P71;

18 programmable analog ports: P50 to P57, P60 to P67, P70 to P71;

3.1 GPIO internal structure diagram

The following internal structure diagram is for reference only and does not represent the actual circuit.



IO control register/data register/pull-up/pull-down structure circuit

3.2 P5 port

The P5 port is an 8-bit wide bidirectional port. Its corresponding direction control register is P5CON. Setting a bit in P5CON to 1 (=1) can configure the corresponding pin as an input. Clearing a bit in P5CON to 0 (=0) can configure the corresponding P5 pin as an output.

The data register corresponding to port P5 is PORT5. When the port is configured as an input, reading the PORT5 register reflects the state of the pins. When the port is configured as an output, reading the PORT5 register reflects the data of P5.

The registers associated with the P5 port include PORT5, P5CON, P5PH, P5PD, and P5IWE.

3.2.1 R18A/P5 (P5 Data Register)

0X18A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5	P5<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 Port Data Control

3.2.2 R18D/P5CON (P5 Control Register)

0X18D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5CON	P5CON<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 Port Input and Output Control Bits:

0: Output

1: Input

3.2.3 R190/P5PH (P5 Pull-Up Control Register)

0X190	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PH	P5PH<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 Port Pull-Up Control Bits:

0: Enable

1: Disable

3.2.4 R193/P5PD (P5 Pull-Down Control Register)

0X193	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PD	P5PD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port pull-down control bit:

0: Enable

1: Disable

3.2.5 R19C/P5IWE (P5 Input Change Interrupt, Wake-up Enable Register)

0X19C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5IWE	P5IWE<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 Port Input Change Wake-up Control Bit:

0: Disable

1: Enable

3.2.6 R1A0/P5AE (P5 Analog Port Enable Register)

0X1A0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5AE	P5AE<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 Port Analog Port Selection Control Bit:

0: Port set as GPIO

1: Port set as Analog Input

3.3 P6 Port

P6 is an 8-bit wide bidirectional port. The corresponding direction control register is P6CON. Setting a bit in P6CON to 1 (=1) configures the corresponding pin as an input. Clearing a bit in P6CON to 0 (=0) configures the corresponding P6 pin as an output.

The data register corresponding to P6 is PORT6. When the port is configured as an input, reading the PORT6 register reflects the status of the pins; when the port is configured as an output, reading the PORT6 register reflects the data of the P6 port.

Registers related to P6 include PORT6, P6CON, P6PH, P6PD, P6IWE, etc.

3.3.1 R18B/P6 (P6 Data Register)

0X18B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6	P6<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 Port Data Control

3.3.2 R18E/P6CON (P6 Control Register)

0X18E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6CON	P6CON<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port input/output control bits:

0: Output

1: Input

3.3.3 R191/P6PH (P6 pull-up control register)

0X191	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PH	P6PH<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port pull-up control bits:

0: Enable

1: Disable

3.3.4 R194/P6PD (P6 pull-down control register)

0X194	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PD	P6PD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port pull-down control bits:

0: Enable

1: Disable

3.3.5 R19D/P6IWE (P6 input change interrupt, wake-up enable register)

0X19D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6IWE	P6IWE <7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 port input change wake-up control bit:

0: Disable

1: Enable

3.3.6 R1A1/P6AE (P6 Analog Port Enable Register)

0X1A1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6AE	P6AE <7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 port analog selection control bit:

0: Port set as GPIO

1: Port set as Analog Input

3.4 P7 port

P7 port is a 2-bit wide bidirectional port. The corresponding direction control register is P7CON. Setting a bit in P7CON to 1 (=1) allows the corresponding pin to be configured as input. Clearing a bit in P7CON to 0 (=0) configures the corresponding P7 pin as output.

The data register corresponding to P7 port is PORT7. When the port is configured as input, reading the PORT7 register retrieves the pin's status; when configured as output, reading the PORT7 register retrieves the data from P7 port.

The registers related to the P7 port include PORT7, P7CON, P7PH, P7PD, P7IWE, etc.

3.4.1 R18C/P7(P7 Data Register)

0X18C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7	-	-	-	-	-	-	P7<1:0>	
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P7 Port Data Control

3.4.2 R18F/P7CON(P7 Control Register)

0X18F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7CON	-	-	-	-	-	-	P7CON<1:0>	
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P7 Port Input/Output Control Bits:

0: Output

1: Input

3.4.3 R192/P7PH(P7 Pull-Up Control Register)

0X192	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7PH	-	-	-	-	-	-	P7PH	
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P7 port pull-up control bits:

0: Enable

1: Disable

3.4.4 R195/P7PD (P7 pull-down control register)

0X195	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7PD	-	-	-	-	-	-	P7PD <1:0>	
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P7 port pull-down control bits:

0: Enable

1: Disable

3.4.5 R19E/P7IWE (P7 input change interrupt, wake-up enable register)

0X19E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7IWE	-	-	-	-	-	-	P7IWE <1:0>	
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P7 port input change wake-up control bits:

0: Disable

1: Enable

3.4.6 R1A2/P7AE (P7 simulation port enable register)

0X1A2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7AE	-	-	-	-	-	-	P7AE <1:0>	
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P7 port selection control bit:

0: Port set as GPIO

1: Port set as Analog Input

3.5 Port input change wake-up

JZ8M4600 includes 18 programmable port input change wake-up I/O: P50 to P57, P60 to P67, P70 to P71. The chip can enter sleep mode or idle mode by executing the "SLEEP" instruction. At this time, the CPU does not execute instructions. Port input change wake-up can continue the original process (execute DI before SLEEP) or execute the corresponding interrupt jump (execute EI before SLEEP) as selected by the program, requiring the relevant interrupt enable control to be turned on, and after the port input change wake-up, jump to the interrupt service routine.

Port status change query wake-up setting:

1. Set the port input change wake-up pin as input;
2. The internal pull-up or pull-down of the wake-up pin can be selected as needed;
3. Enable port input change wake-up control P5IWE/P6IWE/P7IWE;
4. Execute the DI instruction, do not enter the interrupt address pin;
5. Execute the "SLEEP" instruction, IDLE=0 to enter sleep mode or IDLE=1 to enter idle mode;
6. After waking up, execute the next instruction of SLEEP;

Wakeup settings for port state change interrupt mode:

1. Set the port input change wake-up pin as input;
2. The internal pull-up or pull-down of the wake-up pin can be selected as needed;
3. Enable port input change wake-up control P5IWE/P6IWE/P7IWE;
4. Enable port input change interrupts P5ICIE/P6ICIE/P7ICIE;
5. Execute the "EI" instruction, and wait to enter the interrupt address port;
6. Execute the "SLEEP" instruction, IDLE=0 to enter sleep mode or IDLE=1 to enter idle mode;
7. After waking up, it will enter the interrupt address port, and after exiting the interrupt, execute the next instruction of SLEEP;

3.6 Schmitt parameters of the port

The Schmitt characteristics of the JZ8M4600 port are shown in the table below (for reference only):

Port	SMT	
P50～P57	0.22*VDD	0.51*VDD
P60～P67	0.22*VDD	0.51*VDD
P70～P71	0.22*VDD	0.51*VDD

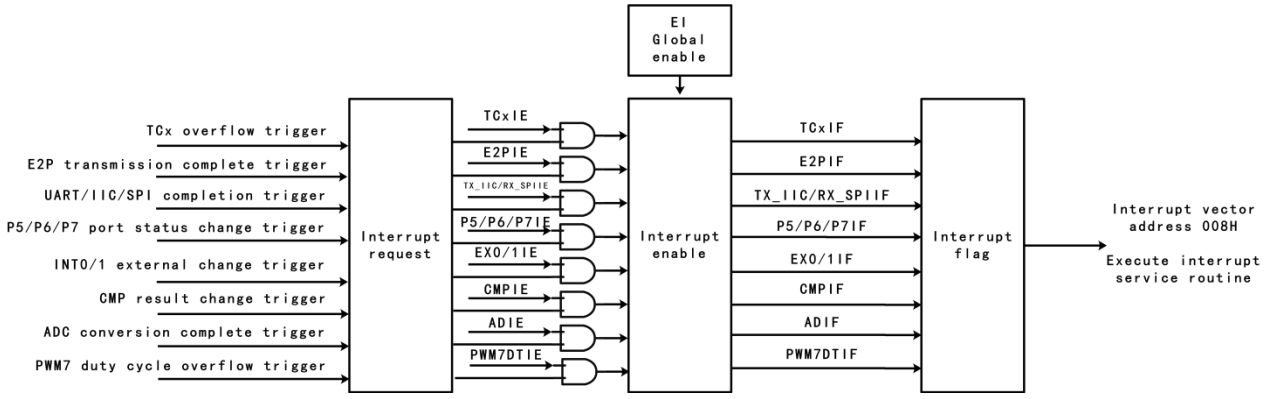
The above parameters are for reference only; please refer to the actual measured data of the target prototype.

4. Interrupt

The JZ8M4600 has 15 interrupt sources. Regardless of which interrupt is used, the global interrupt must be enabled, i.e., the "EI" instruction. The interrupt vector address is fixed at 008H. Below are the characteristics of each interrupt:

Interrupt Sources	Enabling Conditions	Interrupt Flag
TC0 Overflow Interrupt	EI + TC0IE=1	TC0IF
TC1 Overflow Interrupt	EI + TC1IE=1	TC1IF
TC2 Overflow Interrupt	EI + TC2IE=1	TC2IF
TC3 Overflow Interrupt	EI + TC3IE=1	TC3IF
E2P Write Completion Interrupt	EI + E2PIE=1	E2PIF
UART Send\IIC Completion Interrupt	EI + TX_IICIE=1	TX_IICIF
UART Receive\SPI Completion Interrupt	EI + RX_SPIIE=1	RX_SPIIF
P5 port input change interrupt	EI + P5ICIE=1	P5ICIF
P6 port input change interrupt	EI + P6ICIE=1	P6ICIF
P7 port input change interrupt	EI + P7ICIE=1	P7ICIF
INT0 external interrupt	EI + EX0IE=1	EX0IF
INT1 External Interrupt	EI + EX1IE=1	EX1IF
CMP Comparison Completion Interrupt	EI + CMPIE=1	CMPIF
ADC Conversion Completion Interrupt	EI + ADIE=1	ADIF
PWM7 Duty Cycle Overflow Interrupt	EI + PWM7DTIE=1	PWM7DTIF

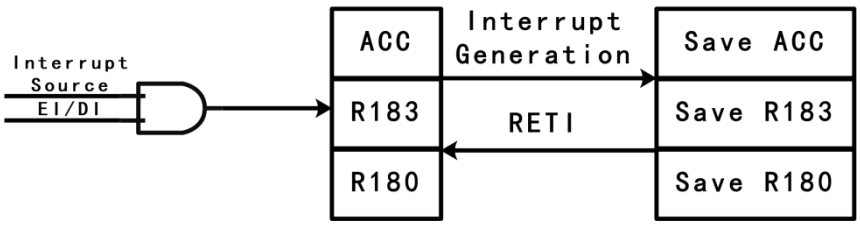
R1DA/R1DB are the interrupt flag registers, which record the interrupt flag bits after an interrupt request is generated. R1D6/R1D7 are the interrupt enable control registers, where the permission and prohibition of interrupts are set in these two registers. The overall interrupt permission is enabled by the "EI" instruction, while the overall interrupt prohibition is set by the "DI" instruction. When an interrupt occurs, the execution of the next instruction will start from the interrupt vector address 008H. Before exiting the interrupt service routine, the corresponding interrupt flag bits must be cleared to avoid erroneous interrupt actions.



Interrupt Principle Schematic

4.1 Interrupt Context Protection

During the interrupt response process, the hardware has a built-in interrupt protection feature that saves the contents of ACC, R183, and R180 until the interrupt service routine is exited. The saved values are then reloaded back to ACC, R183, and R180 to prevent changes to these values during the execution of the interrupt subroutine, which could lead to errors when returning to the main program. As shown in the figure below:



Interrupt Context Protection Schematic

4.2 Related Registers

4.2.1 R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	EXINT1MS<1:0>		EXINT0MS<1:0>		EXINT1S	EXINT0S	CAPS	INTGATE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:6>: EXINT1MS<1:0> - EXINT1 mode selection bit

EXINT1MS<1>	EXINT1MS<0>	EXINT1 mode selection
0	0	Function Disabled
0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

Bit<5:4>: EXINT0MS<1:0>- EXINT0 Mode Selection Bit

EXINT0MS<1>	EXINT0MS<0>	EXINT0 Mode Selection
0	0	Function Disabled
0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

Bit<3>: EXINT1S- EXINT1 Port Selection Bit

0: EXINT1 Port Select P60

1: EXINT1 port selects P65

Bit<2>: EXINT0S-EXINT0 port selection bit

0: EXINT0 port selects P50

1: EXINT0 port selects P54

4.2.2 R1D6/INTE0 (Interrupt Enable Control Register 0)

0X1D6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE0	PWM7DTIE	ADIE	CMPIE	EX1IE	EX0IE	P7ICIE	P6ICIE	P5ICIE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM7DTIE - PWM7 Duty Cycle Match Interrupt Enable Bit

0: Disable

1: Enable

Bit<6>: ADIE - AD Conversion Complete Interrupt Enable Bit

0: Disable

1: Enable

Bit<5>: CMPIE - CMP Comparator Result Change Interrupt Enable Bit

0: Disable

1: Enable

Bit<4>: EX1IE - EXINT1 External Interrupt Enable Bit

0: Disable

1: Enable

Bit<3>: EX0IE - EXINT0 External Interrupt Enable Bit

0: Disable

1: Enable

Bit<2>: P7ICIE - P7 Port Change Interrupt Enable Bit

0: Disable

1: Enable

Bit<1> : P6 ICIE - P6 port change interrupt enable bit

0: Disable

1: Enable

Bit<0>: P5ICIE - P5 port change interrupt enable bit

0: Disable

1: Enable

4.2.3 R1D7/INTE1 (Interrupt Enable Control Register 1)

0X1D7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE1	-	RX_SPIIE	TX_IICIE	E2PIE	TC3IE	TC2IE	TC1IE	TC0IE
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:Unused

Bit<6>:RX_SPIIE- UART Receive/SPI Transmit/SPI Receive Interrupt Enable Bit

0: Disable

1: Enable

Bit<5>:TX_IICIE- UART Transmit/IIC Transmit/IIC Receive Interrupt Enable Bit

0: Disable

1: Enable

Bit<4>:E2PIE- EEPROM Write Completion Interrupt Enable Bit

0: Disable

1: Enable

Bit<3>:TC3IE-TC3 Overflow Interrupt Enable Bit

0: Disable

1: Enable

Bit<2>:TC2IE-TC2 Period Match Interrupt Enable Bit

0: Disable

1: Enable

Bit<1>:TC1IE-TC1 Period Match Interrupt Enable Bit

0: Disable

1: Enable

Bit<0>:TC0IE- TC0 Overflow Interrupt Enable Bit

0: Disable

1: Enable

4.2.4 R1DA/INTF0 (Interrupt Flag Register 0)

0X1DA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF0	PWM7DTIF	ADIF	CMPIF	EX1IF	EX0IF	P7ICIF	P6ICIF	P5ICIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM7DTIF - PWM7 duty cycle interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<6>: ADIF - AD conversion complete interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<5>: CMPIF - CMP comparator result change interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<4>: EX1IF - EXINT1 external interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<3>: EX0IF - EXINT0 external interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<2>: P7 ICIF - P7 port change interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<1>: P6 ICIF - P6 port change interrupt enable bit

0: No interrupt triggered

1: Interrupt triggered

Bit<0>: P5 ICIF - P5 port change interrupt flag

0: No interrupt triggered

1: Interrupt triggered

4.2.5 R1DB/INTF1 (Interrupt Flag Register 1)

0X1DB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF1	-	RX_SPIIF	TX_IICIF	E2PIF	TC3IF	TC2IF	TC1IF	TC0IF
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:Unused

Bit<6> : RX_SPIIF - UART receive/SPI transmit/SPI receive interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<5> : TX_IICIF - UART transmit/IIC transmit/IIC receive interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<4> : E2PIF - EEPROM write complete interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<3> : TC3IF - TC3 overflow interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<2> : TC2IF - TC2 period match interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<1> : TC1IF - TC1 period match interrupt flag

0: No interrupt triggered

1: Interrupt triggered

Bit<0> : TC0IF - TC0 overflow interrupt flag

0: No interrupt triggered

1: Interrupt triggered

5. Reset

5.1 Overview of Reset Function

The JZ8M4600 system offers four types of reset methods:

- Power-On Reset
- RESET pin is reset by low-level input.
- WDT watchdog overflow reset.
- LVR low voltage reset.

When any of the above resets occur, all system registers are initialized to the reset values, the program halts, and the program counter PC is set to zero. After the reset, the system resumes operation from vector 0000H.

Any reset situation requires a certain response time, and the system reset mechanism ensures reliable resetting of the MCU. The time required to complete a reset varies among different types of oscillators. Therefore, the rise time of VDD and the startup time of different oscillators are not fixed. The startup time of RC oscillators is the shortest, while crystal oscillators have a longer startup time. During user terminal usage, consideration should be given to the requirements for power-on reset time based on the application scenario.

5.2 Power-On Reset

Power-on reset is closely related to LVR operation. The system power-on process follows a gradually rising curve, requiring a certain amount of time to reach normal voltage levels.

- Power-On: The system detects the rise in power supply voltage and waits for it to stabilize;
- System Initialization: All system registers are set to their initial values;
- Oscillator Starts: The oscillator begins providing the system clock;
- Execution procedure: After power up, the program begins to run;

The power-on reset time is determined by the【Reset Time】selection in the OPTION, as shown in the table below:

PWRT	Reset establishment time
PWRT=WDT/2	3.5ms (followed by the watchdog reset time/2)
PWRT=WDT/2	14ms (followed by the watchdog reset time/2)
PWRT=WDT/2	57ms (followed by the watchdog reset time/2)
PWRT=WDT/2	228ms (followed by the watchdog reset time/2)
PWRT≠WDT	350us (Independent Fixed Reset Time)

5.3 WDT Watchdog Reset

The watchdog reset is a protective setting of the system. Under normal conditions, the watchdog timer is reset by the program. If an error occurs and the system enters an unknown state, the watchdog timer will overflow, causing the system to reset. After the watchdog reset, the system restarts and enters normal conditions.

- Watchdog Timer Status: The system checks if the watchdog timer has overflowed; if it has, the system resets;
- System Initialization: All system registers are set to their default initialization values;
- Oscillator Starts: The oscillator begins providing the system clock;
- Execution procedure: After power up, the program begins to run;

Explanation of Watchdog Wakeup:

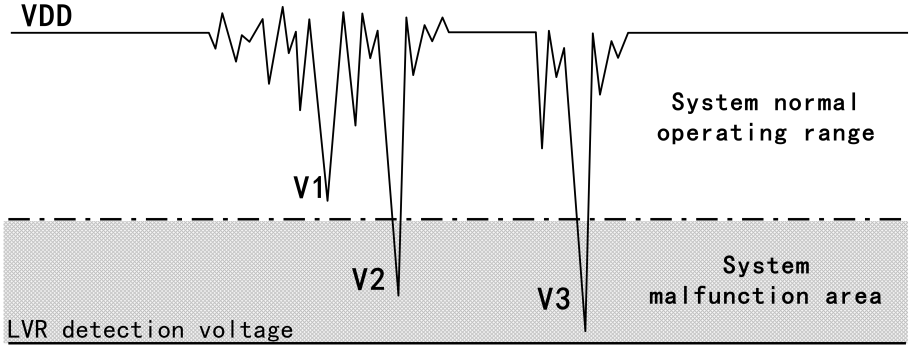
The watchdog reset can occur in idle mode and sleep mode. After the system resets, the program execution starts from address 0X00. The user can check the time overflow bit of Bit4 in the R183 (STATUS) register. If it is a WDT overflow, it can be determined as a watchdog reset, triggering the corresponding wakeup subroutine. Note that watchdog wakeup is essentially a special application of watchdog reset.

Watchdog Timer Application Considerations:

- Before resetting the watchdog, checking the status of I/O ports and RAM can enhance program reliability;
- The watchdog should not be reset within an interrupt, as this would prevent detection of the main program running out of control;
- The action of resetting the watchdog should only occur once in the main program. This architecture maximizes the protective function of the watchdog.

5.4 LVR low voltage reset.

Power-on reset targets situations where system voltage drops due to external factors (e.g., interference or changes in external load), as power loss may cause the system to operate abnormally or execute programs incorrectly.



Voltage drops may lead the system into a dead zone. The dead zone means that the power supply cannot meet the minimum operating voltage requirement of the system. The diagram above shows a typical power-on reset schematic. In the figure, VDD is severely disturbed, and the voltage drops very low. The area above the dotted line indicates normal system operation, while the area below the dotted line signifies that the system enters an unknown operating state, referred to as the dead zone. When VDD decreases to V1, the system remains in a normal state; however, when VDD drops to V2 and V3, the system enters the dead zone, making it prone to errors. The system may enter the dead zone under the following conditions:

In DC applications:

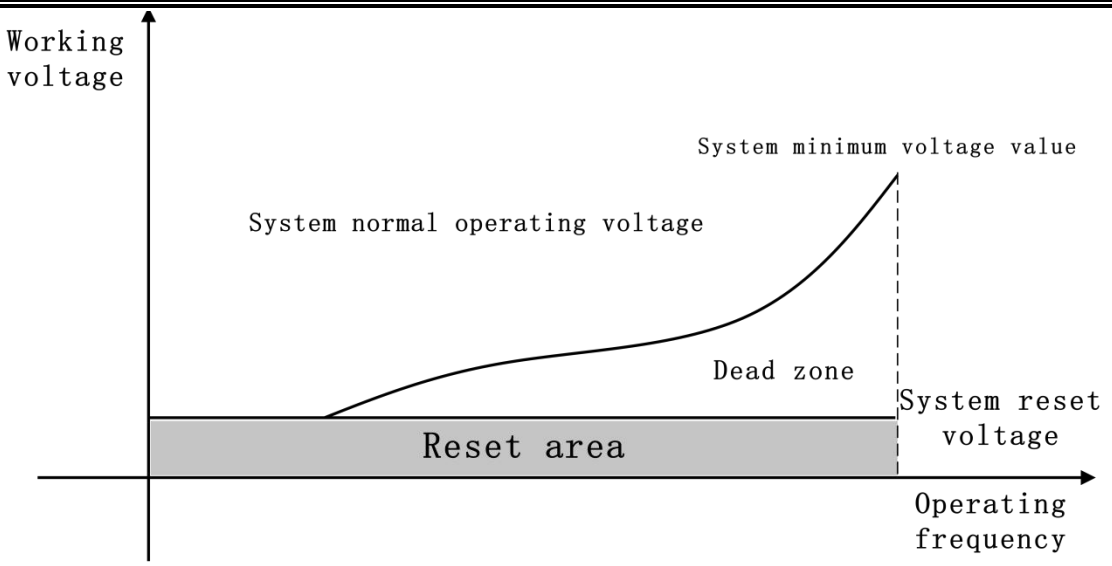
DC applications typically use battery power. When the battery voltage is too low or the microcontroller drives a load, the system voltage may drop and enter the dead zone. At this point, the power supply will not further decrease to the LVR detection voltage, causing the system to remain in the dead zone.

In AC applications:

When the system uses AC power, the DC voltage value is affected by noise in the AC power supply. When the external load is excessively high, such as when driving a motor, the interference generated by load operation also affects the DC power supply. If VDD drops below the minimum operating voltage due to interference, the system may enter an unstable working state. In AC applications, the power-up and power-down times are usually longer. During power-up, the timing protection ensures that the system powers up normally, but the power-down process is similar to that in DC applications; after the AC power is turned off, the VDD voltage slowly decreases, making it easy to enter the dead zone.

5.5 Relationship between operating frequency and LVR voltage detection

To improve the performance of the system's power-on reset, it is essential to clarify the minimum operating voltage value of the system. The system's minimum operating voltage is related to its execution speed, and the minimum operating voltage values vary at different execution speeds.



As shown in the figure above, the normal operating voltage range of the system is generally higher than the system reset voltage, while the reset voltage is determined by the low voltage detection (LVR) level. As the system execution speed increases, the system's minimum operating voltage correspondingly rises. However, since the system reset voltage is fixed, a voltage range appears between the system's minimum operating voltage and the system reset voltage, where the system cannot operate normally and will not reset. This range is known as the dead zone.

To avoid the occurrence of a dead zone voltage, it is important to choose the appropriate LVR reset voltage point when selecting the operating frequency. See the table below:

IRC frequency	Clock Division	LVR Reset Voltage Point
IRC-16MHz	2 Clocks	LVR=3.0V
IRC-8MHz	2 Clocks	LVR=2.3V
IRC-4MHz	2 Clocks	LVR=1.9V
IRC-1MHz	2 Clocks	LVR=1.8V

Note: 1. Operating frequency = instruction cycle frequency = IRC frequency / Clocks prescaler;

2. The corresponding values of this operating frequency and LVR reset voltage point are only recommended values. Users can adjust the reset voltage point as appropriate based on their specific application scenarios.

5.6 Related Registers

5.6.1 R1AF/WDTCON (WDT, Wake-up Control Register)

0X1AF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	WDTPSR<1:0>		LVREN	UARTWE	CMPWE	EXINT1WE	EXINT0WE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Bit<7>: WDTE-WDT Watchdog Enable Control

0: Disable

1: Enable

Bit<6:5>: WDTPSR<1:0>-WDT Prescaler Selection Bits:

WDTPSR<1>	WDTPSR<0>	WDT Prescaler Factor
0	0	1:4
0	1	1:8
1	0	1:16
1	1	1:32

Bit<4>: LVREN - LVR Enable Control

0: Enable

1: Disable

6. System Clock and Working Mode

The JZ8M4600 internally integrates two types of oscillators: a high-speed RC oscillator (IHRC) and a low-speed RC oscillator (ILRC). The system clock can switch between high-speed and low-speed oscillators through the R188/CPUCON register.

6.1 System Clock

6.1.1 Internal IHRC Oscillator

The JZ8M4600 has a built-in IHRC high-speed oscillator, providing a configurable IHRC frequency feature, with a default frequency of 8MHz. The IHRC frequency can be fine-tuned using the IHRCCAL register.

The IHRC oscillator contains five frequency values: 1M/4M/8M/16M/32MHz. By setting the configuration bit of OPTION, the working frequency of IHRC can be selected. Below are their corresponding relationships:

RCM	IRC frequency
1M	IHRC frequency selected as 1MHz
4M	IHRC frequency selected as 4MHz
8M	IHRC frequency selected as 8MHz
16M	IHRC frequency selected as 16MHz
32M	IHRC frequency selected as 32MHz

JZ8M4600 provides multiple frequency division options for instruction clock, which can be selected in OPTION, suitable for more occasions. As shown in the table below:

Clocks	Clock Division
2clock	Frequency division is 2 clock
4 clock	Frequency division is 4 clock
8 clock	Frequency division is 8 clock
16 clock	Frequency division is 16 clock
32 clock	Frequency division is 32 clock

6.1.2 Internal ILRC oscillator

The JZ8M4600 has a built-in ILRC low-speed oscillator, providing a stable 36KHz low-speed clock.

6.1.3 Clock Module Application Instructions

- The internal oscillator is the most commonly used oscillation mode, which can eliminate the need for external circuits;
- Due to varying external conditions, the clock frequency of different oscillation modes may have slight differences, so it should be reasonably

selected according to needs;

6.2 Operating Modes

The JZ8M4600 can operate in four different modes with different clock frequencies. These modes control the operation of the oscillator, the execution of programs, and the power consumption of analog circuits.

- High-Speed Mode: The system clock selects the internal high-speed clock while the low-speed clock operates normally;
- Low-Speed Mode: The system clock selects the internal low-speed clock, and the high-speed clock pauses operation;
- Idle Mode: The system clock operates normally, while other parts of the system enter sleep mode (TC0, TC1, TC2, TC3 can continue to operate using the system clock and wake the system). It can also be woken up through P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, ADCWE, CMPWE, and UARTWE;
- Sleep Mode: All functions pause operation, and the system enters sleep mode, which can be awakened by TC0 (external input clock), P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, and CMPWE;

Functional Modules	High-speed mode	Low-speed mode	Idle mode	Sleep mode
IHRC	Running	Stopped	Running	Stopped
ILRC	Running	Running	Running	Stopped
CPU	Execute	Execute	Stopped	Stopped
TC0	Workable	Workable	Workable	Workable (P62 Input Clock)
TC1	Workable	Workable	Workable	Stopped
TC2	Workable	Workable	Workable	Stopped
TC3	Workable	Workable	Workable	Stopped
Interrupt	All Valid	All Valid	All Valid (TC0, TC1, TC2, TC3 Select System Clock)	TC0IE, P5ICIE, P6ICIE, P7ICIE, INT0IE, INT1IE, CMPIE
Wake-Up Function	-	-	(TC0, TC1, TC2, TC3 Select System Clock Can Wake Up) P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, ADCWE, CMPWE, UARTWE	TC0WE, P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, CMPWE
Watchdog	WDT option	WDT option	WDT option control	WDT option control

6.2.1 High-speed mode

High-speed mode is the operational mode for the system's high-speed clock, with the clock source provided by a high-speed RC oscillator. The program is executed. After a power-on reset or any reset trigger, the system enters high-speed mode to execute the program. In high-speed mode, the high-speed oscillator operates normally, with maximum power consumption.

- The program is executed, and all functions are controllable;
- The system rate is high speed;
- Both the high-speed oscillator and the internal low-speed oscillator operate normally;
- High-speed mode can switch to low-speed mode;
- Entering sleep mode from high-speed mode and returning to high-speed mode after waking up;
- Switch from high-speed mode to idle mode, and return to high-speed mode after waking up;

6.2.2 Low-speed mode

The low-speed mode is the system's low-speed clock operating mode. The system clock source is provided by a low-speed RC oscillator. The low-speed mode is controlled by the CLKMD bit in the CPU mode control register. When CLKMD=0, the system is in high-speed mode; when CLKMD=1, the system enters low-speed mode. After entering low-speed mode, the system cannot automatically disable the high-speed RC oscillator and must be disabled via SPTHX=1 to reduce power consumption.

- The program is executed, and all functions are controllable;
- The system rate is low-speed;
- The internal low-speed oscillator operates normally, while the high-speed oscillator stops working.
- The low-speed mode can switch to high-speed mode;
- Transitioning from low-speed mode to sleep mode, returning to low-speed mode after waking up;
- Transitioning from low-speed mode to idle mode, returning to low-speed mode after waking up;

6.2.3 Idle mode

Idle mode is another ideal state. In sleep mode, all functions and hardware are disabled, but in idle mode, the system clock continues to operate. The power consumption in idle mode is greater than in sleep mode. In idle mode, no program is executed, but the modules with wake-up functionality—TC0, TC1, TC2, TC3, P5IWE,

P6IWE, P7IWE, INT0WE, INT1WE, ADCWE, CMPWE, and UARTWE—continue to function normally. The clock source for timers TC0, TC1, TC2, and TC3 is the still-operating system clock. Whether to enter idle mode is determined by the IDLE bit in the system clock and status control register. When IDLE=1, executing SLEEP will enter idle mode.

- The program execution stops, and all functions are disabled;
- The modules with wake-up functionality operate normally;
- The system clock operates normally;
- Transitioning from high-speed mode to idle mode, returning to high-speed mode after waking up;
- Transitioning from low-speed mode to idle mode, returning to low-speed mode after waking up;
- The wake-up methods in idle mode are P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, ADCWE, CMPWE, UARTWE;
- The functions of TC0, TC1, TC2, and TC3 remain effective in idle mode;

6.2.4 Sleep mode

Sleep mode is the ideal state of the system where no programs are executed, and the oscillator also stops working. The power consumption of the entire chip is less than 1uA. Sleep mode can be awakened by TC0 (P62 input clock), P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, CMPWE. Transitioning from high-speed mode or low-speed mode to sleep mode will return to the corresponding mode after waking up. The ability to enter sleep mode is controlled by the system clock and the IDLE bit of the status control register. When IDLE=0, executing SLEEP will enter sleep mode.

- The program execution stops, and all functions are disabled;
- All oscillators, including the internal high-speed oscillator and the internal low-speed oscillator, stop working;
- Power consumption is less than 1uA;
- Transitioning from high-speed mode to sleep mode, returning to high-speed mode after waking up;
- Transitioning from low-speed mode to sleep mode, returning to low-speed mode after waking up;
- The wake-up methods in sleep mode are TC0 (P62 input clock), P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, CMPWE;

6.3 Related Registers

6.3.1 R188/CPUCON (CPU Mode Control Register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	ADCWE	TC3WE	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: ADCWE - ADC Wake Enable Bit

0: Wakeup Disabled

1: Wakeup Enabled, can wake up from idle mode

Bit<6>: TC3WE - TC3 Wakeup Enable Bit

0: Wakeup Disabled

1: Wakeup Enabled, can wake up from idle mode

Bit<5>: TC2WE - TC2 Wakeup Enable Bit

0: Wakeup Disabled

1: Wakeup Enabled, can wake up from idle mode

Bit<4>: TC1WE - TC1 Wakeup Enable Bit

0: Wakeup Disabled

1: Wakeup Enabled, can wake up from idle mode

Bit<3>: TC0WE - TC0 Wakeup Enable Bit

0: Wakeup Disabled

1: Wakeup Enabled, can wake up from idle mode

Bit<2>: STPHX - High-Speed Clock Control Bit

0: High-Speed Clock Operating Normally

1: Stop High-Speed Clock

Bit<1>: CLKMD - System Clock Control Bit

0: The system clock uses a high-speed oscillator (IHRC) clock

1: The system clock uses a low-speed oscillator (ILRC) clock.

When the system transitions from high-speed mode to low-speed mode, set CLKMD=1 first, then set STPHX=1.

When the system transitions from low-speed mode to high-speed mode, set STPHX=0 first, then set CLKMD=0.

Bit<0>: IDLE - Idle mode enable bit.

0: The system enters sleep mode when executing the SLEEP instruction.

1: The system enters idle mode when executing the SLEEP instruction, and the system clock operates normally.

TC0, TC3, and PWM can continue to operate in idle mode if the system clock is selected, and can wake the system.

6.3.2 R189/IHRCCAL (IHRC frequency trimming register)

0X189	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IHRCCAL	IHRCCAL<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

IHRC High-Speed Oscillator Frequency Fine Tuning

6.3.3 R1AF/WDTCON (WDT, Wake-up Control Register)

0X1AF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	WDTPSR<1:0>		LVREN	UARTWE	CMPWE	EXINT1WE	EXINT0WE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Bit<3>: UARTWE - UART Wake-up Enable Bit
0: Disable
1: Enable

Bit<2>: CMPWE - CMP Wake-up Enable Bit
0: Disable
1: Enable

Bit<1>: EX.INT1WE - EXINT1 Wake-up Enable Bit
0: Disable
1: Enable

Bit<0>: EX.INT0WE - EXINT0 Wake-up Enable Bit
0: Disable
1: Enable

7. Timer Counter

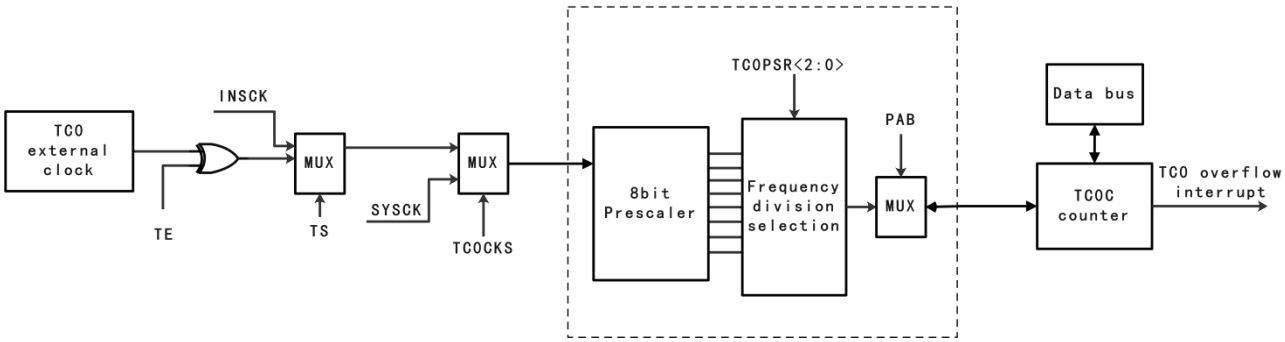
7.1 TC0 Timer Counter

JZ8M4600 provides an 8-bit timer counter as the TC0 prescaler, where the PAB bit of the TC0CON register determines whether to enable the prescaler, and TC0PSR<2:0> three bits determine the prescale ratio.

TC0 is an 8-bit up-counter that operates as long as there is a clock. The clock source can be an internal instruction clock, system clock, or low-speed clock, or an external clock (input from pin P62, with selectable trigger edge), and each clock pulse increments the counter.

TC0 counter overflow can generate an interrupt signal; after overflow, the program needs to reset the initial value, otherwise counting will start from 0.

In IDLE mode, the TC0 overflow interrupt can wake up the circuit, and after waking up, it can either enter the interrupt or continue executing the original program. In sleep mode, when TC0 is configured for the P62 external input clock, it can interrupt the overflow and wake up the circuit.



TC0 structure block diagram

7.1.1 TC0 timer settings explanation

1. Assign an initial value to the TC0C register TC0C;
2. Set the value of the TC0CON register (choose clock source and prescaler);
3. To use it as a counter, select the TC0 signal source as the external input signal in the TC0CON register;
4. After configuring everything, finally set TC0EN in the TC0CON register to enable the timer counter;
5. If interrupt functionality is needed, set TC0IE (Bit0) in the INTE1 register to 1 and execute the EI instruction;
6. Initialize the values again in the interrupt program to avoid counting from 0;
7. The system will automatically save ACC, STATUS, and RSR data during the interrupt service program, and the data will automatically restore after

executing the RETI instruction. Before exiting the interrupt, clear the TC0 interrupt flag;

7.1.2 TC0 timer calculation explanation

The TC0 timing function initializes the timer by writing a value to the TC0C register, allowing the timer to start counting from the initial value until it overflows and generates an interrupt.

TC0 timing calculation formula (selecting internal system clock):

$$\text{TC0 Timing duration} = (1/\text{Fosc}) \times (\text{TC0 prescaler}) \times (256 - \text{TC0 Initial value})$$

Example:

Fosc = 8 MHz, TC0 prescaler = 8, TC0 initial value = 156;

$$\text{TC0 Timing duration} = (1/8) \times (8) \times (256 - 156) = 100\ \text{us}$$

TC0 timing calculation formula (selecting external input clock):

$$\text{TC0 Timing duration} = (1/\text{External clock}) \times (\text{TC0 prescaler}) \times (256 - \text{TC0 Initial value})$$

Example:

External input clock = 1 MHz, TC0 prescaler = 4, TC0 initial value = 156;

$$\text{TC0 Timing duration} = (1/1) \times (4) \times (256 - 156) = 400\ \text{us}$$

7.1.3 TC0 idle mode wake-up description

In idle mode, system instructions stop executing, but modules and the system clock with wake-up capability operate normally while other functions are disabled.

TC0 can wake up from idle mode by setting the Bit3 of the R188/CPUCON register TC0WE to 1. With IDLE = 1 plus the SLEEP instruction, the system enters idle mode, and the TC0 timer operates normally (selecting system clock). When the TC0 timer overflows, the system is awakened. If TC0IE and EI are enabled, it enters an interrupt after being awakened; if DI is executed, it will execute the next instruction after waking up.

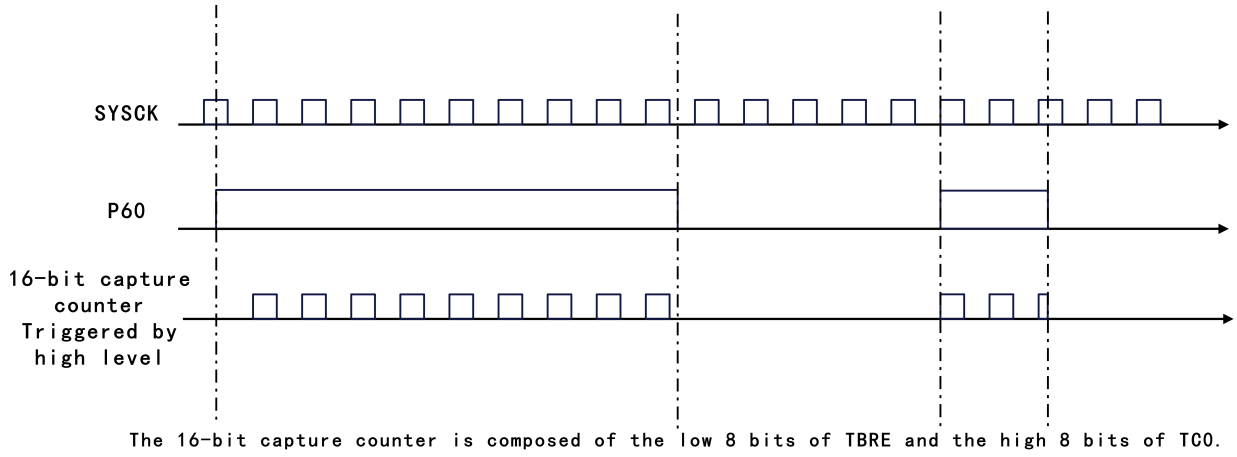
When the clock source selects the P62 external clock, enabling TC0WE = 1 and directly executing the SLEEP command can also wake up the system.

7.1.4 Port Level Capture

JZ8M4600 provides external port level capture functionality, with the captured signal source selectable through the EXINTCON (1AE) register for any external port P60, P65, P50, or P54. The capture mode is enabled via Bit0 of the EXINTCON register, INTGATE. The 8-bit prescaler TPRE (low 8 bits of the level capture counter) and the

8-bit counter TC0C (high 8 bits of the level capture counter) are multiplexed together to form a 16-bit level capture counter, coupled with external interrupts to achieve level change-triggered interrupts, where the interrupt routine checks the capture time of the previous level. If the signal period is long, attention should be paid to the potential overflow issue of the timer counter, adjusting the timer's operating mode and prescaler value accordingly to match the signal characteristics.

Users can trigger interrupts on the falling edge of the external interrupt pin and read the count values of the 0x1C1/TC0C and 0x1AD/TPRE registers in the interrupt routine to calculate the high level time. When the external interrupt pin is high, the TC0 prescaler and counter start counting, while the TC0 stops counting when the external interrupt pin is low. To capture the low level time, the triggering should be set to the rising edge, counting during the low level and stopping during the high level.



7.1.5 TC0 Related Registers

7.1.5.1 R1AD/TPRE (TC0 Prescaler)

0X1AD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TPRE	TPRE<7:0>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

7.1.5.2 R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	EXINT1MS<1:0>		EXINT0MS<1:0>		EXINT1S	EXINT0S	CAPS	INTGATE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:6>: EXINT1MS<1:0> - EXINT1 mode selection bit

EXINT1MS<1>	EXINT1MS<0>	EXINT1 mode selection
0	0	Function Disabled
0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

Bit<5:4>: EXINT0MS<1:0>- EXINT0 Mode Selection Bit

EXINT0MS<1>	EXINT0MS<0>	EXINT0 Mode Selection
0	0	Function Disabled
0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

Bit<3>: EXINT1S- EXINT1 Port Selection Bit

0: EXINT1 Port Select P60

1: EXINT1 port selects P65

Bit<2>: EXINT0S-EXINT0 port selection bit

0: EXINT0 port selects P50

1: EXINT0 port selects P54

Bit<1>: CAPS - Capture input source selection bit (CAPS is invalid when CMPGATE=1)

0: EXINT0

1: EXINT1

Bit<0>: INTGATE - TC0 external port capture gate enable bit

0: Disable

1: Enable

7.1.5.3 R1C0/TC0CON (TC0 Control Register)

0X1C0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CON	TC0EN	TC0CKS<1:0>		TC0EDG	TC0PTEN	TC0PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC0EN - TC0 Timer Counting Enable Bit

0: Disable TC0

1: Enable TC0

Bit<6:5>: TC0CKS<1:0>-TC0 signal source selection bit

00: Instruction Clock

01: External Input Signal (P62)

10: System Clock

11: ILRC Clock (Low-Speed Oscillator)

Bit<4>: TC0EDG – TC0 Signal Edge Selection Bit

0: TC0 Pin Signal Changes from High to Low Increment by 1

1: TC0 Pin Signal Changes from Low to High Increment by 1

Bit<3>: TC0PTEN – Prescaler Enable Bit

0: Disable TC0 Prescaler

1: Enable TC0 Prescaler

Bit<2:0>: TC0PSR<2:0> – TC0 Prescaler Selection Control Bits:

TC0PSR<2>	TC0PSR<1>	TC0PSR<0>	TC0 Prescaler Coefficient
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

7.1.5.4 R1C1/TC0C (TC0 Counter Register)

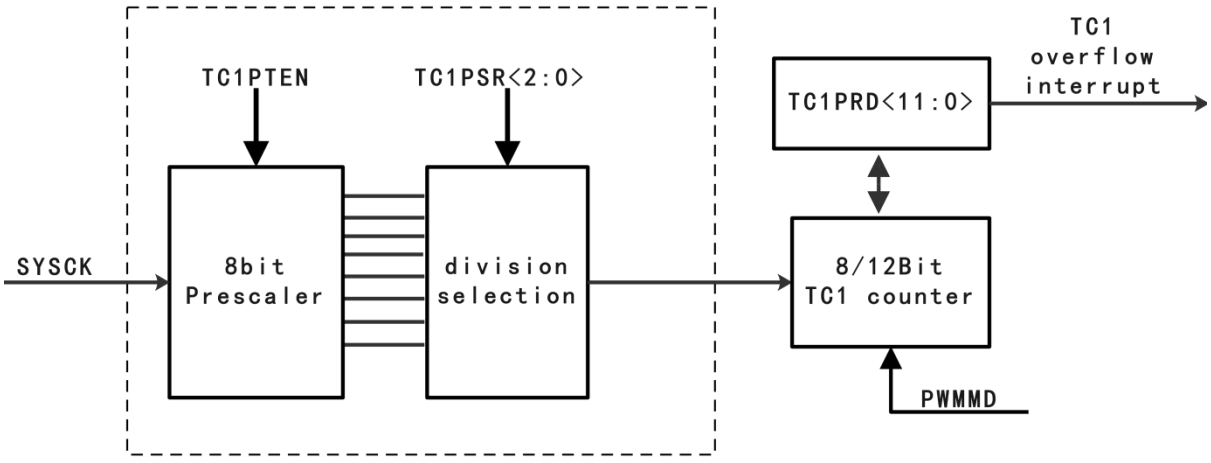
0X1C1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0C	TC0C<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.2 TC1 Timer Counter

TC1 Timer Counter provides an 8-bit prescaler, where the three bits TC1PSR<2:0> in the TC1CON register determine the prescaling ratio. In TC1 mode, each time TC1EN is enabled, the prescaler register is reset.

TC1 is a 12-bit up counter. The TC1 timer requires TC1EN to be enabled to operate, with the clock source being the internal system clock. The counter increments by 1 with every clock cycle. When the TC1 count value matches the TC1PRD set value, an overflow occurs. If TC1IE and EI are enabled, the system jumps to the corresponding interrupt vector address and executes the interrupt service routine.

In IDLE mode, the TC1 interrupt can wake up the circuit. After waking up, it can either enter the interrupt or continue executing the original program, with the method referring to port input changes for waking up.



TC1 Block Diagram

7.2.1 TC1 Timer Configuration Instructions

1. Assign an initial value to the TC1PRD<11:0> register;
2. Set the TC1CON register, configuring the prescaling ratio as needed;
3. Enable interrupt in TC1IE of the R1D7/INTE1 register, and execute the EI instruction;
4. Enable TC1EN to start counting the TC1 timer;
5. The system interrupt service routine will automatically save ACC, STATUS, and RSR data. After executing the RETI instruction, the data will be automatically restored, and the TC1 interrupt flag must be cleared before exiting the interrupt;

7.2.2 TC1 Timer Calculation Description

The TC1 timing function works by writing a value to TC1PRD<11:0>. The timer starts counting from an initial value of 0x01 until the timer count matches the TC1PRD<11:0>

value, then it overflows and executes the interrupt service routine.

TC1 Timing Calculation Formula:

$$\text{TC1 Timing duration} = (1/\text{Fosc}) \times (\text{TC1 prescaler}) \times (\text{TC1PRD})$$

Example:

Fosc = 16 MHz, TC1 prescaler = 16, TC1PRD value = 500;

$$\text{TC1 Timing duration} = (1/16) \times (16) \times （500） = 500\text{us}$$

7.2.3 TC1 Idle Mode Wake-Up Description

TC1 can wake up from idle mode by enabling Bit 4 of the R188/CPUCON register, TC1WE. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC1 timer works normally. After the TC1 timer overflows, the system is woken up. If TC1IE and EI are enabled, it will enter an interrupt upon waking. If DI is executed, it will proceed to the next instruction after waking.

7.2.4 TC1 Related Registers

7.2.4.1 R1B0/TC1CON (TC1 Control Register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GATE	TC1CKS	TC1PTEN	TC1PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC1EN - TC1/PWM123 Counter Enable Control

0: Disable

1: Enable

Bit<6>: TC21EN - TC1/PWM123 and TC2/PWM4567 Counter Enable Control Bit

0: Disable

1: Enable

Bit<5>: PWM1GATE - PWM1 Gate Output Enable Control Bit

0: No Restrictions

1: The PWM1 output is controlled by the comparator result. When CMPOUT=0, a PWM waveform is output. When CMPOUT=1, PWM1 remains at a low level.

Bit<4>: TC1CKS - TC1 Clock Selection

0: System Clock (the system clock is 32M, at a 1 division rate, the minimum operating voltage is 2.2V)

1: Low-Speed Clock

Bit<3:0>: TC1PTEN, TC1PSR2~TC1PSR0 Frequency Division Coefficient Selection:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	TC1 Frequency Division Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

7.2.4.2 R1B1/TC1PRDL(TC1 Timing Counter Lower 8-bit Register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.2.4.3 R1B5/TC1PRDTH (TC1 Timer High 4 Bits)

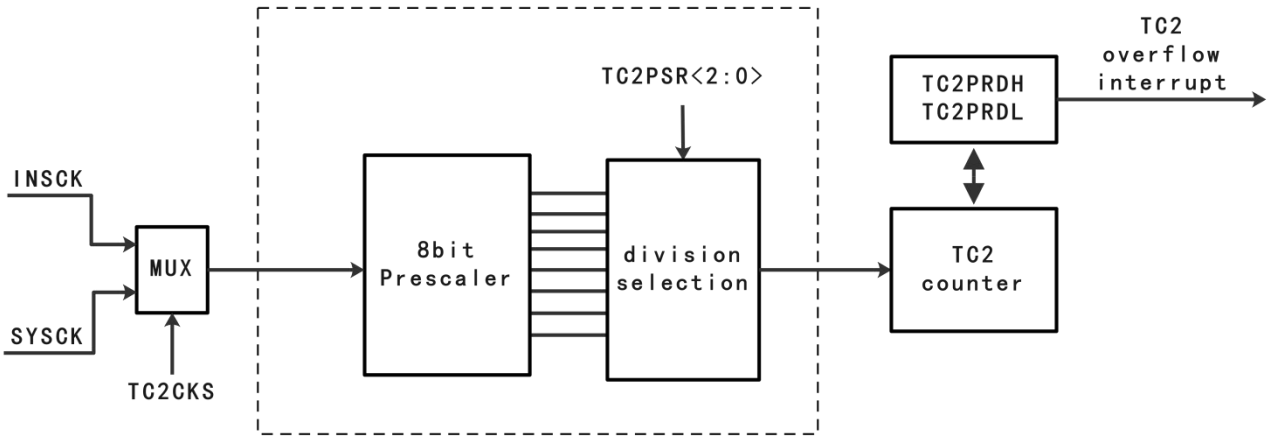
0X1B5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<11:8>				PWM3DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.3 TC2 Timer Counter

TC2 Timer Counter provides an 8-bit pre-scaler, with the three bits TC2PSR<2:0> in the TC2CON register determining the pre-scaling ratio. In TC2 mode, the pre-scaler register is cleared each time TC2EN is enabled.

TC2 is a 12-bit up counter. The TC2 timer must have TC2EN enabled to operate, with the clock source being the internal system clock. With each clock cycle, the counter increments by 1. The TC2 count value generates an overflow when it matches the TC2PRD set value, and if TC2IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service routine.

In IDLE mode, the TC2 interrupt can wake the circuit. After waking, it can either enter into the interrupt or continue executing the original program, using methods similar to port input changes for awakening.



TC2 Structure Block Diagram

7.3.1 TC2 Timer Setting Instructions

1. Assign initial values to the TC2PRD<11:0> register;
2. Set the TC2CON register, configuring the prescaler as needed;
3. Enable the TC2IE interrupt by setting the R1D7/INTE1 register and execute the EI instruction;
4. Enable TC2EN to start TC2 timer counting;
5. The system will automatically save ACC, STATUS, and RSR data in the interrupt service routine, and after executing the RETI instruction, the data will be restored automatically. Before exiting the interrupt, clear the TC2 interrupt flag;

7.3.2 TC2 Timer Calculation Instructions

The TC2 timing function operates by writing values to TC2PRD<11:0>. The timer starts counting from the initial value 0x01 until the timer count matches the TC2PRD<11:0> value, at which point it overflows and executes the interrupt service

routine.

TC2 timing calculation formula:

$$\text{TC2 Timing duration} = (1/\text{Fosc}) \times (\text{TC2 prescaler}) \times (\text{TC2PRD})$$

Example:

Fosc = 16 MHz, TC2 prescaler selection = 16, TC2PRD value = 500;

$$\text{TC2 Timing duration} = (1/16) \times (16) \times （500） = 500\text{us}$$

7.3.3 TC2 Idle Mode Wake-Up Instructions

TC2 can wake up from idle mode by enabling bit 5 (TC2WE) of the R188/CPUCON register. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode while the TC2 timer operates normally. After the TC2 timer overflows, the system is awakened. If TC2IE and EI are enabled, it will enter an interrupt after waking up; if DI is executed, it will proceed to the next instruction after waking up.

7.3.4 TC2 Related Registers

7.3.4.1 R1B8/TC2CON (TC2 Control Register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC2EN-TC2/PWM4567 counter enable control

0: Disable

1: Enable

Bit<6>: PWM4GATE<1>-PWM4 gate output enable control bit 1

0: No Restrictions

1: PWM4 output is controlled by external interrupt EXINT0. When EXINT0=1, PWM is output; otherwise, low level is output

Bit<5>: PWM4GATE<0>-PWM4 gate output enable control bit 0

0: No Restrictions

1: PWM4 output is controlled by comparator result. When CMPOUT=0, PWM is output; otherwise, low level is output

Bit<4>: TC2CKS-TC2 clock selection

0: System clock (system clock is 32M, 1 division, the minimum operating voltage is 3.3V)

1: Low-Speed Clock

Bit<3:0>: TC2PTEN, TC2PSR2～TC2PSR0 prescale factor selection:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 frequency division coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

7.3.4.2 R1B9/TC2PRDL (TC2 timer counter low 8-bit register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.3.4.3 R1BD/TC2PRDTH (TC2 timer counter high 4 bits)

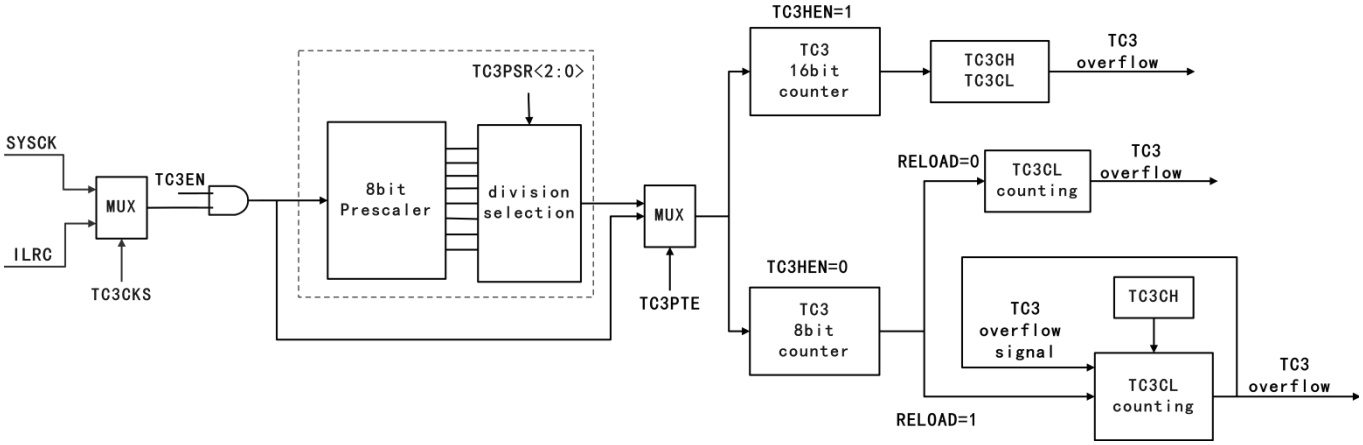
0X1BD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD <11:8>				PWM6DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.4 TC3 timer counter

TC3 timer counter provides an 8-bit prescaler, with the three bits TC3PSR<2:0> in the TC3CON register determining the prescale ratio.

TC3 is an 8/16 Bit up-counter controlled by the TC3HEN high byte counter select bit. When the 8-bit counter function is selected, the high byte TC3CH does not operate, and only the low byte TC3CL counts. When RELOAD is enabled, choosing TC3 as an 8-bit reloadable counter means that the TC3CH register acts as the preload register, and at this point, TC3HEN is set to 0. The TC3 timer requires TC3EN to be enabled to operate, with the clock source being either the internal system clock or the low-speed clock. With each clock cycle, the counter increments by 1. When the count value reaches the maximum, an overflow occurs, and if TC3IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service routine.

In IDLE mode, the TC3 interrupt can wake up the circuit, and after waking up, it can either enter an interrupt or continue executing the original program, using methods similar to how a port input change wakes it up.



TC3 Structure Block Diagram

7.4.1 TC3 Timer Configuration Instructions

1. Set initial values for the TC3C registers TC3CL and TC3CH;
2. Configure the TC3CON register value (select clock source and prescaler); set TC3HEN=0 to choose TC3 as an 8-bit counter function, and set TC3HEN=1 to choose TC3 as a 16-bit counter function;
3. If TC3 is selected as an 8-bit reloadable counter, set the TC3CON register RELOAD=1 and set the TC3CH register as the preload register, with TC3HEN set to 0; if it is a 16-bit counter, it requires reinitialization after an overflow;
4. After all configurations are set, finally set TC3EN in the TC3CON register to enable the timer counter;

5. If interrupt functionality is required, TC3IE (Bit3) in the INTE1 register must be set to 1, and the EI instruction must be executed;
6. The system executing the interrupt service routine will automatically save ACC, STATUS, and RSR data. After executing the RETI instruction, the data will automatically restore, and before exiting the interrupt, the TC3 interrupt flag must be cleared;

7.4.2 TC3 Timing Calculation Instructions

The TC3 timing function works by writing values to the TC3CL and TC3CH registers. The timer increments from the initial value until it overflows and generates an interrupt.

TC3 timing calculation formula (8-bit counter mode):

$$\text{TC3 Timing duration} = (1/\text{Fosc}) \times (\text{TC3 prescaler}) \times (256 - \text{TC3 } \textit{Initial value})$$

Example:

Fosc=16MHz, TC3 prescaler selection=8 prescaler, TC3 initial value=6;

$$\text{TC3 Timing duration} = (1/16) \times (8) \times (256 - 6) = 125\ \text{us}$$

TC3 timing calculation formula (16-bit counter mode):

$$\text{TC3 Timing duration} = (1/\text{Fosc}) \times (\text{TC3 prescaler}) \times (65536 - \text{TC3 Initial value})$$

Example:

Fosc=16MHz, TC3 prescaler selection=8 prescaler, TC3 initial value=63936;

$$\text{TC3 Timing duration} = (1/16) \times (8) \times (65536 - 63936) = 800\text{us}$$

7.4.3 TC3 idle mode wake-up description

The TC3 can wake up from idle mode by enabling Bit6 (TC3WE) of the R188/CPUCON register, selecting the TC3 clock source as the system clock. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC3 timer operates normally. When the TC3 timer overflows, the system wakes up. If TC3IE and EI are enabled, it enters an interrupt upon waking; if DI is executed, it proceeds to the next instruction after waking.

When the clock source is selected as ILRC and TC3WE = 1 is enabled, executing the SLEEP instruction can also wake up the system.

7.4.4 TC3 related registers

7.4.4.1 R1C8/TC3CON (TC3 Control Register)

0X1C8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC3CON	TC3EN	TC3CKS	RELOAD	TC3HEN	TC3PTEN	TC3PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC3EN - TC3 Timer Counting Enable Bit

0: Disable TC3

1: Enable TC3

Bit<6>: TC3CKS - TC3 clock source selection bit

0: System Clock

1: Low-Speed Clock

Bit < 5 >: RELOAD - TC3 Reload Mode Selection Bit

0: TC3 is an 8/16 bits counter, with no reload function

1: TC3 is an 8 bits reloadable counter, TC3CH register is the reload value register, keeping TC3HEN=0

Bit < 4 >: TC3HEN - TC3 High 8-bit Counter Selection Bit

0: TC3 is an 8 bits counter

1: TC3 is a 16 bits counter

Bit<3>: TC3PTEN - Pre-divider Enable Bit

0: Disable TC3 pre-divider

1: Enable TC3 pre-divider

Bit<2:0>: TC3PSR<2:0> - TC3 Prescaler Selection Control Bit:

TC3PSR<2>	TC3PSR<1>	TC3PSR<0>	TC3 Prescaler Coefficient
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

7.4.4.2 R1C9/TC3CL (TC3 Low 8-bit Count Register)

0X1C9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC3CL	TC3C<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.4.4.3 R1CA/TC3CH (TC3 High 8-bit Count Register)

0X1CA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC3CH	TC3C<15:8>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

8. PWM Pulse Width Modulation

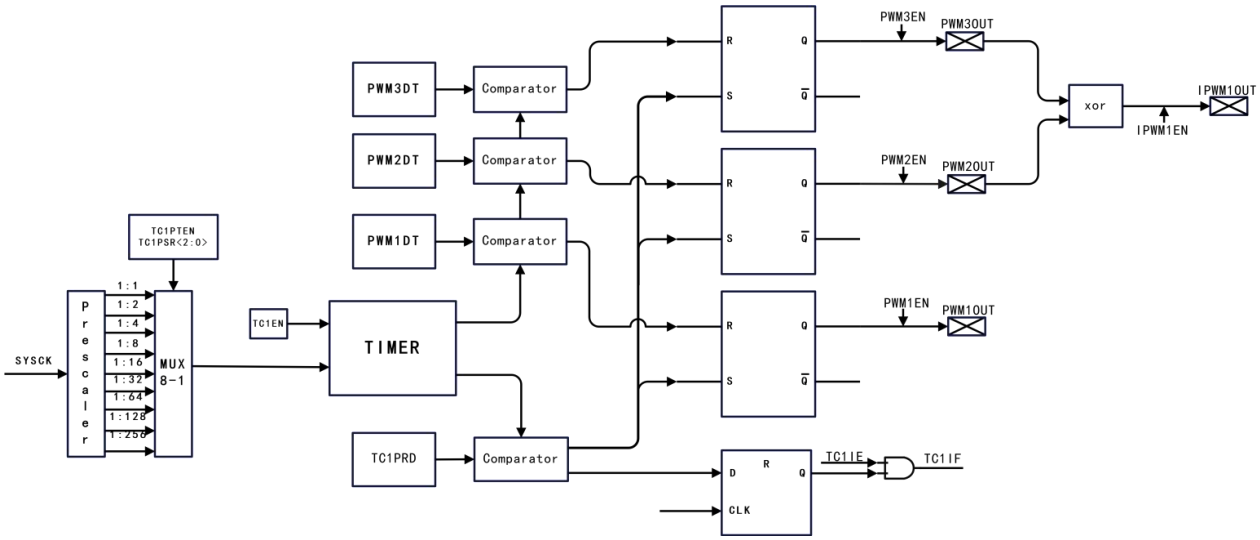
The JZ8M4600 provides two groups of 12-bit TC1 and TC2 counters. The two groups of counters can be divided into a total of seven PWM channels. PWM1-3 reuse the TC1 counter, and PWM4-7 reuse the TC2 counter to generate pulse width modulation signals. The PWM output waveform is determined by the period and duty cycle, with a transmission rate equal to the reciprocal of the period. The chip provides dead-time complementary output, where PWM2 and PWM3 are XORed to form IPWM1, with PWM1 serving as the dead-time complementary signal. (IPWM4 is the same as IPWM1)

PWM includes a period overflow interrupt, which can be enabled to trigger an interrupt.

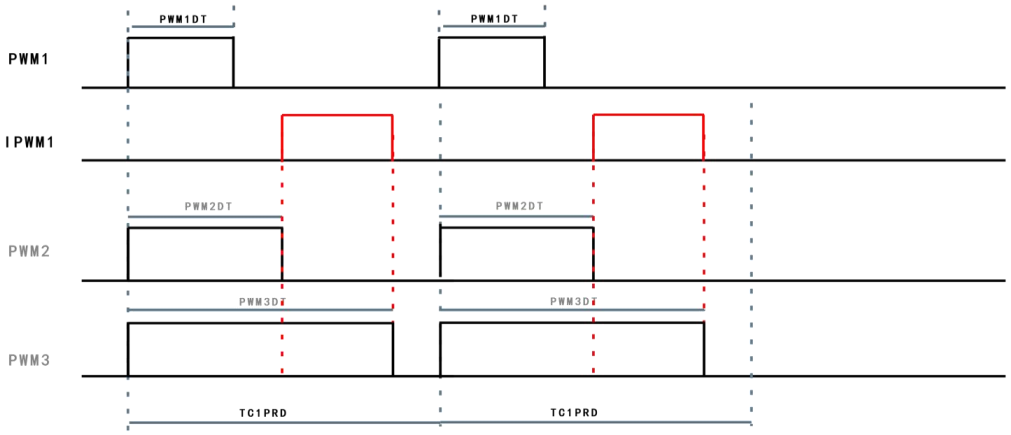
In IDLE mode, the TC1 and TC2 enable selections TC1WE and TC2WE, which can wake the system.

8.1 PWM Internal Structure and Timing

The following internal structure diagram is for reference only and does not represent the actual circuit.



PWM Working Structure Circuit



Timing Description of 3-way Common Period PWM and IPWM

8.2 PWM Period and Duty Cycle

PWM provides a 12-bit clock counter with an 8-bit programmable prescaler, serving as the baud rate clock generator for the PWM module. The counter function can be enabled by setting the TCxEN bit in the PWM control register. The counter's prescaler can be set using control bits TCxPSR<2:0>. PWMxE and IPWMxE enable the PWM function and PWM complementary function, respectively.

The PWM period is written to the TCxPRDL (lower 8 bits) and TCxPRDTH (upper 4 bits) period registers. When the counter value equals the PRD value, the following events occur at the next increment period:

- Reset the counter;
- Set the corresponding PWM output pin to high;
- Generate a PWM period overflow interrupt (if enabled);
- The PWM duty cycle is latched from the PWMxDTL/TCxPRDTH register to the DT/TIMER compare register;

PWM period calculation formula:

$$\text{PWM period} = (\text{PWMxRD}) \times (1/\text{Fosc}) \times (\text{PWM } \textit{division})$$

Example:

PWMxRD=100, Fosc=16MHz, PWMCKS=1, PWM prescaler = divide by 2;

$$\text{PWM period} = (100) \times (1/16) \times (2) = 12.5 \text{ us}$$

The PWM duty cycle is written to the PWM duty cycle register. When the counter overflows and resets to zero, the value of PWMxDT is latched to the DT/TIMER compare register. When the value of the DT/TIMER compare register equals that of the TIMER counter, the PWM output pin is set to low. The value of PWMxDT can be written at any time, but the value of the DT/TIMER compare register is only written during period overflow:

PWM duty cycle calculation formula:

$$\text{PWM } \textbf{duty} = (\text{DT}) \times (\text{PWM_CK}) \times (\text{PWM division})$$

Example:

PWMxDT=50, Fosc=16MHz, PWMCKS=1, PWM prescaler = divide by 2;

$$\text{PWM } \textbf{duty} = (50) \times (1/16) \times (2) = 6.25 \text{ us}$$

8.3 PWM idle mode wake-up description

In idle mode, CPU instruction execution is halted, while modules with wake-up functionality and the system clock operate normally, and other functions are disabled.

PWM can wake up from idle mode by setting TC1/TC2WE wake-up enable, selecting the clock source as the system clock (SYSCK). Set the corresponding cycle or duty cycle interrupt enable, set IDLE (R188) to 1, and use the SLEEP instruction to make the system enter idle mode while the PWM timer works normally.

When the corresponding interrupt condition is met, the system is awakened. If EI is enabled, it enters the interrupt after waking up; if DI is enabled, it executes the next instruction after waking up.

8.4 PWM Comparator Gating Description

The gating function of PWM1 is controlled by the PWM1GATE of the TC1CON register. When PWM1GATE=1, the PWM1 output is controlled by the comparator result, and the PWM waveform is output when CMP_FLAG=0.

The gating function of PWM4 is controlled by PWM4GATE<1:0> of the TC2CON register. When PWM4GATE<0>=1, the PWM4 output is controlled by the comparator result, and the PWM waveform is output when CMP_FLAG=0. When PWM4GATE<1>=1, the PWM4 output is controlled by the external interrupt EXINT (P50 or P54), and the PWM waveform is output when EXINT=1.

8.5 IPWM Waveform and Buzzer Setting Description

The IPWM waveform is not directly inverted but enables IPWM1EN, outputs after XORing PWM2 and PWM3. If IPWM1EN is enabled at this time, control bits can be selected to output from P61/P67 through PWM2; enabling PWM3EN allows output selection from P55/P65 through PWM3. It also supports simultaneous output of the IPWM1 waveform from two ports.

Similarly, enabling IPWM4EN outputs after XORing PWM5 and PWM6. If PWM5EN is enabled at this time, control bits can be selected to output from P52/P63 through PWM5; enabling PWM6EN allows output selection from P50/P64 through PWM6. It also supports simultaneous output of the IPWM4 waveform from two ports.

The PWM module also includes a buzzer function. Users can enable PWM output for the buzzer through the BZXEN (R1B7, R1BF) control bits. The buzzer can select ports via PWM1S (R1B7) and PWM4S (R1BF), outputting from P60/P66 and P51/P62, respectively. It should be noted that to enable the buzzer, PWM1EN and PWM4EN must be cleared and the corresponding output ports set to output.

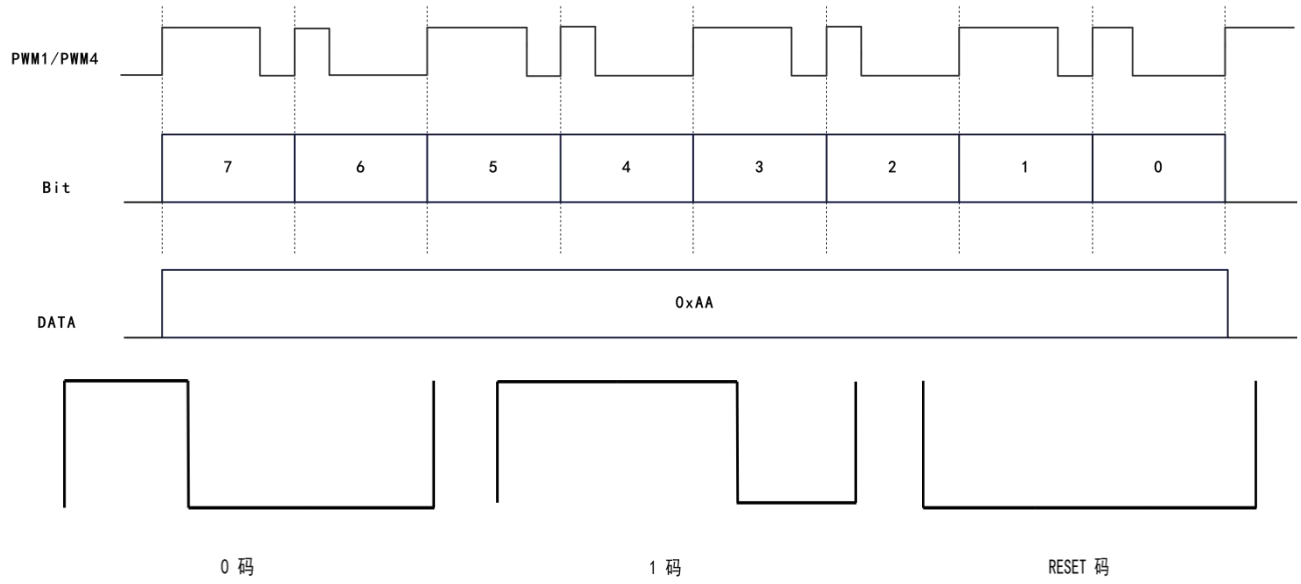
8.6 PWM7DT Interrupt and ADC Trigger Description

PWM7DT provides the function of triggering interrupts based on duty cycle. After enabling PWM7DTIE (R1D6) and executing the EI instruction, it can enter the interrupt program according to the configured PWM7 duty cycle.

PWM can be configured to enable ADC conversion triggered by the PWM7 duty cycle. By setting ADCGATE (R1A7) to 1, the ADC conversion will be triggered on the falling edge of the PWM7 duty cycle.

8.7 Single-wire cascading LED

JZ8M4600 supports two channels of single-wire cascading LED drive, outputting cascading control timing through PWM1 and PWM4 ports. The timing diagram for cascading LED drive is as follows:



Single-wire cascading LED timing explanation

PWM1 and PWM4 are two independent single-wire cascading LED drive controls. When PWM1 is used as the LED drive control, the high-level time for code 0 is set by the PWM1 duty cycle register, while the high-level time for code 1 is set by the PWM2 duty cycle register. The cycle of the code data is determined by the TC1PRD period register. After enabling PWM1_LEDEN (R186) + TC1EN, it starts sending 8-bit cascading data, which is output through the PWM1 port. After sending the 8-bit cascading data, TC1EN automatically resets to zero, and re-setting TC1EN starts sending the next 8-bit cascading data.

When using PWM4 as the LED drive control, the high-level time for code 0 is set by the PWM4 duty cycle register, while the high-level time for code 1 is set by the PWM5 duty cycle register. The cycle of the code data is determined by the TC2PRD period register. After enabling PWM4_LEDEN (R186) + TC2EN, it starts sending 8-bit cascading data, which is output through the PWM4 port. After sending the 8-bit cascading data, TC2EN automatically resets to zero, and re-setting TC2EN starts sending the next 8-bit cascading data.

8.8 PWM-related registers

8.8.1 R186/TBRDH (Table Pointer High Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	PWM4_LEDEN	PWM1_LEDEN	MTP_POWER	VDD_POWER	RBIT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM4_LEDEN - PWM4 LED cascading control bit (bit5/4 must be set to 1)

0: Disable

1: Enable

Bit<6>: PWM1_LEDEN - PWM1 LED cascading control bit

0: Disable

1: Enable

8.8.2 R1B0/TC1CON (TC1 Control Register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GATE	TC1CKS	TC1PTEN	TC1PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC1EN - TC1/PWM123 Counter Enable Control

0: Disable

1: Enable

Bit<6>: TC21EN - TC1/PWM123 and TC2/PWM4567 Counter Enable Control Bit

0: Disable

1: Enable

Bit<5>: PWM1GATE - PWM1 Gate Output Enable Control Bit

0: No Restrictions

1: The PWM1 output is controlled by the comparator result. When CMPOUT=0, a PWM waveform is output. When CMPOUT=1, PWM1 remains at a low level

Bit<4>: TC1CKS - TC1 Clock Selection

0: System Clock (the system clock is 32M, at a 1 division rate, the minimum operating voltage is 2.2V)

1: Low-Speed Clock

Bit<3:0>: TC1PTEN, TC1PSR2~TC1PSR0 Frequency Division Coefficient Selection:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	TC1 Frequency Division Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

8.8.3 R1B1/TC1PRDL(TC1/PWM123 Period Low 8-bit Register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM2, PWM3) Low 8 Bits Period

8.8.4 R1B2/PWM1DTL (PWM1 Duty Cycle Low 8 Bits Register)

0X1B2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DTL	PWM1DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM1 Duty Cycle Low 8 Bits

8.8.5 R1B3/PWM2DTL (PWM2 Duty Cycle Low 8 Bits Register)

0X1B3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2DTL	PWM2DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM2 Duty Cycle Low 8 Bits

8.8.6 R1B4/PWM3DTL (PWM3 Duty Cycle Low 8 Bits Register)

0X1B4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM3DTL	PWM3DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM3 Duty Cycle Low 8 Bits

8.8.7 R1B5/TC1PRDTH(TC1/PWM123 Period High 4 Bits and PWM3 Duty Cycle High 4 Bits Register)

0X1B5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<11:8>				PWM3DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM2, PWM3) Period High 4 Bits and PWM3 Duty Cycle High 4 Bits

8.8.8 R1B6/PWM21DTH(PWM21 Duty Cycle High 4 Bits Register)

0X1B6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM21DTH	PWM2DT<11:8>				PWM1DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM2 Duty Cycle High 4 Bits, PWM1 Duty Cycle High 4 Bits

8.8.9 R1B7/PWMCON1 (PWM Control Register 1)

0X1B7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON1	BZ1EN	PWM3S	PWM2S	PWM1S	IPWM1EN	PWM3EN	PWM2EN	PWM1EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ1EN - BZ1 waveform output enable control bit

0: Disable

1: Output BZ1 waveform (set BZ1EN=1, PWM1EN=0)

(P60/P66 must be set as output to output BZ1 waveform)

Bit<6>: PWM3S-PWM3 output selection control bit

0: PWM3 outputs from P65

1: PWM3 outputs from P55

Bit<5>: PWM2S-PWM2 output selection control bit

0: PWM2 outputs from P61

1: PWM2 outputs from P67

Bit<4>: PWM1S-PWM output selection control bit

0: PWM1 outputs from P60

1: PWM1 outputs from P66

Bit<3>: IPWM1EN-IPWM1 enable control bit

0: Disable

1: Output PWM2 and PWM3 XOR

(Select output port based on PWM2EN (P61/P67) or PWM3EN (P65/P55))

Bit<2>: PWM3EN-PWM3 enable control bit

0: Disable

1: Output PWM3 waveform enable

(The corresponding port must be set to output to output the PWM3 waveform)

Bit<1>: PWM2EN-PWM2 enable control bit

0: Disable

1: Output PWM2 waveform enable

(The corresponding port must be set to output to output the PWM2 waveform)

Bit<0>: PWM1EN-PWM1 enable control bit

0: Disable

1: Enable PWM1 waveform output

(The corresponding port must be set to output to output PWM1 waveform, and BZ1EN=0)

8.8.10 R1B8/TC2CON (TC2 Control Register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC2EN-TC2/PWM4567 counter enable control

0: Disable

1: Enable

Bit<6>: PWM4GATE<1>-PWM4 gate output enable control bit 1

0: No Restrictions

1: PWM4 output is controlled by external interrupt EXINT0. When EXINT0=1, PWM is output; otherwise, low level is output

Bit<5>: PWM4GATE<0>-PWM4 gate output enable control bit 0

0: No Restrictions

1: PWM4 output is controlled by comparator result. When CMPOUT=0, PWM is output; otherwise, low level is output

Bit<4>: TC2CKS-TC2 clock selection

0: System clock (system clock is 32M, 1 division, the minimum operating voltage is 3.3V)

1: Low-Speed Clock

Bit<3:0>: TC2PTEN, TC2PSR2～TC2PSR0 prescale factor selection:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 frequency division coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

8.8.11 R1B9/TC2PRDL (TC2/PWM4567 period low 8-bit register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 (PWM4, PWM5, PWM6, PWM7) period low 8-bit

8.8.12 R1BA/PWM4DTL (PWM4 duty cycle low 8-bit register)

0X1BA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM4DTL	PWM4DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM4 duty cycle low 8-bit

8.8.13 R1BB/PWM5DTL (PWM5 duty cycle low 8-bit register)

0X1BB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM5DTL	PWM5DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM5 duty cycle low 8 bits

8.8.14 R1BC/PWM6DTL (PWM6 duty cycle low 8 bits register)

0X1BC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM6DTL	PWM6DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM6 duty cycle low 8 bits

8.8.15 R1BD/TC2PRDTH (TC2/PWM4567 period high 4 bits and PWM6 duty cycle high 4 bits register)

0X1BD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD <11:8>				PWM6DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 (PWM4, PWM5, PWM6, PWM7) period high 4 bits and PWM6 duty cycle high 4 bits

8.8.16 R1BE/PWM54DTH (PWM54 duty cycle high 4 bits register)

0X1BE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM54DTH	PWM5DT<11:8>				PWM4DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM5 duty cycle high 4 bits, PWM4 duty cycle high 4 bits

8.8.17 R1BF/PWMCON2 (PWM Control Register 2)

0X1BF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON2	BZ2EN	PWM6S	PWM5S	PWM4S	IPWM4EN	PWM6EN	PWM5EN	PWM4EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ2EN - BZ2 waveform output enable control bit

0: Disable

1: Output BZ2 waveform (BZ2EN=1, PWM4EN=0 must be set)

(Set P51/P62 as output to enable BZ2 waveform output)

Bit<6>: PWM6S - PWM6 output selection control bit

0: PWM6 outputs from P64

1: PWM6 outputs from P50

Bit<5>: PWM5S - PWM5 output selection control bit

0: PWM5 outputs from P63

1: PWM5 outputs from P52

Bit<4>: PWM4S-PWM4 output selection control bit

0: PWM4 outputs from P62

1: PWM4 outputs from P51

Bit<3>: IPWM4EN-IPWM4 enable control bit

0: Disable

1: Output PWM5 XOR PWM6

(Select output port based on PWM5EN (P63/P52) or PWM6EN (P64/P50))

Bit<2>: PWM6EN-PWM6 enable control bit

0: Disable

1: Enable output of PWM6 waveform

(The corresponding port needs to be set as output to output PWM6 waveform)

Bit<1>: PWM5EN-PWM5 enable control bit

0: Disable

1: Enable output of PWM5 waveform

(The corresponding port must be set as output to output the PWM5 waveform)

Bit<0>: PWM4EN-PWM4 enable control bit

0: Disable

1: Enable output of PWM4 waveform

(The corresponding port must be set as output to output the PWM4 waveform, and BZ2EN=0)

8.8.18 R1C2/PWM7DTL (PWM7 duty cycle lower 8 bits register)

0X1C2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM7DTL	PWM7DTL<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

8.8.19 R1C3/PWM7CON (PWM7 control and duty cycle higher 4 bits register)

0X1C3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM7CON	CMPGATE	PWM_PULSE_EN	PWM7S	PWM7EN	PWM7DTH<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<6>: PWM_PULSE_EN—PWM7 duty cycle single trigger enable bit

0: Disable

1: Enable

Bit<5>：PWM7S-PWM7 output selection control bit

0：PWM7 output from P57

1：PWM7 output from P54

Bit<4>: PWM7EN - PWM7 enable control bit

0: Disable

1: Enable PWM7 waveform output

(The corresponding port must be set as output to enable PWM7 waveform output)

Bit<3:0>: PWM7DTH<11:8> - High four bits of PWM7 duty cycle

9. DAC digital-to-analog conversion

9.1 DACVREF voltage description

The chip has a built-in DAC module. The DAC module is enabled by setting DACON(R1A5) DACEN high. DACVREF adjusts the reference voltage output from port P57 through the VREFCAL(R1AC) register, with a voltage range from VBG (1.2V) to 4.9V (theoretical value, actual may vary). It can also select an appropriate reference sampling DAC output voltage value through the ADC module, or serve as a comparator input source for voltage comparison.

9.2 DAC related registers

9.2.1 R1A5/DACON (DAC control register)

0X1A5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DACON	DACEN	DACOUT	CMPOE	-	ADAT<11:8>			
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset Value	0	0	0	0	1	0	0	0

Bit<7>: DACEN-DAC module enable control bit

0: Disable

1: Enable

Bit<6>: DACOUT-DAC voltage output control bit

0: Output disabled

1: Output enabled

Bit<4>: Not used

9.2.2 9.2.2. R1AC/VREFCAL (VREF fine-tuning register)

0X1AC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VREFCAL	VREFCAL<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

DAC output voltage fine-tuning, data reference: Section 17.7 DAC voltage parameters

10. ADC analog-to-digital conversion

The JZ8M4600 ADC module provides a 12-bit SAR ADC, including 18 analog channels.

The ADC converter uses successive approximation analog-to-digital conversion, with results stored in R1A3/ADATH (ADC data high 8-bit register), R1A4/ADATL (ADC data low 8-bit register), and R1A5/DACON (DAC control register). The channel selection, internal/external reference voltage source, sampling clock, ADC start, and ADC enable are set through the ADCON0 and ADCON1 control registers. When switching ADC channels, be aware to introduce a certain delay (e.g., 100us) before the next conversion.

Once the AD conversion is complete, it can enter an interrupt, or the status can be checked by querying the ADRUN bit in R1A7/ADCON1.

If the AD wake-up function is enabled, the completion of the AD conversion can wake the module from sleep or idle mode.

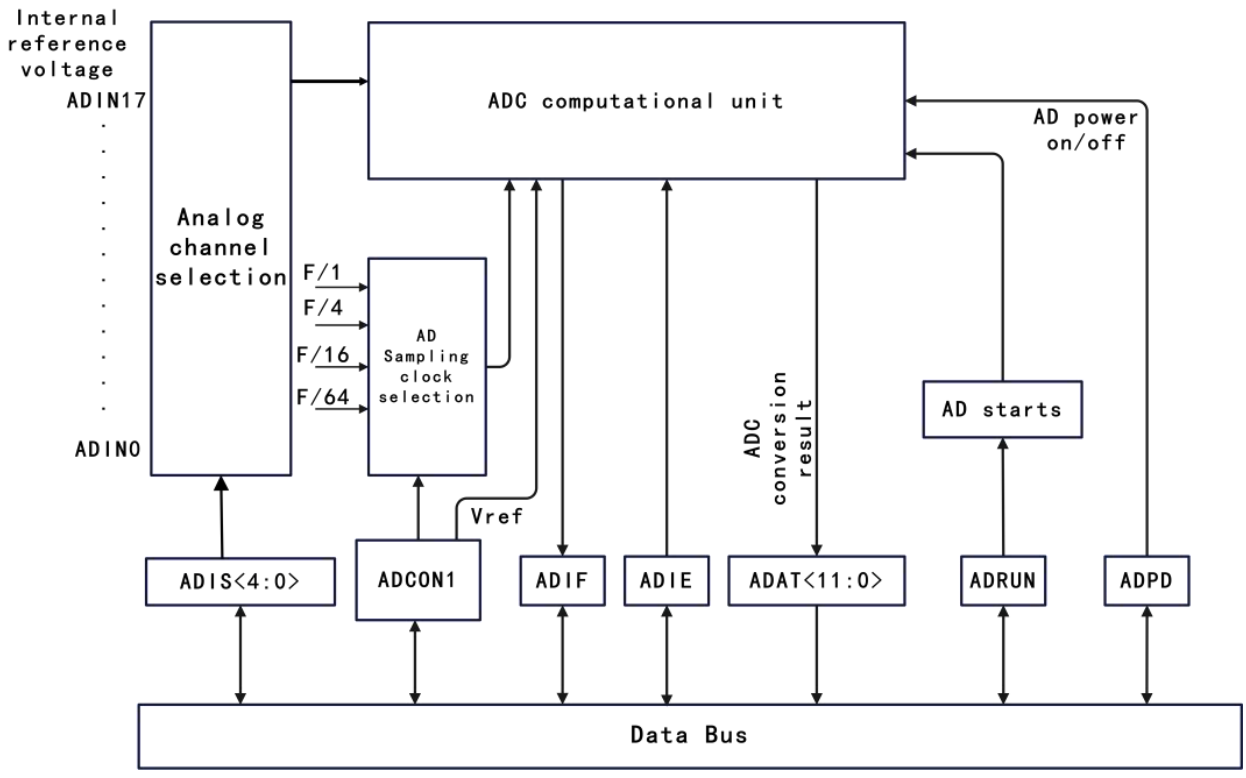


Diagram of AD conversion function

AD conversion time:

The time to convert 1 bit in AD conversion is defined as TAD, and a complete 12-bit ADC conversion requires 16 TAD cycles. It is essential to strictly adhere to TAD timing specifications to ensure normal sampling and obtain correct results. The required settings for different reference voltages and different VDD levels may vary; refer to the following table for appropriate frequency division settings.

Reference voltage/V	Operating Voltage/V	Fastest Frequency Division Setting Fosc=16MHz	Conversion Time/us
VDD	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64
4	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64
3	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64
2	4.0～5.5	Fosc/16	64
	2.7～4.0	Fosc/64	64

AD Sampling Voltage Value Calculation:

$$\text{ADC Sampling voltage} = \frac{\text{sample value}}{4096} * \text{Reference voltage}$$

Example: Reference voltage is internal reference 3V, sampling value is 0x800=2048

$$\text{ADC Sampling voltage} = \frac{2048}{4096} * 3 = 1.5\text{V}$$

10.1 ADC Power Voltage Detection Description

By configuring the ADCON0 (R1A6) register, the channel selection bits ADIS<4:0>=10010 select 1/4 VDD as the sampling channel, EXTVS selects the voltage divider source VDD, and VREF<2:0> selects the reference voltage. The conversion result can be obtained through the ADC conversion. The voltage value of VDD can be derived:

$$\text{Conversion result} = \left(\frac{\text{VDD}}{4}/\text{VREF}\right) \times 4096$$

Then

$$\text{VDD} = (\text{Conversion result}/4096) * 4 * \text{VREF}$$

10.2 P51 port detection of external 1/4 voltage instructions

The JZ8M4600 has a built-in channel for collecting 1/4 divided external voltage. A high voltage can be input from the P51 port, where the value after passing through the voltage divider should be less than the ADC reference voltage. At this time, normal sampling can occur, and the high voltage value can be derived through calculations:

$$\text{P51 Input voltage} = \frac{\text{sample value}}{4096} * \text{Reference voltage} * 4$$

Example: VDD=5V, reference voltage is the internal reference 4V, sampling value is 0x800=2048

$$\text{P51 Input voltage} = \frac{2048}{4096} * 4 * 4 = 8\text{V}$$

10.3 ADC Analog-to-Digital Conversion Setup Instructions

1. Enable ADC input ports and select analog channels by setting R1A0/P5AE, R1A1/P6AE, R1A2/P7AE, R1A6/ADCON0 registers;
2. Set ADC reference voltage and clock division by configuring R1A5/DACON, R1A7/ADCON1 registers;
3. If interrupt functionality is needed, set ADIE=1 and execute the "EI" instruction;
4. Set "ADEN=1" to start supplying power to the AD voltage;
5. Select IDLE/SLEEP mode as needed, set the AD wake-up function, ADCWE=1;
6. Set "ADRUN=1" to start AD conversion;
7. Wait for an interrupt or for ADRUN to be cleared to 0. If an AD interrupt occurs, clear ADIF to 0 when exiting the interrupt routine;
8. Save the conversion results. If multiple AD conversions are needed, jump to step 6;

10.4 ADC Related Registers

10.4.1 R1A3/ADATH (ADC Data High 8-bit Register)

0X1A3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATH	ADAT< 11:4>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	1	0	0	0	0	0	0	0

Bit<7:0>: ADAT<11:4> - AD conversion result high 8 bits

10.4.2 R1A4/ADATL (ADC Data Low 8-bit Register)

0X1A4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATL	ADAT<7:0>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: ADAT<7:0> - AD conversion result low 8 bits

10.4.3 R1A5/DACON (DAC control register)

0X1A5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DACON	DACEN	DACOUT	CMPOE	-	ADAT<11:8>			
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset Value	0	0	0	0	1	0	0	0

Bit<3:0>: ADAT<11:8> - AD conversion result high 4 bits

10.4.4 R1A6/ADCON0 (ADC Control Register 0)

0X1A6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON0	ADIS<4:0>					VCMPS	EXTVS	ADCAP
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:3>: ADIS<4:0> - AD Input Port Selection

ADIS<4>	ADIS<3>	ADIS<2>	ADIS<1>	ADIS<0>	Channel Selection
0	0	0	0	0	AIN0/P50
0	0	0	0	1	AIN1/P51
0	0	0	1	0	AIN2/P52
0	0	0	1	1	AIN3/P53
0	0	1	0	0	AIN4/P54
0	0	1	0	1	AIN5/P55
0	0	1	1	0	AIN6/P56
0	0	1	1	1	AIN7/P57
0	1	0	0	0	AIN8/P60
0	1	0	0	1	AIN9/P61
0	1	0	1	0	AIN10/P62
0	1	0	1	1	AIN11/P63
0	1	1	0	0	AIN12/P64
0	1	1	0	1	AIN13/P65
0	1	1	1	0	AIN14/P66
0	1	1	1	1	AIN15/P67
1	0	0	0	0	AIN16/P70
1	0	0	0	1	AIN17/P71
1	0	0	1	0	1/4* (VDD or P51)
1	0	0	1	1	DACVREF
1	1	1	1	1	GND

Bit<2>: VCMPS-ADC comparison voltage source selection

0: Select VREF

1: Select VDD

Note: When using a 1.2V reference, selecting VDD results in higher sampling accuracy

Bit<1>: EXTVS - sampling channel via 1/4 resistor voltage divider source selection

0: Select VDD as the 1/4 resistor voltage divider source

1: Select P51 as the 1/4 resistor voltage divider source

Bit<0>: ADCAP - ADC sampling channel capacitor selection control bit

0: Disable

1: Enable

10.4.5 R1A7/ADCON1 (ADC Control Register 1)

0X1A7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON1	ADRUN	ADEN	ADPSR<1:0>		ADCGATE	VREF<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	1

Bit<7>: ADRUN

0: ADC not sampling or sampling ended

1: ADC starts sampling

Bit<6>: ADEN

0: ADC disabled (ADC turned off in sleep mode, otherwise there will be power consumption)

1: ADC enabled

Bit<5:4>: ADPSR<1:0>-ADC clock prescaler selection (Fosc is the system clock frequency)

ADPSR<1>	ADPSR<0>	ADC clock
0	0	Fosc/16
0	1	Fosc/4
1	0	Fosc/64
1	1	Fosc/1

Bit<3>: ADCGATE - ADC gate selection bit

0: Gate disabled, enabled by software ADCEN

1: Gate enabled, triggered ADC sampling enable by the falling edge of PWM7 duty cycle

Bit<2:0>: VREF<2:0> - Reference voltage selection

VREF<2>	VREF<1>	VREF<0>	Reference voltage
0	0	0	VBG 1.2V
0	0	1	Reference 2V
0	1	0	Reference 3V
0	1	1	Reference 4V
1	0	0	EXVREF
1	0	1	VDD

11. CMP Comparator

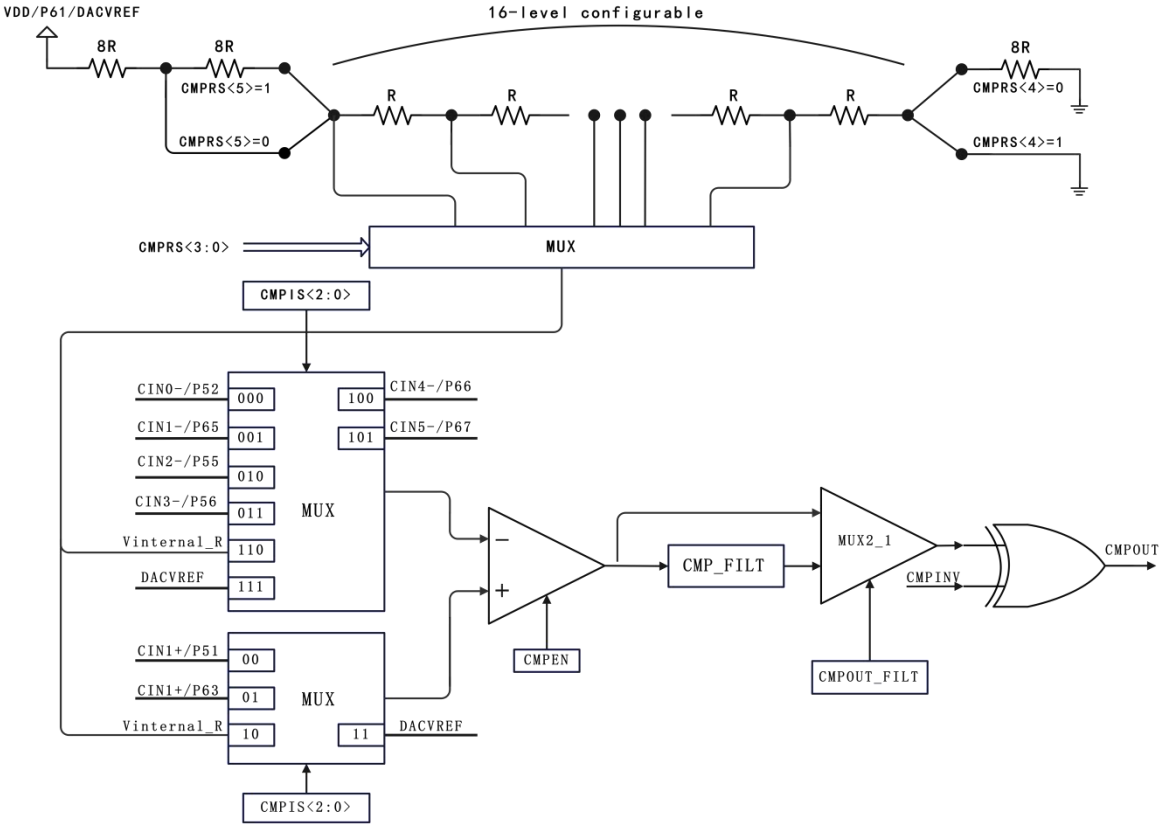
The JZ8M4600 features a built-in hardware comparator that can compare any two of the three inputs: input pin, resistor divider V_internal R, and DACVREF. One of these can be selected as the positive input, and another as the negative input. The negative input of the comparator can be P52, P55, P56, P65, P66, P67, resistor divider (selected by CMPRS<5:0>), or DACVREF. The positive input of the comparator can be P51, P63, resistor divider (selected by CMPRS<5:0>), or DACVREF. (The same port cannot serve as both the positive and negative input simultaneously, and the resistor divider input source also cannot serve as both positive and negative at the same time.)

The resistor divider can be configured through the CMPCON control register to select the input voltage source as P61 input, VDD, or DACVREF.

The output result of the comparator can be selected to output at P61 via the DACON (1A5) register's CMPOE bit, supporting output inversion. The chip supports digital filtering of the output result, which can be selected in the OPTION.

The comparator supports interrupt triggering based on output result changes; enabling CMPIE can generate interrupt signals.

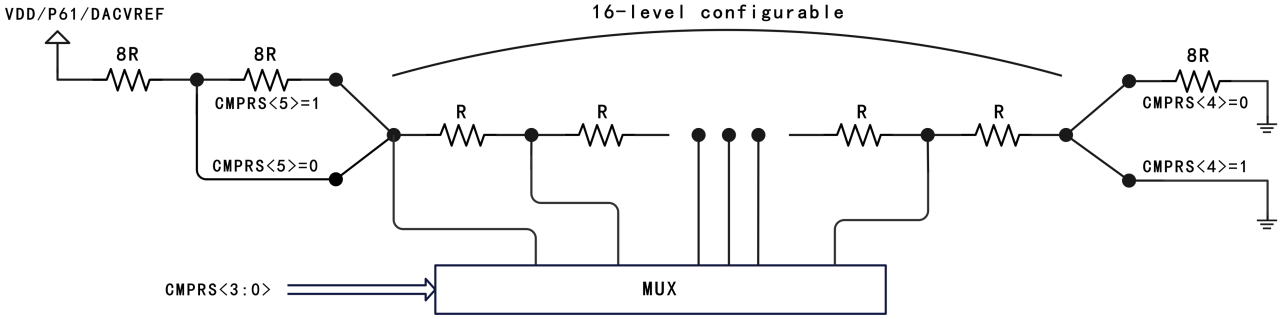
The comparator supports wake-up from output result changes; enabling CMPWE can wake up from idle mode and sleep mode. If CMPEN is enabled in idle mode and sleep mode, it will enable the low-speed oscillator, increasing sleep power consumption.



Comparator Schematic Description

11.1 Vinternal R output voltage of pressure divider resistor

The output voltage V_internal R of the resistor divider is composed of a series of resistors that can produce different levels of reference voltages. CMPRS<5:0> jointly determines the magnitude of V_internal R, with CMPRS<5> and CMPRS<4> selecting the maximum and minimum values of V_internal R, while CMPRS<3:0> is used to select the desired voltage level, which is divided into 16 equal parts from the average of the maximum and minimum values of V_internal R, chosen by CMPRS<3:0>.



Comparator adjustment schematic

Example 1: CMPRS<5>=0, CMPRS<4>=0

Value range: $V_{internal\ R} = (3/4) * VDD \sim (1/4) * VDD + (1/32) * VDD$

Calculation formula: $V_{internal\ R} = (1/4) * VDD + \frac{(n+1)}{32} * VDD$

Example 2: CMPRS<5>=0, CMPRS<4>=1

Value range: $V_{internal\ R} = (2/3) * VDD \sim (1/24) * VDD$

Calculation formula: $V_{internal\ R} = \frac{(n+1)}{24} * VDD$

Example 3: CMPRS<5>=1, CMPRS<4>=0

Value range: $V_{internal\ R} = (3/5) * VDD \sim (1/5) * VDD + (1/40) * VDD$

Calculation formula: $V_{internal\ R} = (1/5) * VDD + \frac{(n+1)}{40} * VDD$

Example 4: CMPRS<5>=1, CMPRS<4>=1

Value range: $V_{internal\ R} = (1/2) * VDD \sim (1/32) * VDD$

Calculation formula: $V_{internal\ R} = \frac{(n+1)}{32} * VDD$

n=CMPRS<3:0>

11.2 Comparator configuration

When using the comparator, enable CMPEN (this will activate the LRC used for filtering the output result CMPOUT, which will increase power consumption). Set CMPIS<5:0> to select the positive and negative input sources. The positive and negative ports must be set as inputs, and the same port cannot serve as both positive and negative inputs simultaneously. The resistor divider input source also cannot serve as both positive and negative.

If the resistor divider is selected as the input source, set register CMPRS<5:0> as needed to choose the desired resistor divider output voltage V_internal R for

comparison.

Example 1:

Select P52 as the negative input and V_internal R voltage as (18/32)*VDD for the positive input. Configure V_internal R with CMPRS<5>=0, CMPRS<4>=0, and CMPRS<3:0>=4b' 1001 (n=9) to obtain:

V_internal R = (1/4)*VDD + [(9+1)/32]*VDD = (18/32)*VDD

Once the configuration is complete, enable Bit7 CMPEN of the CMPCON0 (R1EA) control register to start the comparator comparison. The comparison result can be output through P61 by configuring Bit5 CMPOE of DACON (R1A5) (P61 must be set as output). The output result can also be inverted by setting Bit7 CMPINV of the CMPCON1 register.

11.3 Usage of DACVREF

The built-in DACVREF reference voltage can provide a voltage from 1.2V to 4.9V, which can measure the level of external power supply voltage. Specifically, this can be implemented by selecting the DACVREF reference voltage as the negative input of the comparator to compare with the positive input V_internal R. Set the power supply of V_internal R to VDD, and by adjusting the voltage level of V_internal R and comparing with the DACVREF voltage, the voltage of VDD can be determined. If n (CMPRS[3:0] in decimal) makes V_internal R closest to 1.2V (the minimum value of the DAC), using the four cases in 3.12.1 as examples, the voltage of VDD can be calculated using the following formulas:

For using Case 1: VDD = [32/(n+9)] * 1.2V;

For using Case 2: VDD = [24/(n+1)] * 1.2V;

For using Case 3: VDD = [40/(n+9)] * 1.2V;

For using Case 4: VDD = [32/(n+1)] * 1.2V;

11.4 RFC resistor frequency conversion

The JZ8M4600 has a built-in RFC resistor frequency conversion function, which controls TC0 capture using the comparison result of the comparator to achieve time counting of external voltage changes.

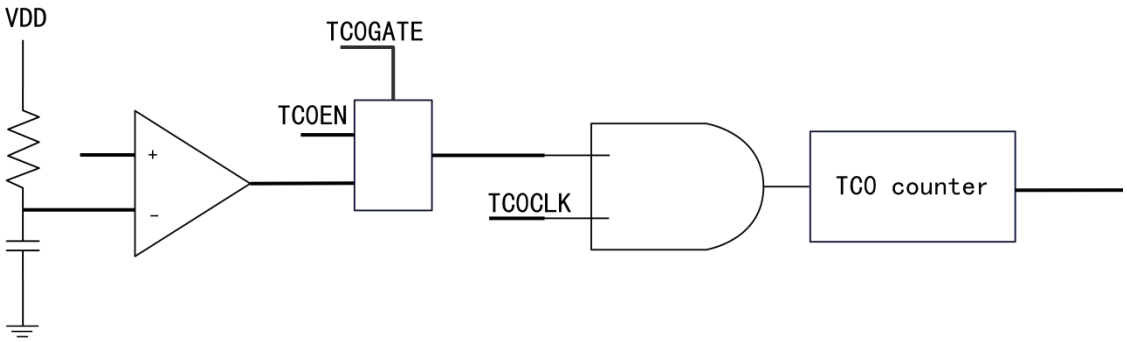
RFC principle:

The change in voltage at the RFC port affects the output result of the comparator. When the CMPGATE bit of register R1C3 is enabled, the TC0 count is controlled by the output result CMPOUT of the comparator. When the RFC port voltage is lower than the positive voltage of the comparator and CMPOUT=1, TC0 starts counting; when the RFC port voltage is higher than the positive voltage of the comparator and CMPOUT=0, TC0

stops counting. The TC0 count value records the time taken for the RFC port voltage to charge to the preset voltage value (the positive voltage of the comparator).

Application steps:

1. Set the PxAE register to select the analog port of the comparator;
2. Set registers CMPCON0 and CMPCON1 to establish the positive input source of the comparator as a fixed voltage and the negative input source of the comparator as an external port (as shown in the diagram);
3. Set the port output of the negative input source of the comparator to low level to discharge the port capacitor;
4. Clear the initial value of the TC0 timer;
5. Set comparator. The port for the negative input source is set as the analog input port, and the sampling of the RFC port voltage begins;
6. Read the TC0 count value and calculate the RFC port charging time;



RFC structure diagram

11.5 CMP related registers

11.5.1 R1A5/DACON (DAC control register)

0X1A5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DACON	DACEN	DACOUT	CMPOE	-	ADAT<11:8>			
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit<5>: CMPOE - Comparator result output enable

0: P61 as GPIO

1: Comparator result output from P61

11.5.2 R1C3/PWM7CON (TCO capture comparator gating)

0X1C3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM7H	CMPGATE	PWM_PULSE_EN	PWM7S	PWM7EN	PWM7DTH<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPGATE - TCO capture gating enable bit

0: Disable

1: Enable gate control, CMPOUT as the capture source

11.5.3 R1EA/CMPCON0 (CMP Control Register 0)

0X1EA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON0	CMPEN	CMPOUT	CMPRS<5:0>					
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPEN - CMP Enable Control Bit

0: Disable

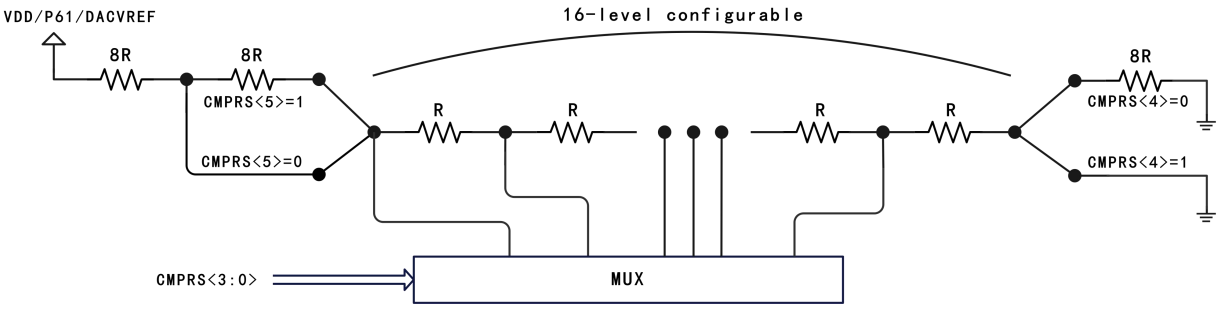
1: Enable

Bit<6>: CMPOUT - CMP Result Output Bit

0: The positive voltage of the comparator is less than the negative voltage

1: The positive voltage of the comparator is greater than the negative voltage

Bit<5:0>: CMPRS<5:0> - Comparator Trim Bit



When CMPCON1 register = 0x17, the comparator positive terminal selects resistor voltage divider, the comparator negative terminal selects DACVREF, VREFCAL = 0x00 (1.21V), different resistor divider levels CMPRS<5:0> correspond to different detection voltages, as detailed in the table below (the gray section indicates detection voltages that are not allowed):

CMPRS	Measuring Voltage/V	CMPRS	Measuring Voltage/V	CMPRS	Measuring Voltage/V	CMPRS	Measuring Voltage/V
00H	4.30	10H	29.04	20H	5.38	30H	38.72
01H	3.87	11H	14.52	21H	4.84	31H	19.36
02H	3.52	12H	9.68	22H	4.40	32H	12.91
03H	3.23	13H	7.26	23H	4.03	33H	9.68
04H	2.98	14H	5.81	24H	3.72	34H	7.74
05H	2.77	15H	4.84	25H	3.46	35H	6.45
06H	2.58	16H	4.15	26H	3.23	36H	5.53
07H	2.42	17H	3.63	27H	3.03	37H	4.84
08H	2.28	18H	3.23	28H	2.85	38H	4.30
09H	2.15	19H	2.90	29H	2.69	39H	3.87
0AH	2.04	1AH	2.64	2AH	2.55	3AH	3.52
0BH	1.94	1BH	2.42	2BH	2.42	3BH	3.23
0CH	1.84	1CH	2.23	2CH	2.30	3CH	2.98
0DH	1.76	1DH	2.07	2DH	2.20	3DH	2.77
0EH	1.68	1EH	1.94	2EH	2.10	3EH	2.58
0FH	1.61	1FH	1.82	2FH	2.02	3FH	2.42

11.5.4 R1EB/CMPCON1 (CMP Control Register 1)

0X1EB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON1	CMPINV	CMPIS<6:0>						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPINV-CMPOUT output result inversion

0: No inversion

1: Inversion

Bit<6:5>: CMPIS<6:5> - Voltage divider resistor input voltage source selection

CMPIS<6>	CMPIS<5>	Voltage divider resistor input source
0	0	VDD
0	1	P61
1	0	DACVREF
1	1	Reserved

Bit<4:3>: CMPIS<4:3> - Positive input source selection of the comparator

CMPIS<4>	CMPIS<3>	Positive input source
0	0	CIN0+/P51
0	1	CIN1+/P63
1	0	Resistive voltage divider
1	1	DACVREF

Bit<2:0>: CMPIS<2:0> - Negative input source selection of the comparator

CMPIS<2>	CMPIS<1>	CMPIS	Negative Electrode Input Source
0	0	0	CIN0-/P52
0	0	1	CIN1-/P65
0	1	0	CIN2-/P55
0	1	1	CIN3-/P56
1	0	0	CIN4-/P66
1	0	1	CIN5-/P67
1	1	0	Resistive voltage divider
1	1	1	DACVREF

12. LED Dot Matrix Driver

The JZ8M4600 chip has a built-in LED driver module, which supports a maximum of 8*8 mode for driving 64 LEDs. The LEDCON register can be configured for LEDDUTY<2:0> to select different dot matrix modes (4*4, 5*5, 6*6, 6*7, 7*7, 7*8, 8*8) while keeping the corresponding LED addresses constant (all starting from LED0). The LED data is set from LEDRAM0~7. The LED clock source can be selected from either the system clock or the instruction clock, with a clock division of 4/8/16/32/64/128 through LEDPSR<2:0>. The brightness of the lights can be adjusted using the LED duty cycle register LEDDT<6:0>.

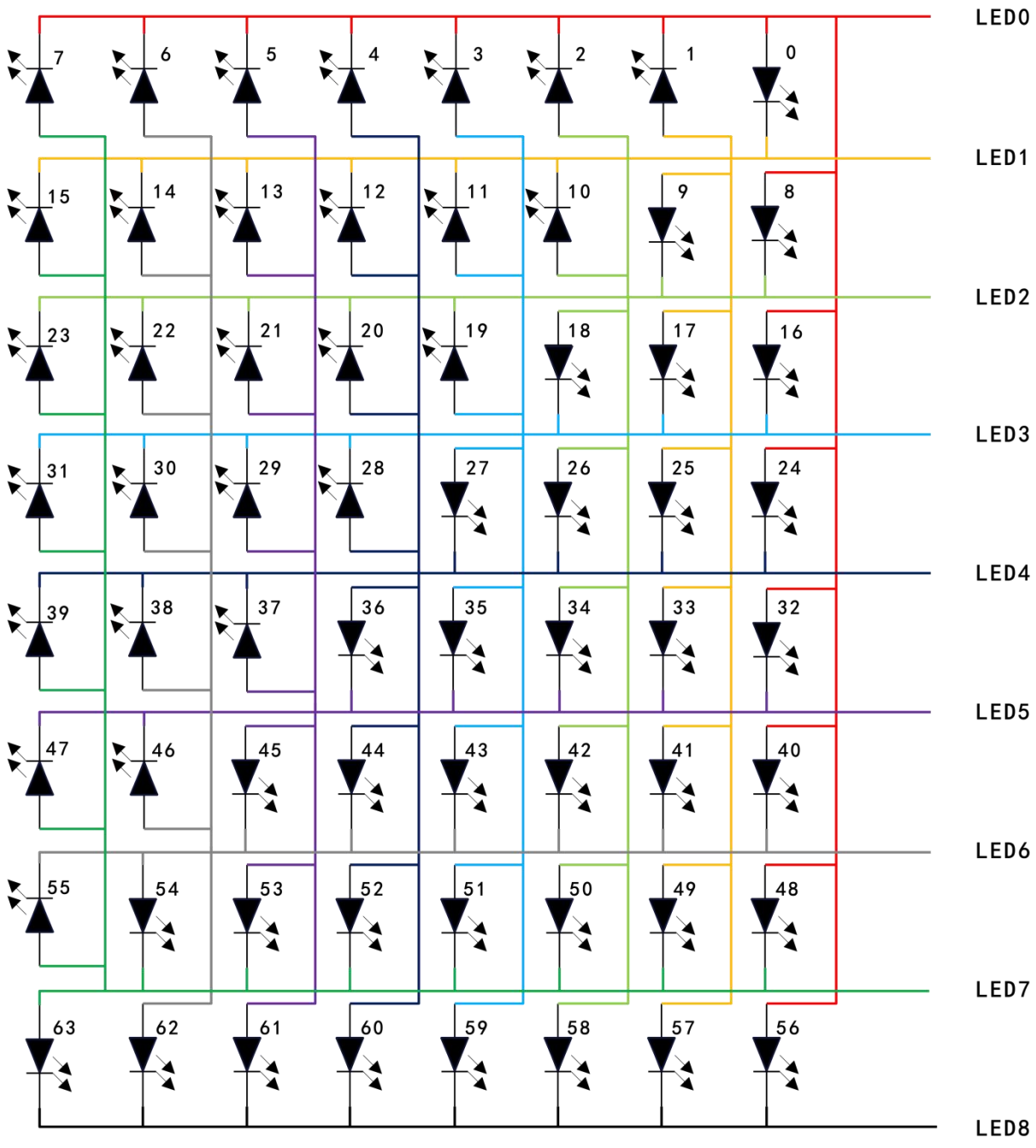
12.1 LED Function Description

The LED dot matrix has three main scanning modes. The commonly used 7*7 matrix and larger primarily use a three-light scanning mode, meaning that a maximum of three lights can be lit simultaneously (common cathode). Smaller matrix modes primarily use dual-light and single-light scanning modes, meaning at most two lights or one light can be lit at a time. LEDRAM0~7 corresponds to the status of the lights displayed in the table, where 1 indicates the light is on, and 0 indicates the light is off.

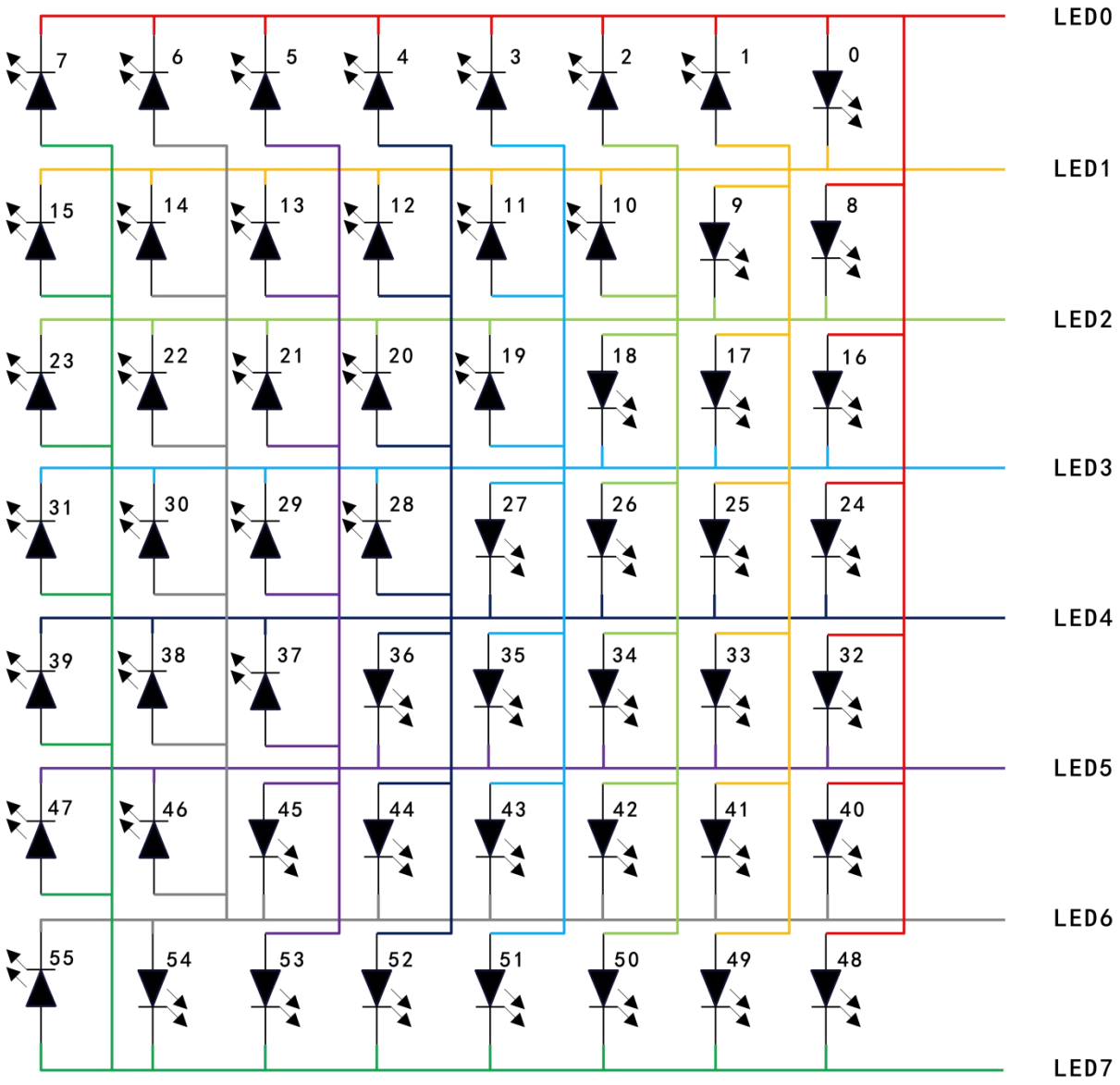
Set the register LEDEN=1 to enable the LED dot matrix mode. When setting LEDDT<6:0> to 0x7F, the brightness is at its highest. The LEDHOLD can be set to provide a scanning pause function.

LEDRAM	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM0	7	6	5	4	3	2	1	0
LEDRAM1	15	14	13	12	11	10	9	8
LEDRAM2	23	22	21	20	19	18	17	16
LEDRAM3	31	30	29	28	27	26	25	24
LEDRAM4	39	38	37	35	35	34	33	32
LEDRAM5	47	46	45	44	43	42	41	40
LEDRAM6	55	54	53	52	51	50	49	48
LEDRAM7	63	62	61	60	59	58	57	56

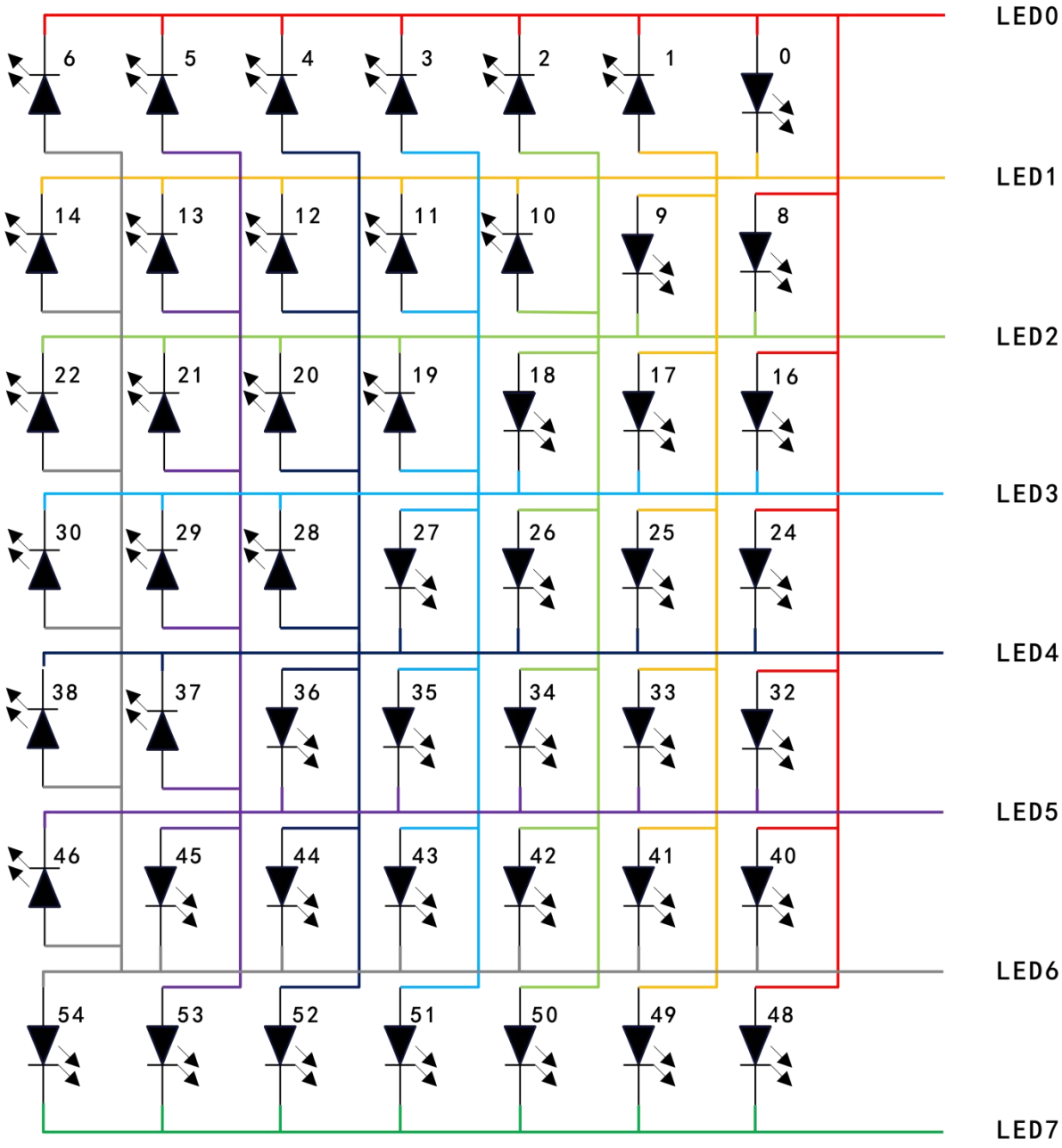
8*8 Matrix:


LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED8
7 6 5 4 3 2 1 0
15 14 13 12 11 10 9 8
23 22 21 20 19 18 17 16
31 30 29 28 27 26 25 24
39 38 37 36 35 34 33 32
47 46 45 44 43 42 41 40
55 54 53 52 51 50 49 48
63 62 61 60 59 58 57 56

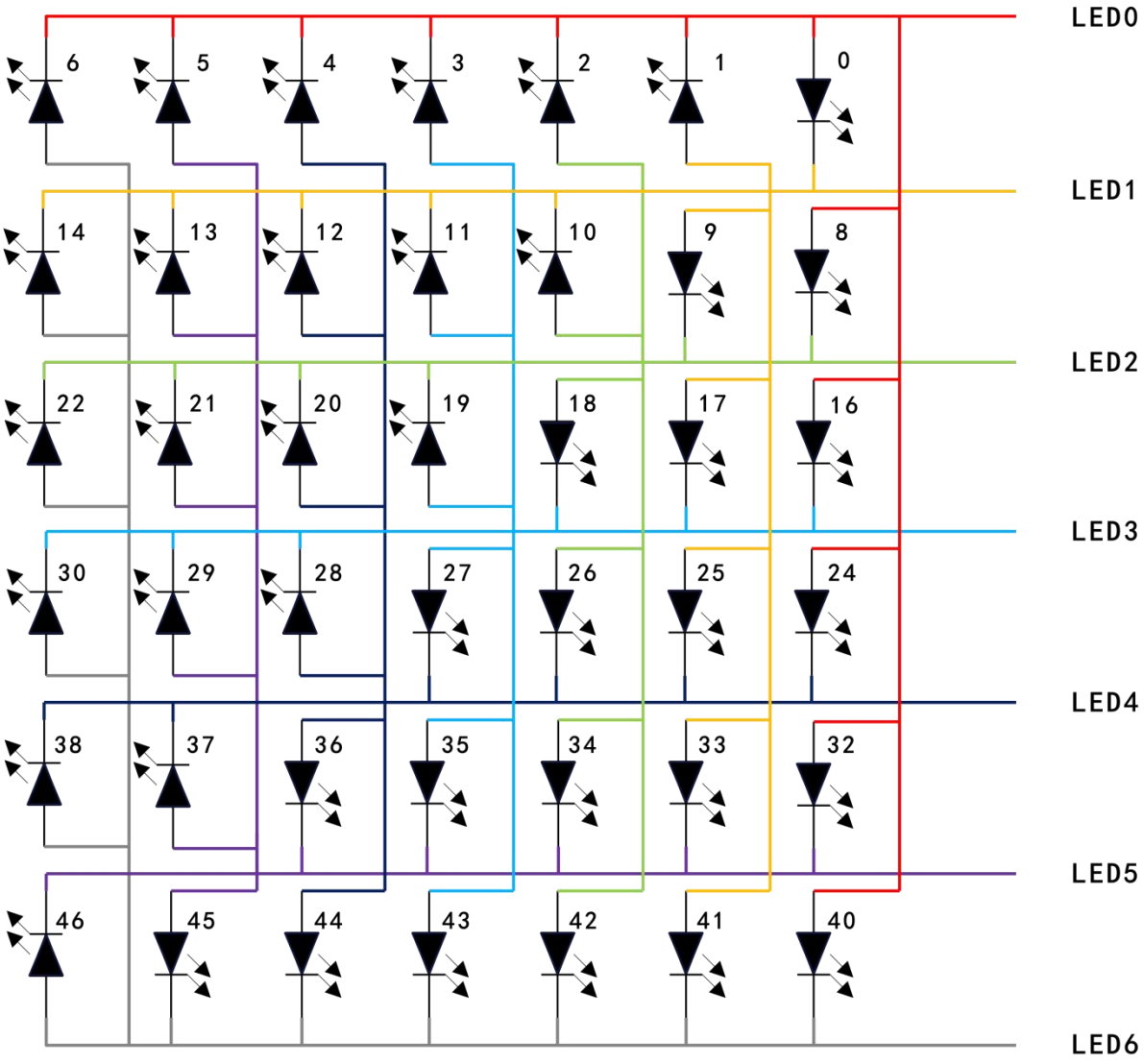
7*8 Matrix:


LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
7 6 5 4 3 2 1 0
15 14 13 12 11 10 9 8
23 22 21 20 19 18 17 16
31 30 29 28 27 26 25 24
39 38 37 36 35 34 33 32
47 46 45 44 43 42 41 40
55 54 53 52 51 50 49 48

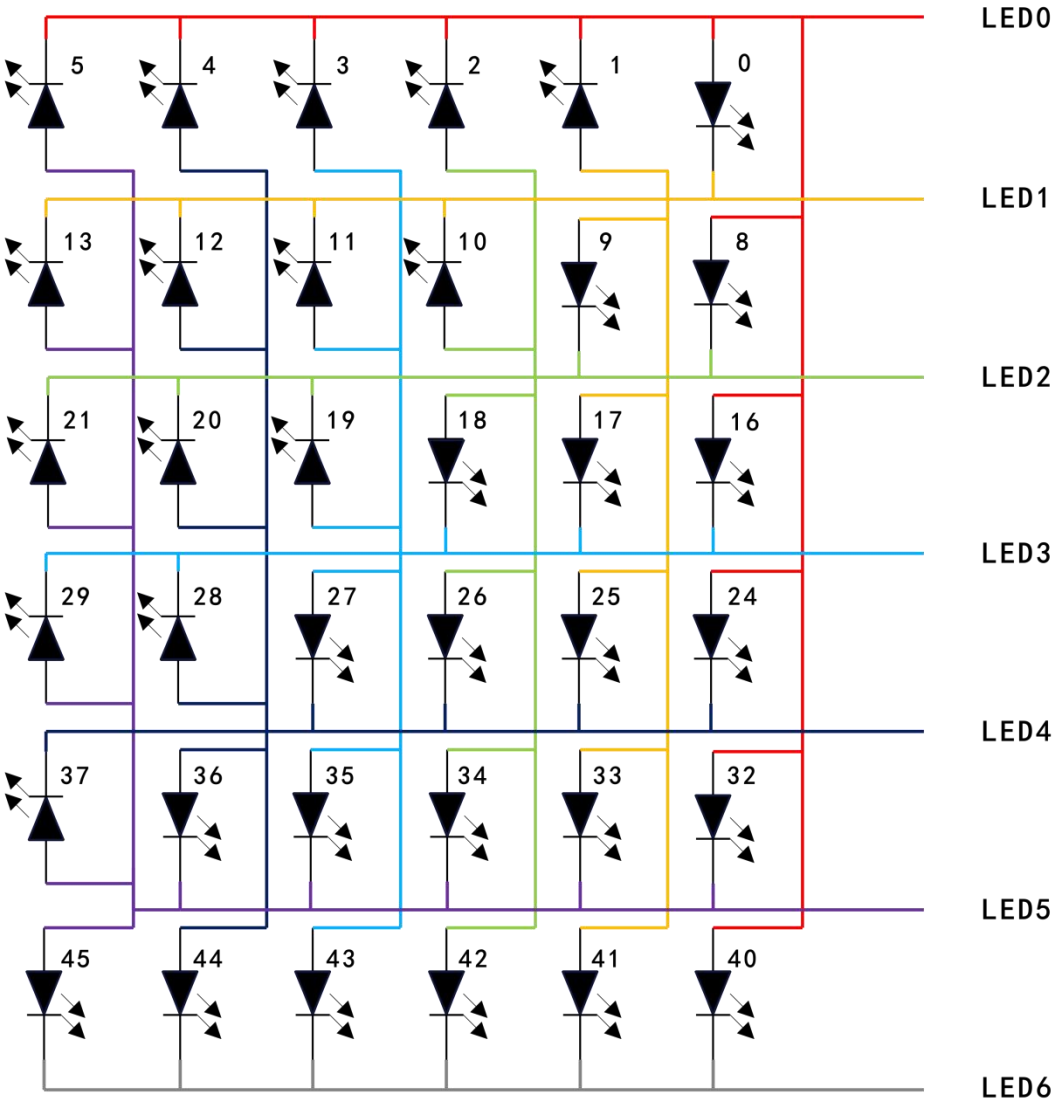
7*7 Matrix:


LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
6 5 4 3 2 1 0
14 13 12 11 10 9 8
22 21 20 19 18 17 16
30 29 28 27 26 25 24
38 37 36 35 34 33 32
46 45 44 43 42 41 40
54 53 52 51 50 49 48

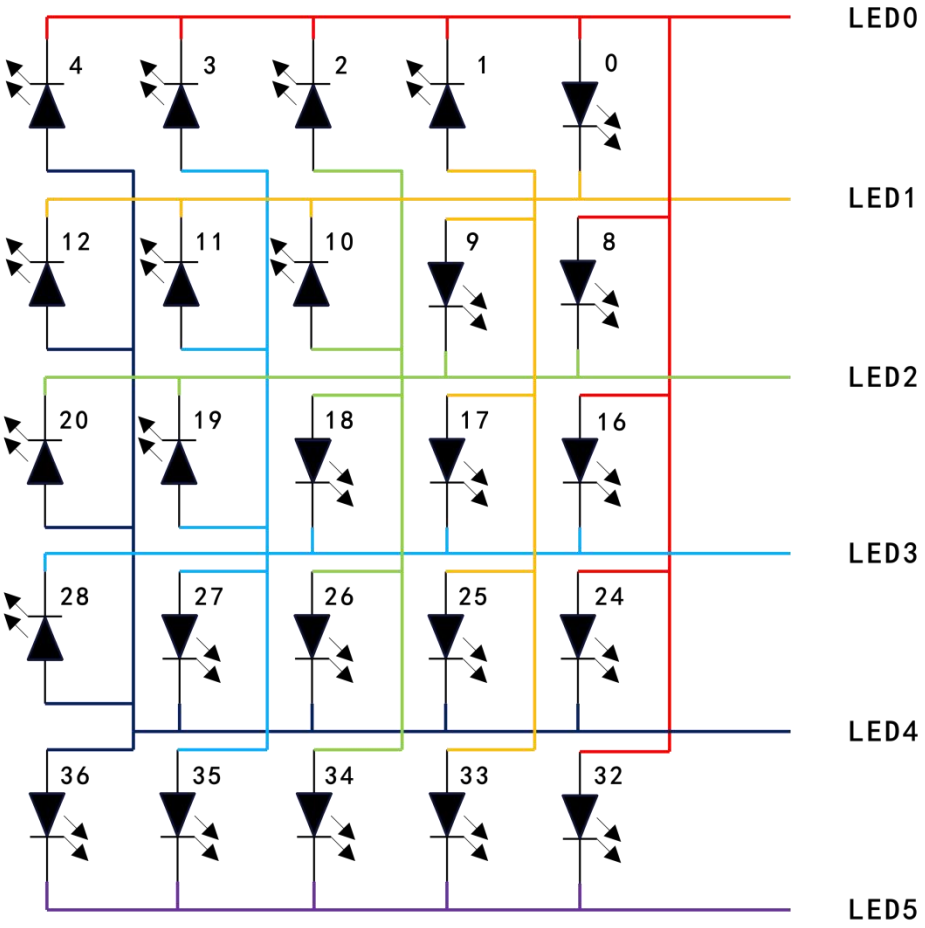
6*7 Matrix:


LED0
LED1
LED2
LED3
LED4
LED5
LED6
6 5 4 3 2 1 0
14 13 12 11 10 9 8
22 21 20 19 18 17 16
30 29 28 27 26 25 24
38 37 36 35 34 33 32
46 45 44 43 42 41 40

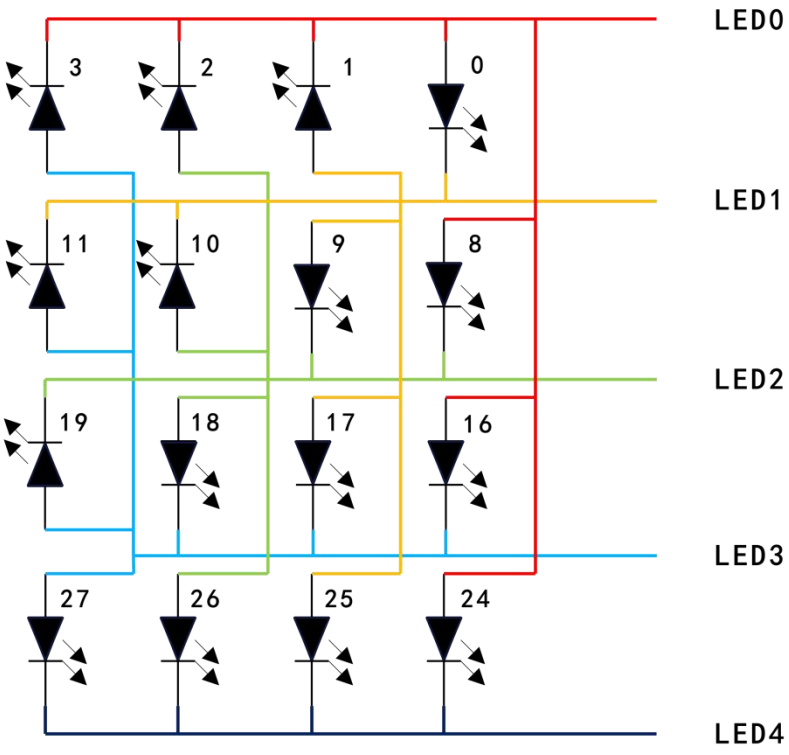
6*6 Matrix:

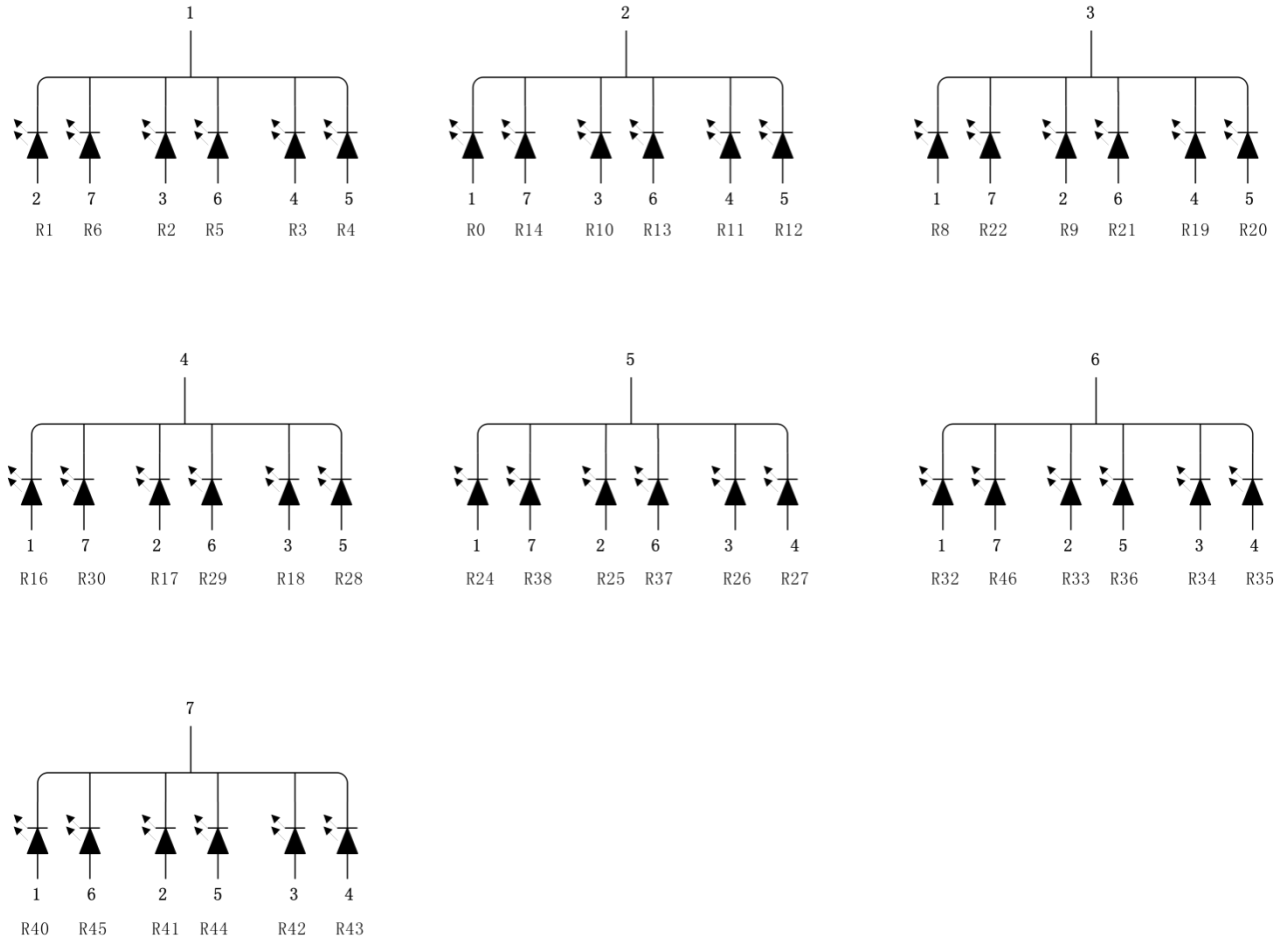

LED0
LED1
LED2
LED3
LED4
LED5
LED6
5 4 3 2 1 0
13 12 11 10 9 8
21 20 19 18 17 16
29 28 27 26 25 24
37 36 35 34 33 32
45 44 43 42 41 40

5*5 Matrix:



4*4 matrix:





Dot Matrix Scanning Distribution Map (6*7)

12.2 LED Dot Matrix Driver Setup Instructions

1. Set the register LEDRAM0～7 write values to light up the corresponding LED lights.
2. Set the LED duty cycle register LEDDT<6:0> to configure the brightness needed for the LEDs.
3. Configure the LED control register to enable the LEDs, set the dot matrix mode, and select the LED clock source and division ratio.
4. If you need to pause the LED dot matrix scan, set LEDHOLD=1, and the LED port outputs a low level; when LEDHOLD=0, the LED port output resumes and continues scanning.

12.3 Related Registers for LED Dot Matrix

12.3.1 R1F0/LEDRAM0 (LEDRAM Register 0)

0X1F0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM0	LEDRAM0<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM0<7:0> - LEDRAM data read/write bit

12.3.2 R1F1/LEDRAM1 (LEDRAM Register 1)

0X1F1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM1	LEDRAM1<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM1<7:0> - LEDRAM data read/write bit

12.3.3 R1F2/LEDRAM2 (LEDRAM Register 2)

0X1F2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM2	LEDRAM2<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM2<7:0> - LEDRAM data read/write bit

12.3.4 R1F3/LEDRAM3 (LEDRAM Register 3)

0X1F3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM3	LEDRAM3<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM3<7:0> - LED RAM data read/write bit

12.3.5 R1F4/LEDRAM4 (LEDRAM register 4)

0X1F4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM4	LEDRAM4<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM4<7:0> - LEDRAM data read/write bit

12.3.6 R1F5/LEDRAM5 (LEDRAM register 5)

0X1F5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM5	LEDRAM5<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM5<7:0> - LEDRAM data read/write bit

12.3.7 R1F6/LEDRAM6 (LEDRAM Register 6)

0X1F6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM6	LEDRAM6<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM6<7:0> - LEDRAM Data Read/Write Bits

12.3.8 R1F7/LEDRAM7 (LEDRAM Register 7)

0X1F7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM7	LEDRAM7<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM7<7:0> - LEDRAM Data Read/Write Bits

12.3.9 R1F8/LEDCON (LED Control Register)

0X1F8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDCON	LEDEN	LEDDUTY<2:0>			LEDCKS	LEDPSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: LEDEN - LED enable bit

0: Disable

1: Enable

Bit<6:4>: LEDDUTY<2:0> - LED matrix mode selection bits

LEDDUTY<2>	LEDDUTY<1>	LEDDUTY<0>	LED Dot Matrix Mode
0	0	0	4*4
0	0	1	5*5
0	1	0	6*6
0	1	1	6*7
1	0	0	7*7

1	0	1	7*8
1	1	0	8*8

Bit<3>：LEDCKS - LED Clock Source Selection Bit

0: System Clock

1：Instruction Clock

Bit<2:0>：LEDPSR<2:0> - LED Clock Division Selection Bit

LEDPSR<2>	LEDPSR<1>	LEDPSR<0>	Division Ratio
0	0	0	4 clock
0	0	1	8 clock
0	1	0	16 clock
0	1	1	32 clock
1	0	0	64 clock
1	0	1	128 clock

12.3.10 R1F9/LEDDT (LED Duty Cycle Register)

0X1F9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDDT	LEDHOLD	LEDDT<6:0>						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: LEDHOLD - LED hold pause bit

0: LED operates normally

1: LED is on hold

Bit<6:0>: LEDDT<6:0> - LED brightness selection bits

00H(0 level: dimmest) ～ 7FH(127 level: brightest)

13. UART/IIC/SPI three-in-one serial port

The JZ8M4600 has an integrated triple selectable serial interface, enabling easy connection of the MCU with devices or equipment featuring different interfaces. Users can select any communication mode (UART, IIC, or SPI) by configuring the two bits MODE1～0 in the SCON0(R1E3) register.

13.1 UART serial receiver/transmitter

The Universal Synchronous/Asynchronous Receiver-Transmitter (UART) serial port is a serial I/O communication peripheral. The serial interface is used for low-speed data transmission and communication with low-speed peripherals. The JZ8M4600 supports a data length of one byte, with a transmission format that includes a start bit, 8 data bits, a parity bit, and a stop bit. The programmable baud rate supports peripherals with different speeds.

The serial communication mode mainly has the following two modes, selected by Bit 5 of the SSICON1 (R1E4) register.

Mode 1, 8-bit communication mode, consists of one start bit and 8 data bits, where the send and receive baud rate can select the system clock's division, with TC0 or TC3 overflow signals as the clock source.

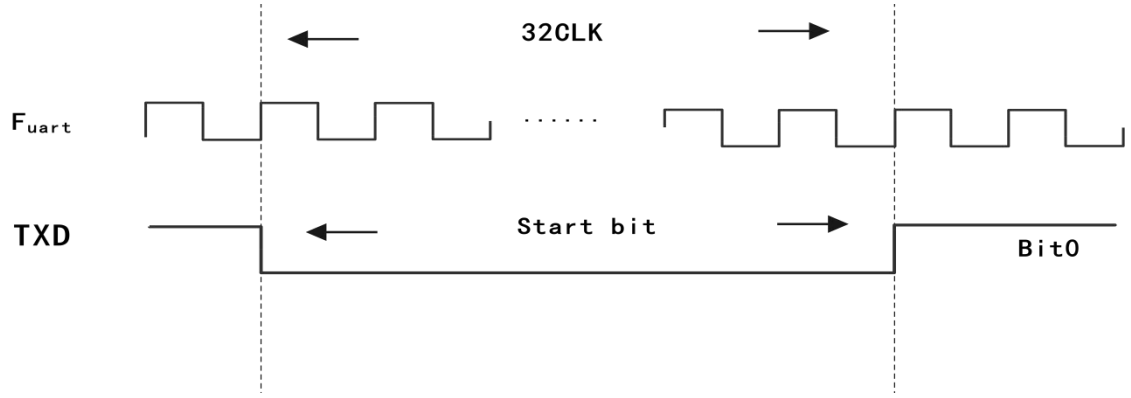
Mode 2, 9-bit communication mode, consists of one start bit and 8+1 data bits. The ninth data bit is sent via Bit 1 of the SSICON1 (R1E4) register, and the send and receive communication baud rate can select the system clock's division, with TC0 or TC3 overflow signals as the clock source.

13.1.1 UART Transmission

The main operations for UART serial data transmission are as follows:

1. Configure the UART serial control registers SSICON0 (R1E3) and SSICON1 (R1E4), select the corresponding mode, port, and baud rate, and enable TEN for transmission.
2. Write the data to the UART transmit and receive data register SSIBUF (R1E6); the UART will automatically begin transmission.
3. Data will be sent serially from the TX pin, with the data output from LSB to MSB.
4. Stop bit: output one stop bit ("1").

The diagram below shows the timing of the UART sending counter (32CLK is for reference only; the baud rate can be selected through configuration bits).

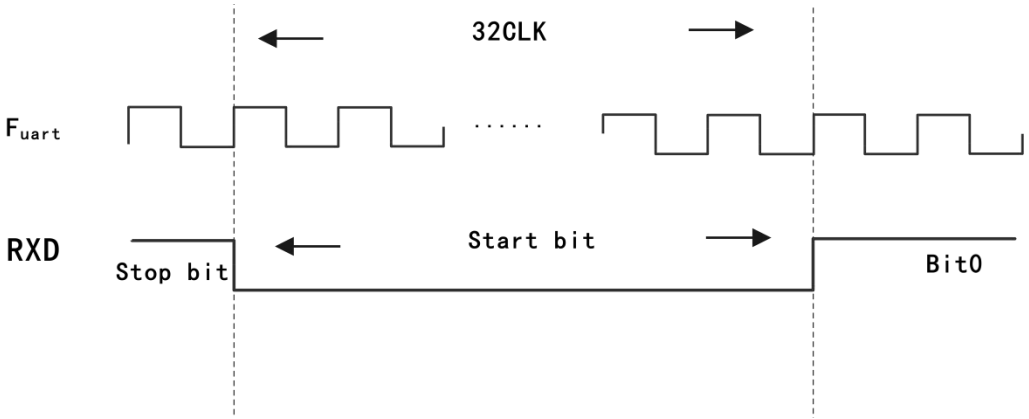


13.1.2 UART Reception

The main operations for UART serial data reception are as follows:

1. Set the REN bit of the SSICON1 (R1E4) register high to enable UART reception functionality. The UART monitors the RXD pin and performs internal synchronization upon detecting the start bit.
2. Start bit, output a "0" bit.
3. The received data is shifted into the BUF register from LSB to MSB order; after receiving 8 bits of data, it will be written to SSIBUF.
4. Parity bit; when the 9-bit UART mode is enabled, RBIT8 of the SSISR1 register can be read.
5. Stop bit: output a stop bit ("1").
6. Receive the parity bit and stop bit; after receiving the last character, the RI bit of the SCON0 register will be set to "1". If UART interrupts are enabled and EI is set, a UART interrupt will occur.
7. Read the received data from the SSIBUF register. The RI bit is cleared by software.

The diagram below shows the timing of the UART reception counter (32CLK is for reference only, baud rate can be selected via configuration bits).



13.2 IIC Serial Receiver/Transmitter

IIC is a synchronous serial half-duplex communication bus. This bus allows multiple devices to be connected simultaneously and selected through the specific address of each chip.

On the IIC bus, only one device is allowed to be in the transmitting state at any given time. The data sent is received by all chips on the bus. The IIC communication protocol includes a device address; only when the address carried by the sender matches the address of a specific receiver can the receiver execute relevant instructions.

The IIC bus specifies that when the device is in an idle state, both the clock and data lines are at a high level.

13.2.1 IIC Operating Process

The main operations for sending data via the IIC serial are as follows:

1. Start signal: SCL remains high, and SDA transitions from high to low (falling edge);
2. Send the I2C device address through the I2CADDR (1E5) register. Each I2C device has a unique device address, and the specific device address is sent to determine which I2C device to access.
3. The I2C device address is followed by a read/write bit; 0 indicates a write operation, and 1 indicates a read operation;
4. The matching slave sends an ACK response signal in the ninth clock cycle. ACK (low level) indicates successful reception and continues transmission, while NACK (high level) indicates a failure in data reception or termination of transmission.
5. Data transmission (write operation), the master device writes data to the slave device. After the address matches and receives the acknowledgment signal, the master device starts sending bytes, and the slave device responds with ACK after each byte.

   Data transmission (read operation), the master device reads the data sent by the slave device. After the address matches and the master receives the slave ACK signal, it waits for the slave to send bytes, and the master responds with ACK after each byte. When the acknowledgment signal is NACK, it stops sending.
6. Repeat start condition, when the master needs to switch the read/write direction or access another slave, it does not release the bus and continues transmission, returning to operation 2;
7. Stop condition, SCL remains high, and SDA transitions from low to high (rising

edge).

13.2.2 IIC Send and Receive

1. Host Mode

(1) The main operations for IIC sending data are as follows:

1. Set the SSICON0(R1E3) register to enable SSIEN, select IIC mode, and set the clock division as needed.
2. Set the SSICON1(R1E4) register to configure the mapped port as needed, setting it to host mode.
3. If an interrupt is required upon completion of sending, enable TX_IICIE.
4. Write the slave address and WR control in I2CADDR(R1E5).
5. If you need to send an address, enable START; if you need to end communication, enable STOP.
6. Enable RUN_EN (R1E4) to start sending.
7. Wait for the RUN_EN signal to clear after transmission completion to finish address sending (and manually clear the START or STOP signals).
8. Write the data to be sent into SSIBUF (R1E6), and repeat steps 6-7 to complete the data sending.
9. Before the last data sending, you need to enable the STOP signal to end communication before enabling the RUN_EN signal.

(2) The main operations for IIC receiving data are as follows:

1. Set the SSICON0(R1E3) register to enable SSIEN, select IIC mode, and set the clock division as needed.
2. Set the SSICON1(R1E4) register to configure the mapped port as needed, setting it to host mode.
3. If you need to enter an interrupt upon completion of reception, enable TX_IICIE.
4. Write the slave address and WR control in I2CADDR(R1E5).
5. If you need to receive data, enable START; if you need to end communication, enable STOP.
6. Set AA=1 to enable the acknowledgement signal, then enable RUN_EN (R1E4) to start receiving data.
7. After waiting for the RUN_EN signal to finish sending, clear it to 0 to complete the reception (and manually clear the START or STOP signal).
8. The received data is stored in SSIBUF. Repeat steps 6 to 7 to complete multiple data receptions.

9. Before receiving the last data, the RUN_EN signal must be enabled, and the STOP signal and non-acknowledgment signal (AA=0) must be enabled to end communication.

2. Slave mode

(1) The main operations for IIC sending data are as follows:

1. Set the SSICON0(R1E3) register to enable SSIEN, select IIC mode, and set the clock division as needed.
2. Set the SSICON1 (R1E4) register, configure the mapping port as needed, and set the slave mode.
3. If an interrupt is required upon completion of sending, enable TX_IICIE.
4. Write the slave address in I2CADDR (R1E5).
5. The slave address matches and sends acknowledgment signal AA=1.
6. Wait for the TREQ (R1E8) flag to be sent after completion, then receive the host ACK and set it to 1.
7. Wait for one ACK time before starting the next data transmission.
8. Write the data to be sent into SSIBUF (R1E6), and clear the TREQ flag at this time.
9. Repeat steps 6 to 8 to complete multiple data transmissions.

(2) The main operations for IIC receiving data are as follows:

1. Set the SSICON0(R1E3) register to enable SSIEN, select IIC mode, and set the clock division as needed.
2. Set the SSICON1 (R1E4) register, configure the mapping port as needed, and set the slave mode.
3. If an interrupt is required upon completion of sending, enable TX_IICIE.
4. Write the slave address in I2CADDR (R1E5).
5. Set to 1 after waiting for the completion of receiving the RREQ (R1E8) flag.
6. Manually clear the RREQ flag and send the response signal AA=1.
7. The received data is stored in SSIBUF(R1E6),
8. Repeat steps 5 to 7 to receive multiple pieces of data.

13.3 SPI Receiver/Transmitter

SPI is a synchronous, full-duplex, master-slave serial communication protocol. This bus consists of four lines: MISO, MOSI, SCK, and CS, and different communication modes can be achieved through clock polarity and phase configuration.

The following are the main functions of the four SPI lines:

SCK (Serial Clock): Clock signal provided by the master device, which determines

the timing of data transmission.

MOSI (Master Out, Slave In): The data output pin from the master device and the input pin for the slave device.

MISO (Master In, Slave Out): The data input pin for the master device and the output pin from the slave device.

CS (Chip Select): Chip select pin, active low, controlled by the master device, used to select the slave device for current communication.

13.3.1 SPI Working Mode

SPI can configure the clock polarity and phase through the SSICON1(R1E4) register Bit6:5.

- CPOL=0, when the SPI bus is idle, the clock line SCK is at a low level.
- CPOL=1, when the SPI bus is idle, the clock line SCK is at a high level.
- CPHA=0, on the first edge transition of SCK, the master samples the level on the MISO pin; master data transmission occurs on the second edge transition.
- CPHA=1, on the second edge transition of SCK, the master samples the level on the MISO pin. Master data transmission occurs on the first edge transition.

Four modes are implemented as follows:

Mode0: CPOL=0, CPHA=0: In this mode, when idle, SCK is at a low level, and data is sampled on the first edge, which is the transition from low to high on SCK, so data sampling occurs on the rising edge, and data transmission occurs on the falling edge.

Mode1 (Not for use): CPOL=0, CPHA=1: In this mode, when idle, SCK is at a low level, and data transmission occurs on the first edge, which is the transition from low to high on SCK, so data sampling occurs on the falling edge, and data transmission occurs on the rising edge.

Mode2: CPOL=1, CPHA=0: In this mode, when idle, SCK is at a high level, and data is gathered on the first edge, which is the transition from high to low on SCK, so data gathering occurs on the falling edge, and data transmission occurs on the rising edge.

Mode3: CPOL=1, CPHA=1: At this time, the idle state has SCK at a high level, and data transmission occurs on the first edge, that is, when SCK transitions from high to low. Therefore, data collection happens on the rising edge, and data transmission occurs on the falling edge.

13.3.2 SPI Sending and Receiving

1. Master Mode

(1) SPI Data Sending Process:

1. Set the SSICON0 (R1E3) register to enable SSIEN, select SPI mode, and configure the clock prescaler as needed.
2. Set the SSICON1 (R1E4) register to configure the mapped port as needed, set master mode, clock polarity, and phase.
3. If an interrupt is needed upon completion of sending, enable RX_SPIIE.
4. Pull the chip select CS signal port low, store the data to be sent in SSIBUF, and set TEN to enable sending.
5. Set the SSICON1 (R1E4) register to enable RUN_EN, and start sending data.
6. Wait for the RUN_EN signal to clear after sending is completed, finishing one frame of data transmission.
7. After data transmission is complete, release and pull the chip select CS signal port high.

(2) SPI Data Reception Process:

1. While the master device sends data, the slave device returns response data through the MISO line, enabling reception by setting REN.
2. If RX_SPIIE is enabled, an interrupt is triggered upon completion of reception.
3. The received data can be obtained by reading the SSIBUF register.

2. Slave Mode

(1) SPI Data Sending Process:

1. Set the SSICON0 (R1E3) register to enable SSIEN, select SPI mode, and configure the clock prescaler as needed.
2. Set the SSICON1 (R1E4) register to configure the mapped port as needed, set master mode, clock polarity, and phase.
3. If an interrupt is needed upon completion of sending, enable RX_SPIIE.
4. Store the data to be sent in SSIBUF and enable transmission by setting TEN.
5. Set the SSICON1 (R1E4) register to enable RUN_EN, and start sending data.
6. Wait for the RUN_EN signal to clear after sending is completed, finishing one frame of data transmission.

(2) SPI Data Reception Process:

1. Enable reception by setting REN, and if RX_SPIIE is enabled, the slave will enter an interrupt upon completion of reception.
2. The received data can be obtained by reading the SSIBUF register.

13.4 Three-in-one Related Registers

13.4.1 R1E3/SSICON0 (Serial Control Register 0)

0X1E3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SSICON0	SSIEN	MODES<1:0>		SSICKS	SSIPTEN	SSIPSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: SSIEN - SSI three-in-one communication module enable

0: Disable

1: Enable

Bit<6:5>: MODES<1:0>-Mode selection bits

00: Not selected

01: UART mode(UART default 32 prescale)

10: IIC mode(IIC default 2 prescale)

11: SPI mode (SPI default 2 prescaler)

Bit<4:3>: SSICKS: SSIPTEN - SSI clock source selection

00: Select system clock (IIC/SPI prohibit selecting SYSCK, fastest supports system clock 2 prescaler)

01: Select prescaler clock

10: TC0 overflow (UART/IIC/SPI prohibition)

11: TC3 overflow (IIC/SPI prohibition)

Bit<2:0>: SSIPSR<2:0> - SSI prescaler selection control bits:

SSIPSR<2>	SSIPSR<1>	SSIPSR<0>	SSI division
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

13.4.2 R1E4/SSICON1 (Serial Control Register 1)

0X1E4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SSICON1	RUN_EN	START_EN	STOP_EN	MSTR	TEN	REN	AA	SSIOS
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:RUN_EN - Start sending

0: Disable

1: Enable (UART write BUFF auto-trigger)

Bit<6>:START_EN - I2C send START/SPI mode CPOL

0: Disable

1: Enable

CPOL=0, when the SPI bus is idle, the clock line SCK is at a low level.

CPOL=1, when the SPI bus is idle, the clock line SCK is at a high level.

Bit<5>:STOP_EN - I2C send STOP enable/9-bit UART mode enable (send AA)/SPI mode CPHA

0: Disable

1: Enable

CPHA=0, on the first edge transition of SCK, the master samples the level of the MISO pin; the master's data is sent on the second edge transition.

CPHA=1, on the second edge transition of SCK, the master samples the level of the MISO pin; the master's data is sent on the first edge transition.

Bit<4>:MSTR - Master/slave mode selection

0: Slave mode

1: Master mode

Bit<3>:TEN - Transmit enable control bit (Enable is needed to send data in UART and SPI mode)

0: Disable

1: Enable

Bit<2>:REN - Receive Enable Control Bit (enable is required for receiving data in UART and SPI modes)

0: Disable

1: Enable

Bit<1>:AA - I2C acknowledgment enable bit/UART bit 9 data transmission/SPI inverted data transmission

0: Disable

1: Enable

Bit<0>:SSIOS - SSI port mapping selection bit

0:

Communicatio	UART	IIC	SPI
P60	TX	SDA	MOSI
P61	RX	SCL	SCK
P62	-	-	CS
P63	-	-	MISO

1:

Communicatio	UART	IIC	SPI
P53	TX	SDA	MOSI
P54	RX	SCL	SCK
P62	-	-	CS
P63	-	-	MISO

13.4.3 R1E5/I2CADDR(I2C Address Register)

0X1E5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2CADDR	I2CADDR<6:0>							WR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

13.4.4 R1E6/SSIBUF(UART Transmit and Receive Data Register)

0X1E6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SSIBUF	SSIBUF<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

When sending in serial, the MCU writes data to SSIBUF.

During serial reception, the MCU reads data from SSIBUF.

The write and read data share the same address without affecting each other.

13.4.5 R1E7/SSISR0 (Serial Port Status Register 0)

0X1E7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SSISR0	-	BUS_BUSY	MSTR_IDLE	ARB_LOST	DATA_ACK	ADD_ACK	MSTR_ERROR	MSTR_BUSY
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	X	1	0	0	0	0	0

Bit<6>: BUS_BUSY - IIC bus busy flag in master/slave mode

0: Write 0 to clear

1: IIC bus busy

Bit<5>: MSTR_IDLE - IIC master mode idle flag

0: Working state

1: Idle state

Bit<4>: ARB_LOST - I2C master mode arbitration flag

0: Write 0 to clear

1: Lost bus control

Bit<3>:DATA_ACK - I2C master mode addressing acknowledgment flag bit

0: Write 0 to clear

1: No response for the last data transmission

Bit<2> : ADD_ACK - I2C master mode addressing acknowledgement flag

0: Write 0 to clear

1: No response for the last addressing

Bit<1> : MSTR_ERROR - I2C master mode error flag

0: Write 0 to clear

1: No response from the addressed slave / No response for the data transmission / I2C bus arbitration conflict

Bit<0> : MSTR_BUSY - I2C master module busy flag

0: Not transmitted

1: The I2C module is transmitting data (including send and receive)

13.4.6 R1E8/SSISR1 (Serial Status Register 1)

0X1E8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SSISR1	-	-	TI	RI	RBIT8	SENDFIN	TREQ	RREQ
Read/Write	R	R	R/W	R/W	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<5>: TI - UART transmit complete flag

0: Write 0 to clear

1: Transmission complete

Bit<4>: RI - UART receive complete flag

0: Write 0 to clear

1: Reception complete

Bit<3>: RBIT8 - The 9th bit of UART received data

Bit<2>: SENDFIN - I2C slave mode send complete flag

0: Data is being transmitted

1: The master device no longer requires data; the current data transmission is complete

Bit<1>: TREQ - I2C slave mode ready to send flag

0: Write 0 to clear

1: Addressed as the Transmitter or the Master Device is Ready to Receive Data

Bit<0>: RREQ - I2C slave mode receive complete flag

0: Write 0 to clear

1: Reception complete

14. EEPROM and ISP online programming

14.1 EEPROM read and write operations

The JZ8M4600 has a built-in 256 Byte 16-bit EEPROM data memory, with default factory data set to 0xFFFF. It supports real-time reading or writing of data while powered on, and when writing data, the MCU will halt instruction execution until the writing is complete.

Write EEPROM:

Before writing to the EEPROM cell, the user must first write the address to the TBRDL register, which is used to select the EEPROM address. Then, the user should write values to the EEPROM data registers E2PDATL/E2PDATH. Finally, the E2PLOCK must be opened to unlock the EEPROM write operation, setting the E2PWREN bit to 1. Once a write process is initiated, clearing the E2PWREN bit will not affect the write cycle. When the write cycle is complete, the E2PWREN bit will be cleared by hardware, and the user must activate it again before the next write operation.

Note: During EEPROM writing, the instruction clock stops, and the MCU does not execute any instructions. The high-speed oscillator and low-speed oscillator operate normally, and the system clock is normal;

Reading EEPROM:

To read the EEPROM memory unit, the user must first write the address to the TBRDL register and set the E2PRDEN bit of the E2PCON register to 1. After enabling the read control bit, the TBRD instruction should be executed, and the data from the EEPROM will be stored in the corresponding R (high 8 bits of the data) and ACC (low 8 bits of the data).

14.2 ISP Online Programming Timing

The JZ8M4600 supports two different programming methods: regular programming and in-circuit programming with power applied. For in-circuit programming, the user must pre-configure the programming port and functions.

1. Regular programming:

In the OPTION settings【Programming port configuration】, select【Normal programming/Program as the programming port only during reset (can be used by the program)】, and in the OPTION settings【Programming function selection】, select【Regular programming (programmer powered programming)】. The above configurations do not affect the usage of the programming port.

2. In-circuit programming:

In-circuit programming requires the MCU to first select "Regular programming" to have the program ready. It cannot burn an unprogrammed chip. In in-circuit programming mode, the programmer needs to connect 3 wires: GND, SDA, and SCL, and VDD should not be connected. The following two programming methods are supported.

Select the option【ISP mode timing port】to choose between programming pin【P5】(P53/P54) or【P6】(P60/P61) with power on the board.

Method 1: P53/P54 serves as the programming port only during reset; the program can be used.

Set the OPTION option [Programming Port Configuration] to [Normal Programming/Programming Port Only During Reset (Program Can Be Used)], and set the OPTION option [Programming Function Selection] to [In-System Programming with Power On]. With the above configuration, the programming pins can be used as GPIO normally. The program needs to configure specific registers and enable external interrupts to receive clock data sent by the programmer on the programming pins. After correct decoding, the software unlocks the ISP function; please refer to the ISP demo for details.

Software unlock for ISP mainly consists of the following two steps:

1. The program writes 0110 to the high 4 bits of the E2PCON (0x1E0) register, completing the first step of unlocking;

2. The program writes 0xC5 to the E2PDATH (0x1E2) register and then writes 0x3A to the E2PDATL (0x1E1) register to complete the second step of unlocking;

After completing the two steps of unlocking, the MCU hardware sets SDA and SCL as input ports, waiting for external timing control to reset the MCU.

Method 2: Serves only as a programming port; the program is uncontrollable.

Set the OPTION option [Programming Port Configuration] to [Only as a Programming Port (Hardware Pull Up, Program Uncontrollable), the chip can switch to programming mode at any time] or [Only as a Programming Port (Hardware Pull Down, Program Uncontrollable), the program cannot control it, and the chip can switch to programming mode at any time], and set the OPTION option [Programming Function Selection] to [In-System Programming with Power On]. With the above configuration, the programming pin needs to be left floating; if Type-C port upgrade is needed, connect to CC1/CC2 ports.

Note: Selecting only as a programming port means the program cannot control it; in the case of VDD being 5V, sleep will have a power consumption of about 4uA.

14.3 Related Registers

14.3.1 R1E0/E2PCON (EEPROM Control Register)

0X1E0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2PCON	E2PLOCK<3:0>				-	E2PTIME	E2PRDEN	E2PWREN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:4>: E2PLOCK<3:0>- EEPROM unlock bit for functionality

1001: Input data 1001 unlock EEPROM write operation

0110: Input data 0110 unlock ISP functionality

Bit<2>: E2PTIME- EEPROM write time select bit

0: EEPROM write time select fast mode

1: Choose slow mode for EEPROM write time

Bit<1>: E2PRDEN-EEPROM Read Enable Bit

0: Disable

1: Enable

Bit<0>: E2PWREN-EEPROM Write Enable Bit

0: Disable

1: Enable

14.3.2 R1E1/E2PDATL (EEPROM Data Low 8-bit Register)

0X1E1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2PDATL	E2PDAT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

14.3.3 R1E2/E2PDATH (EEPROM Data High 8-bit Register)

0X1E2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2PDATH	E2PDAT<15:8>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

15. OPTION Configuration Table

CODE OPTION	Options	Function Description
Watchdog	Enable	Watchdog WDT Enable
	Disable	Watchdog WDT Disable
Clock Division	2 Clocks	Instruction Clock Division Selection 2 Clocks
	4 Clocks	Instruction Clock Division Selection 4 Clocks
	8 Clocks	Instruction Clock Division Selection 8 Clocks
	16 Clocks	Instruction Clock Division Selection 16 Clocks
	32 Clocks	Instruction Clock Division Selection 32 Clocks
IRC frequency	1M	IRC Frequency Selection 1M
	4M	IRC Frequency Selection 4M
	8M	IRC Frequency Selection 8M
	16M	IRC Frequency Selection 16M
	29.4M	Special frequency of 32M fine-tuning, configurable serial baud rate 115200
	32M	IRC Frequency Selection 32M
Low Voltage Reset Option	Enabled: LVR always	Default LVR function is always enabled
	Enabled: Software	LVR enable bit is software configurable
Low Voltage Reset	LVR=1.8V	Low Voltage Reset Point Selection 1.8V
	LVR=1.9V	Low Voltage Reset Point Selection 1.9V
	LVR=2.1V	Low Voltage Reset Point Selection 2.1V
	LVR=2.3V	Low voltage reset point selection 2.3V
	LVR=2.7V	Low voltage reset point selection 2.7V
	LVR=3.0V	Low voltage reset point selection 3.0V
	LVR=3.5V	Low voltage reset point selection 3.5V
	LVR=4.0V	Low voltage reset point selection 4.0V
Reset time	PWRT=3.5ms, WDT=7.1ms	Reset establishment time=3.5ms, WDT overflow time (4 divide) = 7.1ms
	PWRT = 14ms, WDT = 28ms	Reset hold time = 14ms, WDT overflow time (4 divide) = 28ms
	PWRT = 57ms, WDT = 114ms	Reset hold time = 57ms, WDT overflow time (4 divide) = 114ms
	PWRT = 228ms, WDT = 455ms	Reset hold time = 228ms, WDT overflow time (4 divide) = 455ms
	PWRT=350us, WDT=7.1ms	Reset establishment time = 350us, WDT overflow time (4 divide) = 7.1ms
	PWRT = 350us, WDT = 28ms	Reset establishment time = 350us, WDT overflow time (4 divide) = 28ms
	PWRT = 350us, WDT = 114ms	Reset establishment time = 350us, WDT overflow time (4 divide) = 114ms
	PWRT = 350us, WDT = 455ms	Reset establishment time = 350us, WDT overflow time (4 divide) = 455ms

P55 port	RST	P55 port serves as the external reset pin
	GPIO	P55 port serves as a general input/output pin
External pull-up for P55 port	Enable	External pull-up for P55 port enabled
	Disable	P55 port external pull-up disabled
CMP_FILT	Comparator digital filtering enabled	Comparator hardware filtering enabled, with a delay of two ILRC cycles
	Comparator digital filtering disabled	Comparator result digital filtering disabled
Comparator hysteresis selection	10mV	Comparator hysteresis voltage selection 10mV
	40mV	Comparator Hysteresis Voltage Selection 40mV
	60mV	Comparator Hysteresis Voltage Selection 60mV
Standard Port Pull Current Enhancement Selection	Disable	Standard Port Pull Current Enhancement Disabled
	Enable	Standard Port Pull Current Enhancement Enabled
LED Port Sink Current Enhancement Selection	Disable	LED Port Sink Current Enhancement Disabled
	Enable	LED Port Sink Current Enhancement Enabled
LED Port Pull Current Level 1 Enhancement Selection	Disable	LED Port Pull Current Level 1 Enhancement Disabled
	Enable	LED Port Pull Current Level 1 Enable
LED Port Pull Current Level 2 Enhancement Selection	Disable	LED Port Pull Current Level 2 Enhancement Disable
	Enable	LED Port Pull Current Level 2 Enable
Package Pins	20pin	Chip Package Pin Selection 20 Pins
	16pin	Chip Package Pin Selection 16 Pins
	8pin	Chip package pin selection 8 pins
Burning Mode Selection	FLASH	Burn only the FLASH area
	EEPROM	Burn only the EEPROM area; EEPROM supports independent read and write for programs
	FLASH+EEPROM	Burn FLASH+EEPROM area
Burning Port Settings	Normal burning / Only as a burning port when reset (program can be used)	Normal burning / Only as a burning port when reset (program can be used)

	Only as a burning port (hardware pull-down program uncontrollable); the chip can enter burning mode at any time	Only as a burning port (hardware pull-down, program uncontrollable); the chip can enter burning mode at any time
	Only for programming interface (hardware pull-up program uncontrollable), the chip can enter programming mode at any time	Only for programming interface (port hardware pull-up, program uncontrollable), the chip can enter programming mode at any time
Programming function selection	Conventional programming	Conventional programming (programmer powered programming)
	In-circuit programming with power	External power programming, do not connect programmer VDD pin
Programming port selection	P60/P61	P60/P61 as programming interface
	P53/P54	P53/P54 for programming port
OS testing	Enable	OS testing enable (detect all pins)
	Disable	OS testing disable (only detect programming pins)
Power-on time selection (see notes)	Fast power-on	Capacitance between power ground ≤ 50uF
	Slow power-on	50uF ≤ Capacitance between power ground ≤ 470uF

16. Instruction Set

Instruction	Instruction Action	Flag
ADD A,R	A+R→A	Z,C,DC
ADD R,A	A+R→R	Z,C,DC
AND A,R	A&R→A	Z
AND R,A	A&R→R	Z
CLRA	0→A	Z
CLR R	0→R	Z
INVA R	/R→A	Z
INV R	/R→R	Z
DA	A register adjusted to BCD value	C
DECA R	R-1→A	Z
DEC R	R-1→R	Z
DJA R	R-1→A, skip if zero	-
DJ R	R-1→R, skip if zero	-
INCA R	R+1→A	Z
INC R	R+1→R	Z
IJA R	R+1→A, skip if zero	-
IJ R	R+1→R, skip if zero	-
MOV R,A	A→R	-
MOV A,R	R→A	Z
MOV R,R	R→R	Z
OR A,R	A∨R→A	Z
OR R,A	A∨R→R	Z
SUB A,R	R-A→A	Z,C,DC
SUB R,A	R-A→R	Z,C,DC
XOR A,R	A⊕R→A	Z
XOR R,A	A⊕R→R	Z
BTC R,b	0→R(b)	-
BTS R,b	1→R(b)	-
JBTC R,b	if R(b)=0, skip	-
JBTS R,b	if R(b)=1, skip	-
LCR R	R(n)→R(n+1),R(7)→C, C→R(0)	C
LCA R	R(n)→A(n+1),R(7)→C, C→A(0)	C

RCR R	R(n)→R(n-1),R(0)→C, C→R(7)	C
RCA R	R(n)→A(n-1),R(0)→C, C→A(7)	C
SWAP R	R(0-3) ⇔ R(4-7)	-
SWAPA R	R(0-3)→A(4-7),R(4-7)→A(0-3)	-
ADD A,k	A+k→A	Z,C,DC
AND A,k	A&k→A	Z
MOV A,k	k→A	-
OR A,k	A∨k→A	Z
SUB A,k	k-A→A	Z,C,DC
XOR A,k	A⊕k→A	Z
CALL k	PC+1→[SP], (Page,k)→PC	-
DI	Disable Interrupts	-
EI	Enable Interrupt	-
JMP k	K (Page,k)→PC	-
NOP	Empty instruction	-
RET	[Stack top]→PC	-
RETI	[Stack top]→PC, enable interrupt	-
RETL k	k→A,[Stack top]→PC	-
SLEEP	0→WDT, oscillator stops oscillating (sleep mode)	T,P
CWDT	0→WDT	T,P
TBRD R	Machine code bit 7～0 to ACC Machine code bit 15～8 to R (general-purpose register)	-

17. Electrical characteristics

17.1 Limit parameters

Operating temperature..... -40℃～85℃
Storage Temperature..... -40℃～125℃
Input Voltage..... Vss-0.3V～Vdd+0.5V
Output Voltage..... Vss-0.3V～Vdd+0.5V
Operating Voltage..... 1.8V-5.5V

17.2 DC Electrical Characteristics

(VDD =5V, Operating Temperature=25℃, unless otherwise specified)

Operating Characteristics

Symbol	Parameter		Minimum	Typical	Maximum	Unit	Condition
Fosc (SYSCK)	System Clock		-	32	-	MHz	Frequency value selected by option [IRC Frequency] selection (Tuning error ±3%)
			-	16	-	MHz	
			-	8	-	MHz	
			-	4	-	MHz	
			-	1	-	MHz	
Fcpu	Instruction Clock	2T/4T	-	-	8	MHz	VDD=3.0V～5.5V
		8T	-	-	4	MHz	VDD=2.3V～5.5V
		16T/32T	-	-	2	MHz	VDD=1.9V～5.5V
T PWRT	Power-on Reset Hold Time		-	350	-	μs	Independent PWRT Time
			Reset Time = WDT Overflow			ms	PWRT=WDT/2
T RST	External Reset Pulse		2	-	-	μs	25℃
T UIS	Three-in-One Module		2.4	-	-	V	25℃

Low Voltage Reset (LVR)

Symbol	Parameter Description	Minimum	Typical	Maximum	Unit
I LVR	Reset Current	-	0.6	-	μA
V LVR	LVR Threshold	-10%	1.8	+10 %	V
		- 10 %	1.9	+10 %	
		-10%	2.1	+10%	
		-10%	2.3	+10%	
		-15%	2.7	+15%	
		-15%	3.0	+15%	
		-15%	3.5	+15%	
		-15%	4.0	+15%	

Note: To avoid process fluctuations, please leave sufficient margin for the actual product

I/O port circuit

Symbol	Parameter		Minimum	Typical	Maximum	Unit	Condition
VIL	Low-level threshold		0	-	0.22*VDD	V	25℃
VIH	High-level threshold		0.51*VDD	-	VDD	V	25℃
I_{OH1}	Source current (LED port)	L0	7	8	10	mA	25℃, VDD=5V, VOH=4.4V
		L1	13	15	17		
		L2	22	24	25		
I_{OH2}	Source current	L0	13	15	17	mA	
		L1	25	26	27		
I_{OL}	Sink current	L0	26	31	34	mA	25℃, VDD=5V, VOL=0.6V
		L1(LED port)	51	56	60		
R_{PH}	Pull-up resistor		45	50	55	KΩ	25℃, VDD=5V
R_{PL}	Pull-down resistor		45	50	55	KΩ	25℃, VDD=5V

General ports: P50, P52～P57, P70～P71

LED ports: P51, P60～P67

Operating current (I DD)

Parameter	SYSCK	Typical value @ VDD 2.0V	3.0V	5.0V	Unit
Normal Mode (2T)	32 MHz	0.86	1.7	2.8	mA
	16 MHz	0.6	0.93	1.5	
	8 MHz	0.36	0.6	0.86	
	4 MHz	0.24	0.31	0.44	
	1 MHz	0.16	0.19	0.25	
	36 KHz	5.8	6.5	8.5	uA
Sleep mode (WDT off, LVR on)	-	0.2	0.3	0.6	uA
Sleep mode (WDT on, LVR on)	-	2.5	3	5	
Sleep mode (WDT off, LVR on, ADC on)	-	20	33	90	
Sleep mode (WDT off, LVR on, CMP on)	-	6	6.5	9	

MTP and EEPROM

Parameter		Mini value	Typical value	Max value	Unit	Condition
VDD-READ	MTP/EEPROM	1.8	-	5.5	V	25℃, FCPU≤8MHz
VDD-WRIT	MTP	2.1	-	5.5	V	25℃
	EEPROM	2.1	-	5.5	V	25℃
Endurance	MTP/EEPROM	-	10000	-	Times	25℃
Retention	MTP/EEPROM	-	10	-	Years	25℃
T_{WRIT} Fast Write Time	MTP/EEPROM	-	5.5	-	ms	25℃
T_{WRIT} Slow Write Time	MTP/EEPROM	-	9.5	-	ms	25℃
TERASE Erase Time	MTP/EEPROM	-	1.5	-	ms	25℃
IP/E Erase Current	MTP/EEPROM	-	0.9	-	mA	25℃, VDD=5.5V

17.3 AD Conversion Characteristics

(VDD =5V, VSS=0V, Operating Temperature=25℃)

Symbol	Parameter Description	Condition	Minimum	Typical	Maximum	Unit
V_{DD}	ADC Operating	-	2.5	-	5.5	V
I_{VDD}	ADC Operating	VDD=VREF=5V	-	90	-	uA
V_{AIN}	Analog Input	-	V_{SS}	-	V_{REF}	V
EXVREF	External	-	2.0	-	V_{DD}	V
V_{REF}	Reference voltage output	VBG, 2V, 3V, 4V	-	±1	±2	%
T_{AD}	Conversion clock cycle	VDD=2.5～5.5V	1	-	-	us
T_{CN}	AD conversion time	VDD=2.5～5.5V	-	16	-	T_{AD}
RN	Resolution	-	-	12	-	Bit
VDDmin	Minimum supply	-	-	VREF+0.5	-	V
E_{IL}	Integral Error	V_{DD}= V_{REF}= 5V	-	±8.0	-	LSB
E_{DL}	Differential		-	±4.0	-	LSB
E_{OFF}	Offset Error		-	±5.0	-	LSB
E_{GN}	Gain Error		-	±2.0	-	LSB

Note: The error is derived from evaluation and is not tested during production.

17.4 Comparator Characteristics

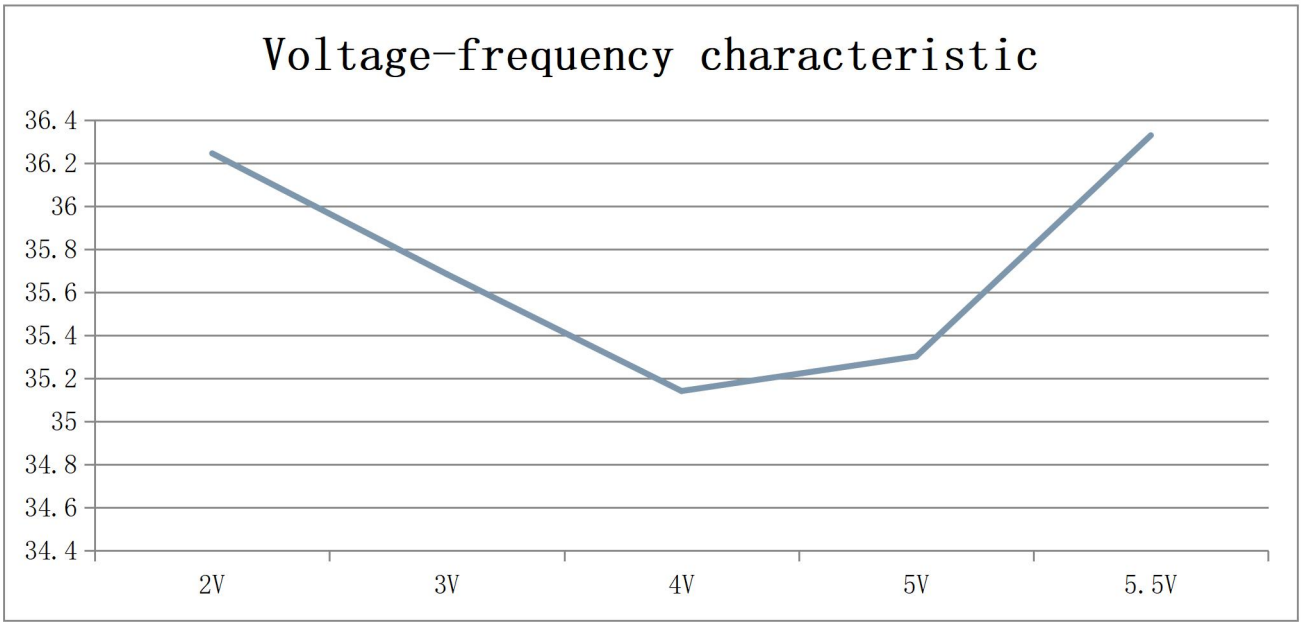
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{DD}	Operating Voltage	1.8	-	5.5	V	25℃
Vos	Comparator Hysteresis Voltage	-	10	-	mV	25℃
		-	40	-	mV	
		-	60	-	mV	
Tr	Comparator Response Time	-	50	-	ns	25℃, VDD=5V Digital filtering
		-	400	-	ns	
		-	60	-	us	25℃, VDD=5V Digital filtering

17.5 Characteristic curve diagram

The curves listed in this chapter are for design reference only. Some data provided may exceed the specified operating range of the chip. To ensure the normal operation of the chip, please strictly refer to the electrical characteristics description.

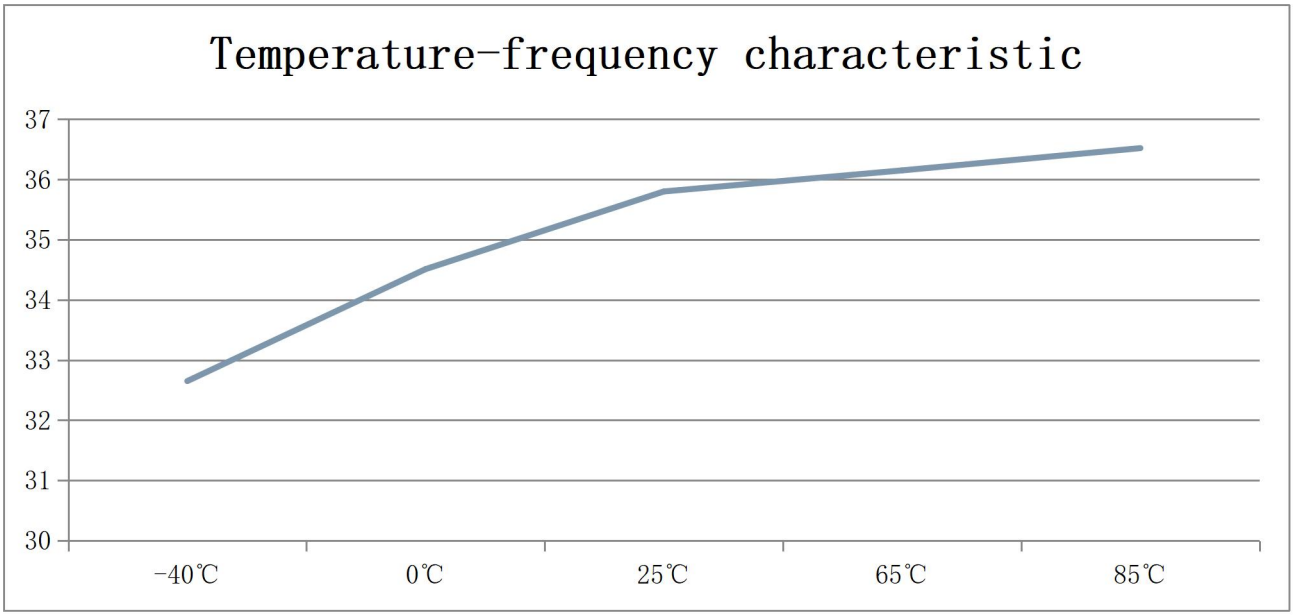
17.5.1 Internal Low-Speed Oscillator - Voltage-Frequency Characteristic Curve

Operating temperature at 25° C: (Unit: KHz)



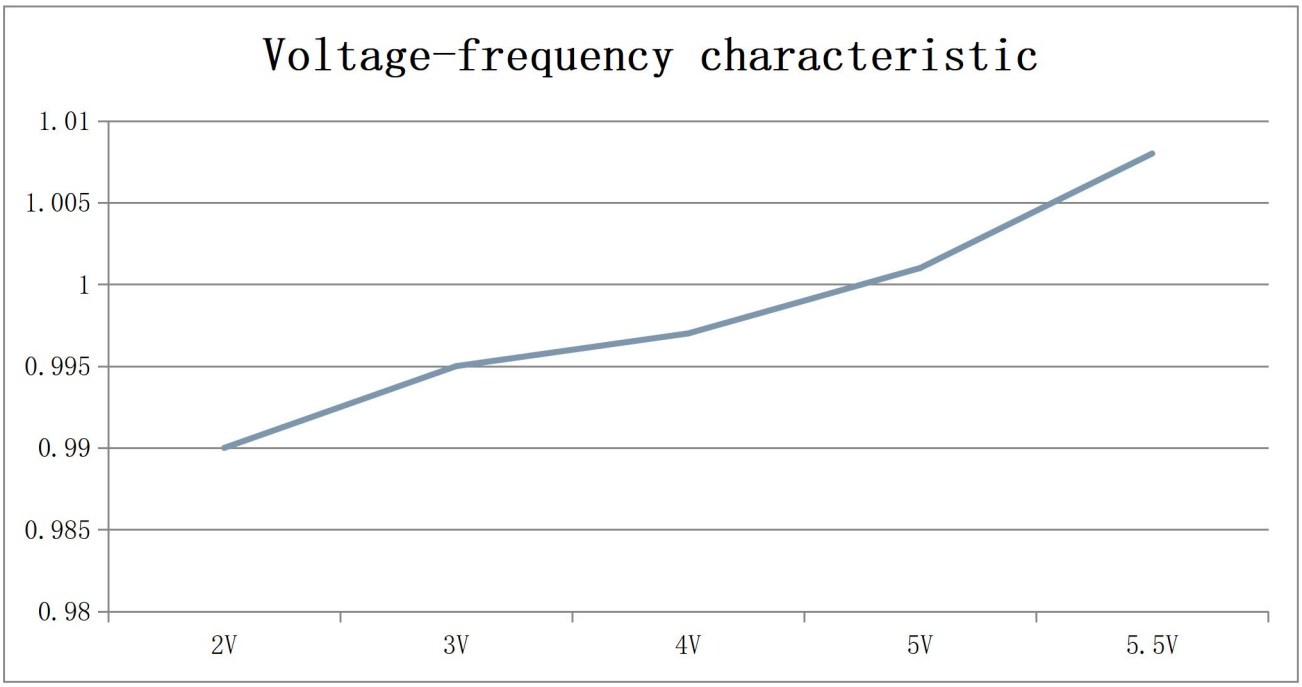
17.5.2 Internal low-speed oscillator - frequency-temperature characteristic curve

Operating voltage at 5V: (Unit: KHz)



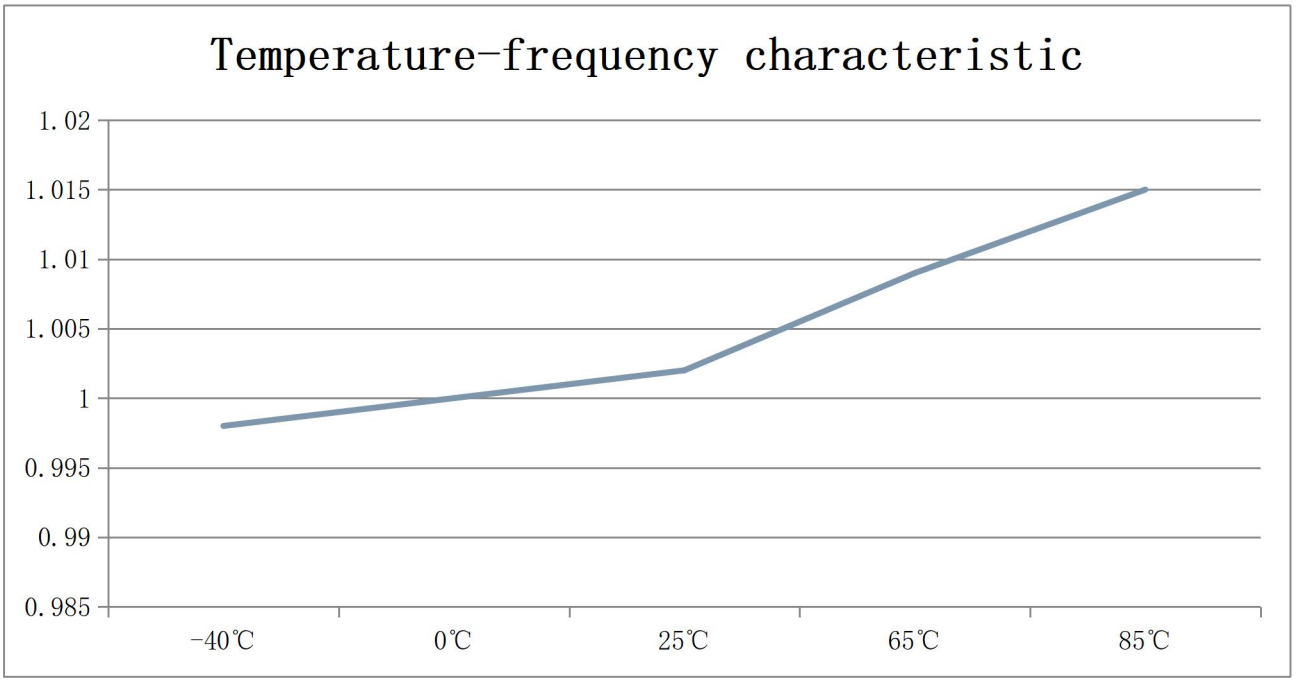
17.5.3 Internal 1MHz RC oscillator - frequency-voltage characteristic curve

Operating temperature at 25℃ conditions: (Unit MHz)



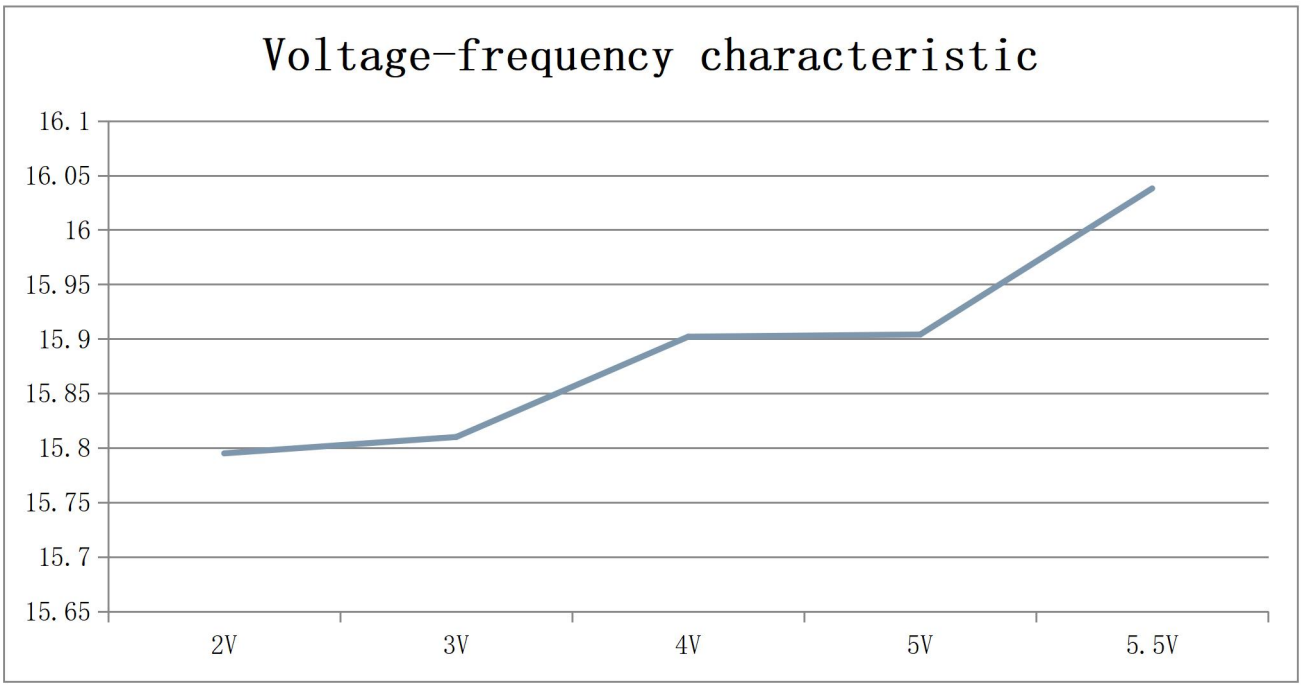
17.5.4 Internal 1MHz RC Oscillator - Temperature Frequency Characteristic Curve

Operating voltage under 5V conditions: (Unit MHz)



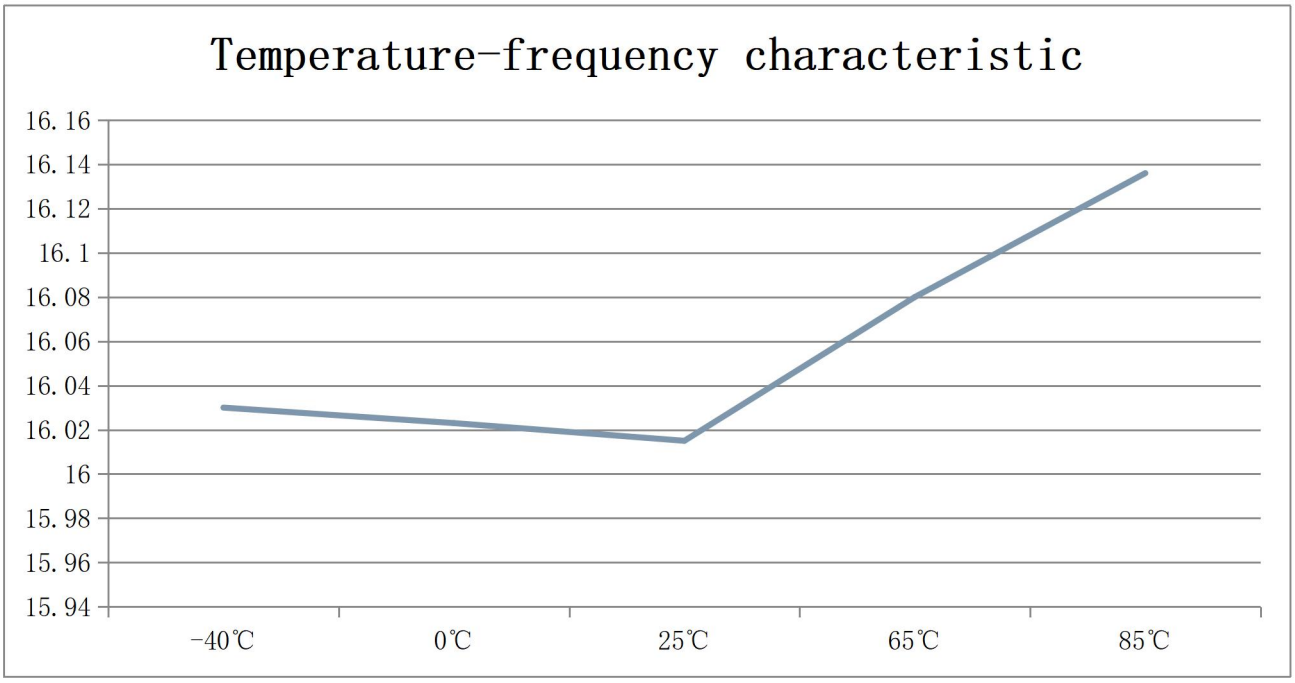
17.5.5 Internal 16MHz RC Oscillator - Frequency Characteristics Curve

Operating temperature at 25℃ conditions: (Unit MHz)



17.5.6 Internal 16MHz RC Oscillator - Temperature Frequency Characteristic Curve

Operating voltage under 5V conditions: (Unit MHz)



17.6 IHRC Frequency Trimming Parameter Description

Parameter descriptions are for reference only and may have deviations.

IHRCCAL Trimming Value (Hexadecimal)	Frequency (MHz)	Trimming Deviation (IHRCCAL=0x7F)
00	7.8685	-51.27%
01	7.8989	-51.08%
02	7.9306	-50.88%
03	7.9615	-50.69%
04	7.9946	-50.48%
05	8.0244	-50.30%
06	8.0567	-50.10%
07	8.0900	-49.89%
08	8.1230	-49.69%
09	8.1554	-49.49%
0A	8.1911	-49.27%
0B	8.2221	-49.08%
0C	8.2612	-48.83%
0D	8.2928	-48.64%
0E	8.3260	-48.43%
0F	8.3594	-48.23%
10	8.3979	-47.99%
11	8.4313	-47.78%
12	8.4694	-47.54%
13	8.5057	-47.32%
14	8.5400	-47.11%
15	8.5790	-46.87%
16	8.6136	-46.65%
17	8.6503	-46.42%
18	8.6891	-46.18%
19	8.7255	-45.96%
1A	8.7629	-45.73%
1B	8.8015	-45.49%
1C	8.8443	-45.22%
1D	8.8817	-44.99%
1E	8.9246	-44.73%
1F	8.9603	-44.50%
20	9.0002	-44.26%
21	9.0346	-44.04%
22	9.0782	-43.77%
23	9.1206	-43.51%
24	9.1629	-43.25%
25	9.2062	-42.98%
26	9.2536	-42.69%
27	9.2929	-42.44%
28	9.3373	-42.17%

29	9.3862	-41.87%
2A	9.4265	-41.62%
2B	9.4737	-41.32%
2C	9.5194	-41.04%
2D	9.5634	-40.77%
2E	9.6137	-40.46%
2F	9.6657	-40.13%
30	9.7111	-39.85%
31	9.7610	-39.54%
32	9.8052	-39.27%
33	9.8555	-38.96%
34	9.9056	-38.65%
35	9.9545	-38.35%
36	10.0069	-38.02%
37	10.0607	-37.69%
38	10.1097	-37.38%
39	10.1618	-37.06%
3A	10.2126	-36.75%
3B	10.2720	-36.38%
3C	10.3227	-36.07%
3D	10.3786	-35.72%
3E	10.4337	-35.38%
3F	10.4836	-35.07%
40	10.5419	-34.71%
41	10.6021	-34.34%
42	10.6584	-33.99%
43	10.7153	-33.63%
44	10.7758	-33.26%
45	10.8314	-32.91%
46	10.8925	-32.54%
47	10.9519	-32.17%
48	11.0149	-31.78%
49	11.0798	-31.38%
4A	11.1415	-30.99%
4B	11.2065	-30.59%
4C	11.2811	-30.13%
4D	11.3397	-29.77%
4E	11.4024	-29.38%
4F	11.4741	-28.93%
50	11.5460	-28.49%
51	11.6136	-28.07%
52	11.6864	-27.62%
53	11.7510	-27.22%
54	11.8237	-26.77%
55	11.8957	-26.32%

56	11.9714	-25.85%
57	12.0446	-25.40%
58	12.1222	-24.92%
59	12.1995	-24.44%
5A	12.2718	-23.99%
5B	12.3573	-23.46%
5C	12.4258	-23.04%
5D	12.5138	-22.50%
5E	12.5884	-22.03%
5F	12.6776	-21.48%
60	12.7655	-20.94%
61	12.8476	-20.43%
62	12.9325	-19.90%
63	13.0183	-19.37%
64	13.1138	-18.78%
65	13.2061	-18.21%
66	13.2976	-17.64%
67	13.3926	-17.05%
68	13.4878	-16.46%
69	13.5799	-15.89%
6A	13.6794	-15.28%
6B	13.7778	-14.67%
6C	13.8836	-14.01%
6D	13.9823	-13.40%
6E	14.0871	-12.75%
6F	14.1931	-12.09%
70	14.3019	-11.42%
71	14.4097	-10.75%
72	14.5217	-10.06%
73	14.6339	-9.36%
74	14.7487	-8.65%
75	14.8661	-7.93%
76	14.9850	-7.19%
77	15.1078	-6.43%
78	15.2292	-5.68%
79	15.3525	-4.91%
7A	15.4803	-4.12%
7B	15.6073	-3.34%
7C	15.7431	-2.49%
7D	15.8757	-1.67%
7E	16.0069	-0.86%
7F	16.1458	0.00%
80	14.7633	-8.56%
81	14.8206	-8.21%
82	14.8799	-7.84%

83	14.9406	-7.46%
84	14.9875	-7.17%
85	15.0587	-6.73%
86	15.1219	-6.34%
87	15.1816	-5.97%
88	15.2429	-5.59%
89	15.3056	-5.20%
8A	15.3653	-4.83%
8B	15.4271	-4.45%
8C	15.4962	-4.02%
8D	15.5627	-3.61%
8E	15.6262	-3.22%
8F	15.6900	-2.82%
90	15.7579	-2.40%
91	15.8226	-2.00%
92	15.8758	-1.67%
93	15.9582	-1.16%
94	16.0252	-0.75%
95	16.0920	-0.33%
96	16.1644	0.11%
97	16.2341	0.55%
98	16.3050	0.99%
99	16.3822	1.46%
9A	16.4535	1.91%
9B	16.5289	2.37%
9C	16.6084	2.87%
9D	16.6874	3.35%
9E	16.7538	3.77%
9F	16.8327	4.25%
A0	16.9115	4.74%
A1	16.9946	5.26%
A2	17.1022	5.92%
A3	17.1442	6.18%
A4	17.2501	6.84%
A5	17.3241	7.30%
A6	17.4032	7.79%
A7	17.4754	8.23%
A8	17.5911	8.95%
A9	17.6619	9.39%
AA	17.7601	10.00%
AB	17.8608	10.62%
AC	17.9364	11.09%
AD	18.0114	11.55%
AE	18.1189	12.22%
AF	18.2237	12.87%

B0	18.3181	13.45%
B1	18.4032	13.98%
B2	18.4694	14.39%
B3	18.5649	14.98%
B4	18.6502	15.51%
B5	18.7591	16.19%
B6	18.8554	16.78%
B7	18.9598	17.43%
B8	19.0521	18.00%
B9	19.1623	18.68%
BA	19.2432	19.18%
BB	19.3453	19.82%
BC	19.4602	20.53%
BD	19.5515	21.09%
BE	19.6595	21.76%
BF	19.7762	22.49%
C0	19.8803	23.13%
C1	19.9999	23.87%
C2	20.1009	24.50%
C3	20.2071	25.15%
C4	20.3154	25.82%
C5	20.4301	26.54%
C6	20.5520	27.29%
C7	20.6728	28.04%
C8	20.8597	29.20%
C9	20.9218	29.58%
CA	21.0434	30.33%
CB	21.1664	31.10%
CC	21.2888	31.85%
CD	21.4206	32.67%
CE	21.5467	33.45%
CF	21.6666	34.19%
D0	21.7945	34.99%
D1	21.9343	35.85%
D2	22.0665	36.67%
D3	22.2033	37.52%
D4	22.3494	38.42%
D5	22.4765	39.21%
D6	22.6220	40.11%
D7	22.7328	40.80%
D8	22.9036	41.85%
D9	23.0364	42.68%
DA	23.1816	43.58%
DB	23.3294	44.49%
DC	23.4603	45.30%

DD	23.6235	46.31%
DE	23.7779	47.27%
DF	23.9420	48.29%
E0	24.1088	49.32%
E1	24.2740	50.34%
E2	24.4546	51.46%
E3	24.6332	52.57%
E4	24.7976	53.59%
E5	24.9741	54.68%
E6	25.1388	55.70%
E7	25.3200	56.82%
E8	25.4950	57.90%
E9	25.6810	59.06%
EA	25.8604	60.17%
EB	26.0300	61.22%
EC	26.2191	62.39%
ED	26.4211	63.64%
EE	26.6126	64.83%
EF	26.8000	65.99%
F0	27.0091	67.28%
F1	27.1812	68.35%
F2	27.3823	69.59%
F3	27.6009	70.95%
F4	27.7993	72.18%
F5	27.9843	73.32%
F6	28.2271	74.83%
F7	28.4457	76.18%
F8	28.6658	77.54%
F9	28.9211	79.12%
FA	29.1583	80.59%
FB	29.3971	82.07%
FC	29.5810	83.21%
FD	29.8559	84.91%
FE	30.1299	86.61%
FF	30.3641	88.06%

17.7 DAC voltage parameters

(VDD =5V, VSS=0V, Operating Temperature=25℃)

VREFCAL	Voltage/V	VREFCAL	Voltage/V	VREFCAL	Voltage/V	VREFCAL	Voltage/V
0x00	1.21	0x10	1.44	0x20	1.665	0x30	1.895
0x01	1.225	0x11	1.45	0x21	1.675	0x31	1.905
0x02	1.24	0x12	1.465	0x22	1.695	0x32	1.915
0x03	1.25	0x13	1.475	0x23	1.705	0x33	1.93
0x04	1.27	0x14	1.495	0x24	1.725	0x34	1.945
0x05	1.28	0x15	1.505	0x25	1.735	0x35	1.955
0x06	1.295	0x16	1.52	0x26	1.745	0x36	1.975
0x07	1.305	0x17	1.53	0x27	1.76	0x37	1.985
0x08	1.325	0x18	1.55	0x28	1.78	0x38	2.005
0x09	1.34	0x19	1.56	0x29	1.79	0x39	2.015
0x0A	1.35	0x1A	1.575	0x2A	1.805	0x3A	2.03
0x0B	1.365	0x1B	1.59	0x2B	1.815	0x3B	2.045
0x0C	1.38	0x1C	1.605	0x2C	1.835	0x3C	2.055
0x0D	1.39	0x1D	1.615	0x2D	1.845	0x3D	2.075
0x0E	1.405	0x1E	1.63	0x2E	1.86	0x3E	2.085
0x0F	1.42	0x1F	1.645	0x2F	1.875	0x3F	2.095

VREFCAL	Voltage/V	VREFCAL	Voltage/V	VREFCAL	Voltage/V	VREFCAL	Voltage/V
0x40	2.105	0x50	2.33	0x60	2.555	0x70	2.78
0x41	2.115	0x51	2.345	0x61	2.57	0x71	2.79
0x42	2.135	0x52	2.355	0x62	2.585	0x72	2.81
0x43	2.145	0x53	2.365	0x63	2.595	0x73	2.82
0x44	2.155	0x54	2.385	0x64	2.61	0x74	2.84
0x45	2.175	0x55	2.395	0x65	2.625	0x75	2.85
0x46	2.185	0x56	2.415	0x66	2.64	0x76	2.86
0x47	2.195	0x57	2.425	0x67	2.65	0x77	2.875
0x48	2.215	0x58	2.445	0x68	2.67	0x78	2.895
0x49	2.225	0x59	2.455	0x69	2.68	0x79	2.905
0x4A	2.245	0x5A	2.465	0x6A	2.695	0x7A	2.92
0x4B	2.255	0x5B	2.48	0x6B	2.71	0x7B	2.935
0x4C	2.275	0x5C	2.495	0x6C	2.725	0x7C	2.95
0x4D	2.285	0x5D	2.51	0x6D	2.735	0x7D	2.96
0x4E	2.295	0x5E	2.525	0x6E	2.75	0x7E	2.975
0x4F	2.315	0x5F	2.535	0x6F	2.765	0x7F	2.99

VREFCAL	Voltage/V	VREFCAL	Voltage/V	VREFCAL	Voltage/V	VREFCAL	Voltage/V
0x80	3	0x90	3.23	0xA0	3.455	0xB0	3.68
0x81	3.01	0x91	3.24	0xA1	3.47	0xB1	3.695
0x82	3.03	0x92	3.25	0xA2	3.485	0xB2	3.705
0x83	3.04	0x93	3.265	0xA3	3.495	0xB3	3.72
0x84	3.06	0x94	3.28	0xA4	3.51	0xB4	3.735
0x85	3.07	0x95	3.295	0xA5	3.52	0xB5	3.745
0x86	3.08	0x96	3.31	0xA6	3.535	0xB6	3.765
0x87	3.095	0x97	3.32	0xA7	3.55	0xB7	3.775
0x88	3.11	0x98	3.34	0xA8	3.57	0xB8	3.795
0x89	3.13	0x99	3.35	0xA9	3.58	0xB9	3.805
0x8A	3.14	0x9A	3.365	0xAA	3.595	0xBA	3.82
0x8B	3.15	0x9B	3.38	0xAB	3.605	0xBB	3.835
0x8C	3.17	0x9C	3.395	0xAC	3.625	0xBC	3.845
0x8D	3.18	0x9D	3.41	0xAD	3.635	0xBD	3.86
0x8E	3.2	0x9E	3.42	0xAE	3.65	0xBE	3.875
0x8F	3.21	0x9F	3.43	0xAF	3.66	0xBF	3.885

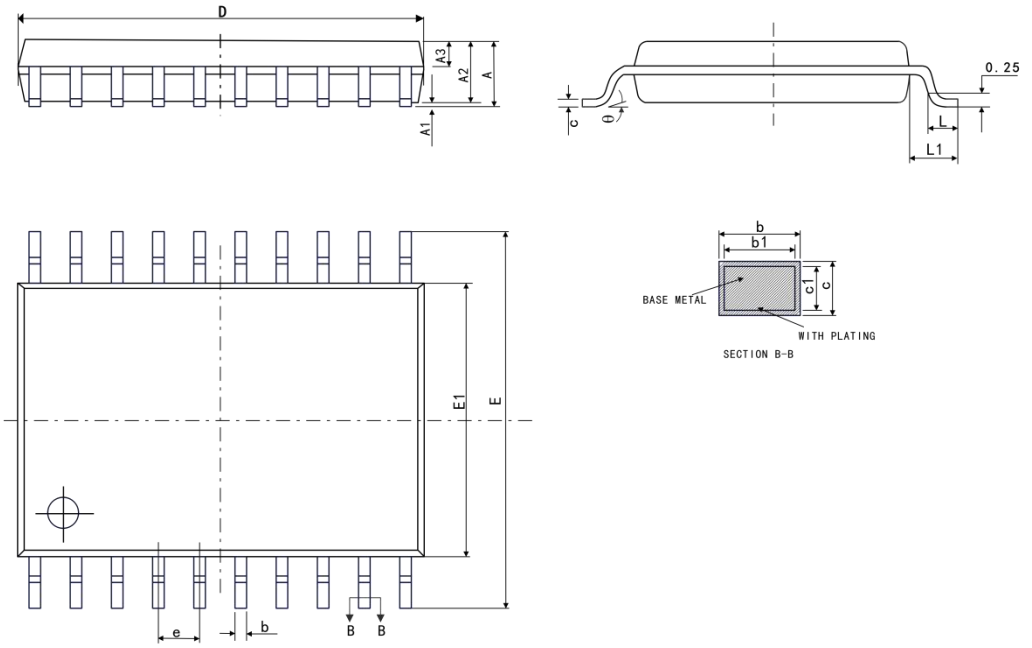
VREFCAL	Voltage/V	VREFCAL	Voltage/V	VREFCAL	Voltage/V	VREFCAL	Voltage/V
0xC0	3.895	0xD0	4.115	0xE0	4.345	0xF0	4.57
0xC1	3.905	0xD1	4.135	0xE1	4.355	0xF1	4.585
0xC2	3.92	0xD2	4.145	0xE2	4.37	0xF2	4.6
0xC3	3.935	0xD3	4.155	0xE3	4.385	0xF3	4.61
0xC4	3.945	0xD4	4.175	0xE4	4.405	0xF4	4.625
0xC5	3.965	0xD5	4.185	0xE5	4.415	0xF5	4.64
0xC6	3.975	0xD6	4.195	0xE6	4.425	0xF6	4.655
0xC7	3.985	0xD7	4.215	0xE7	4.44	0xF7	4.665
0xC8	4.005	0xD8	4.235	0xE8	4.455	0xF8	4.685
0xC9	4.015	0xD9	4.245	0xE9	4.47	0xF9	4.695
0xCA	4.035	0xDA	4.255	0xEA	4.485	0xFA	4.71
0xCB	4.045	0xDB	4.27	0xEB	4.495	0xFB	4.725
0xCC	4.06	0xDC	4.285	0xEC	4.515	0xFC	4.74
0xCD	4.075	0xDD	4.295	0xED	4.525	0xFD	4.75
0xCE	4.085	0xDE	4.315	0xEE	4.54	0xFE	4.765
0xCF	4.095	0xDF	4.325	0xEF	4.555	0xFF	4.775

Note: The DAC output voltage ranges from 3V to 5V with a tolerance of ±2%. The above data represents the average voltage value at 5V and is for reference only.

18. Package Dimensions

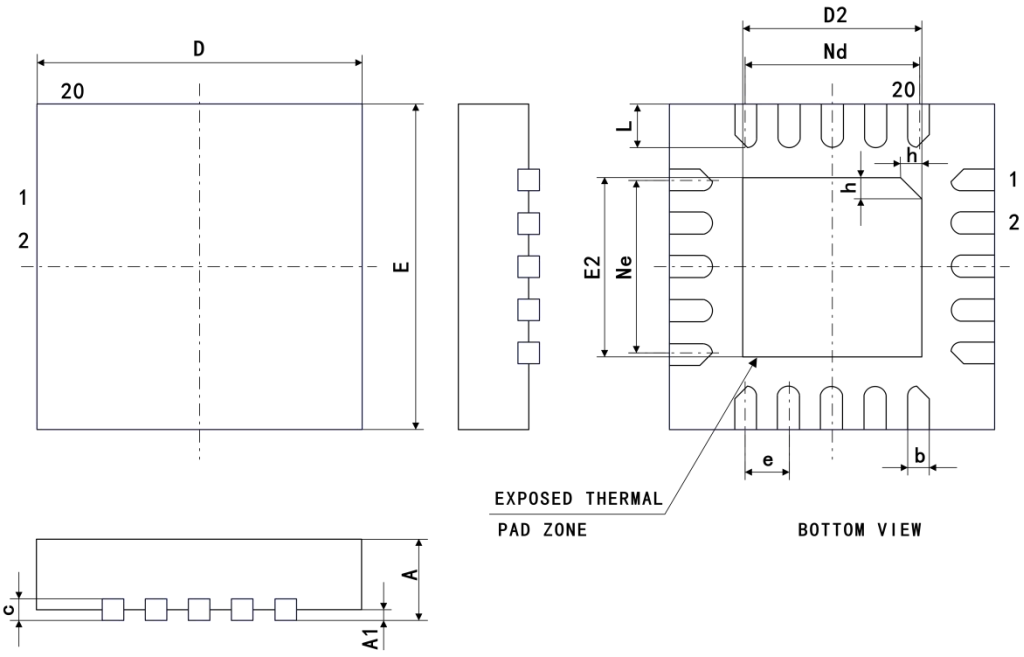
18.1 20PIN Package Dimensions

(Unit: mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	0.08	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

TSSOP20 Package Dimensions

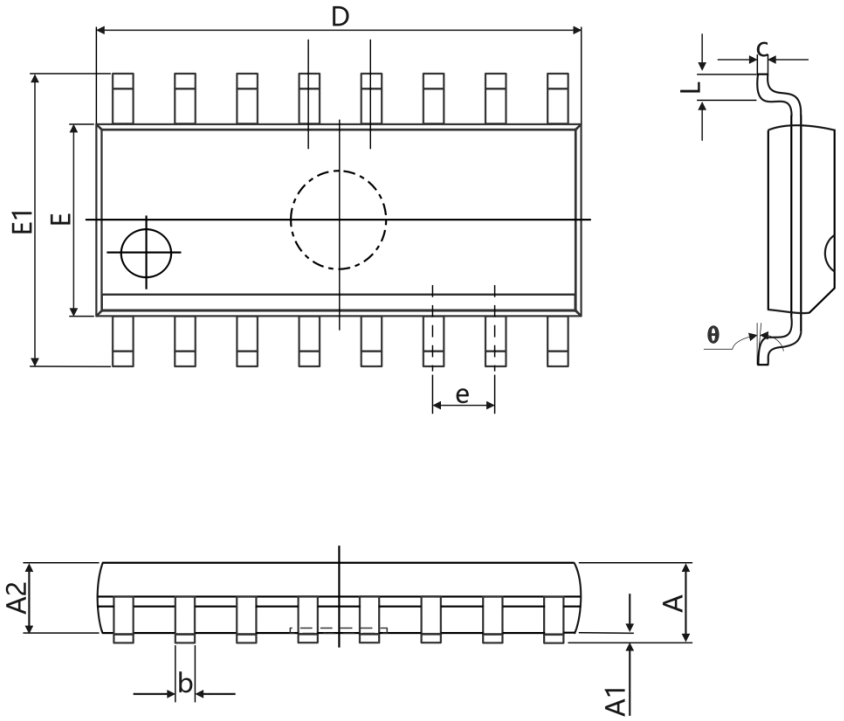


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸 (单位)	75*75		

QFN20 Package Dimensions

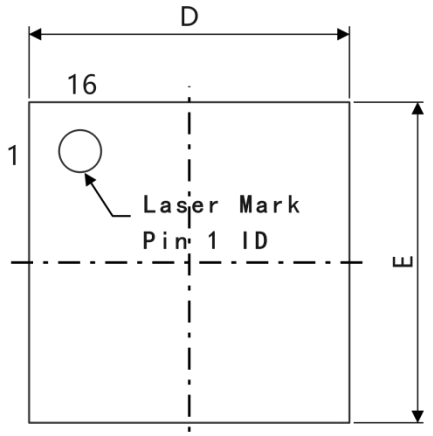
18.2 16PIN Package Dimensions

(Unit: mm)

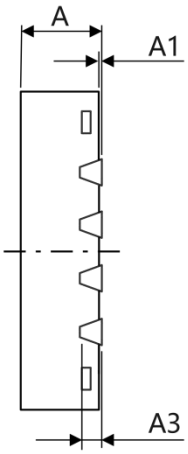


Symbol	Dimensions In Millimeter		Dimensions In Lnches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

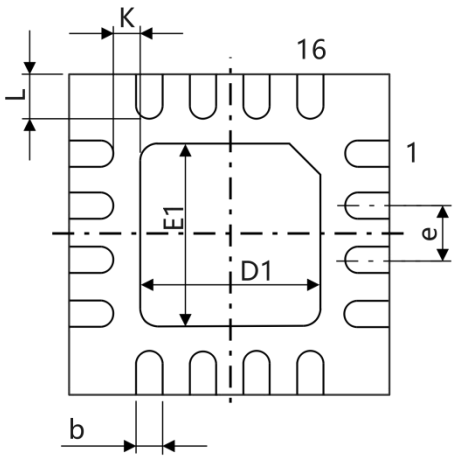
SOP16 Package Dimensions



Top View



Side View



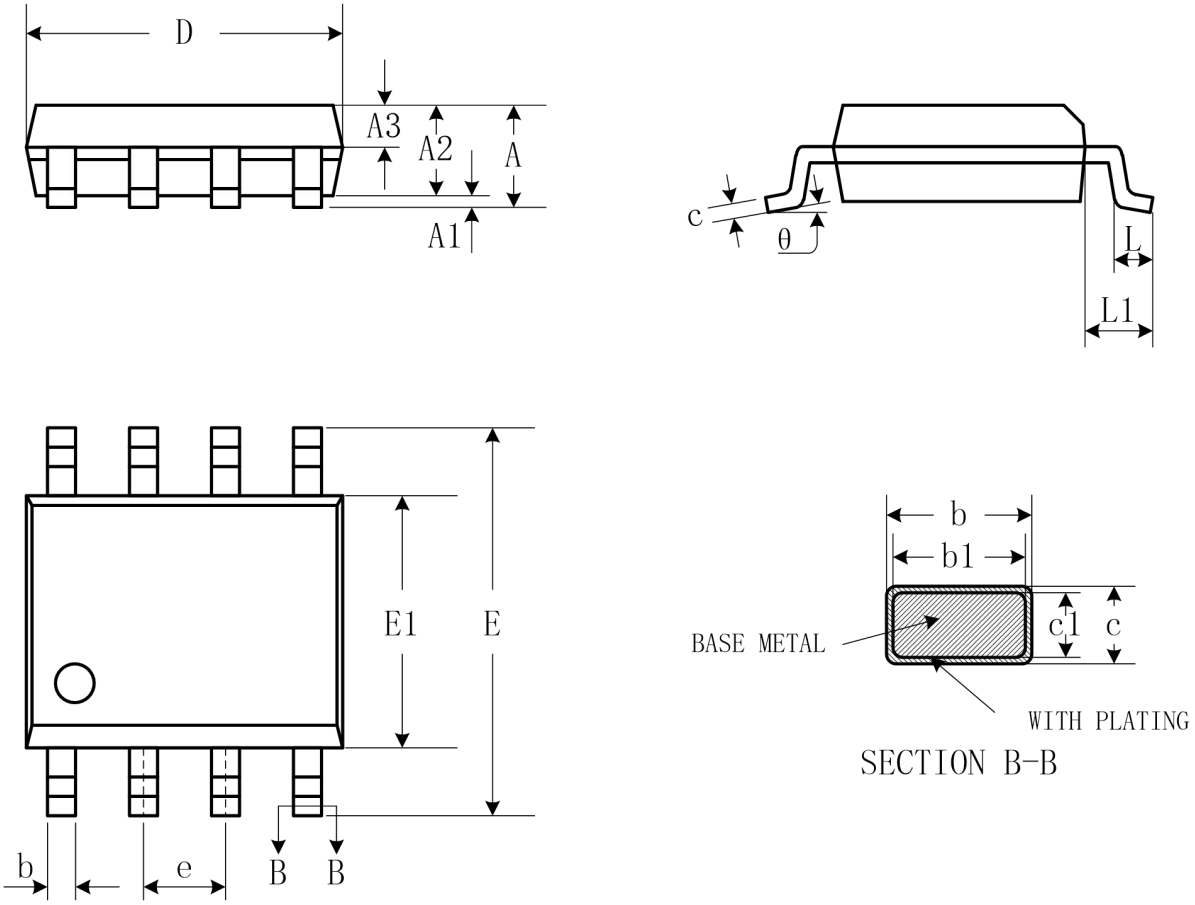
Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e	0.50TYP		
K	0.20	—	—
L	0.30	0.40	0.50

QFN16 Package Dimensions

18.3 8PIN package size

SOP8(Unit: mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	-	8°

SOP8 package dimensions