JZ8M4601

8-bit MTP microcontroller

User Data Manual

Version V1.6

Revision Record Description

Version	Revision Description	Remarks
V1.0	Initial Draft Version	
V1.1	Corrected Incorrect Parameters and Error Descriptions	
V1.2	Add QFN20 Package	
V1.3	Modify 8PIN Pinout, Add HXT and RTC Descriptions, Revise Error Descriptions	
V1.4	Revise Incorrect Parameters, Error Descriptions, Low-Speed Clock Frequency, Option Settings, and On-Board Programming Instructions	
V1.5	Update Logo Display, Standardize Register Definition Descriptions, Add Explanation for Option [Power-On Time Selection]	
V1.6	Revise Error Descriptions	

Notes:

1. The TC0 low-speed timing wake-up prescaler should be kept as small as possible. Before entering sleep again, a delay of half a TC0 clock cycle (1/ILRC * prescaler * (65536 - initial value) / 2) must be ensured to avoid repeated wake-ups;
2. When using the TC3 timer in 8-bit reload mode, the system clock SYSCK must not exceed 8MHz;
3. For zero-crossing signals, avoid using comparator ports and AD ports. It is recommended to use P53/P54, or select VDD in the option [IRC Oscillator Voltage Source Selection];
4. When the LCD duty cycle is 1/2, the COM ports can only use COM0/1; when it is 1/3, only COM0/1/2 can be used. Unused COM ports should be set as analog inputs and cannot be used for other functions;
5. When using UART, the serial port baud rate clock source must be used with a divider; using a division factor of 1 is prohibited;

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1. Chip Introduction

1.1 Functional Features

CPU Configuration

- 4K×16-Bit MTP ROM
- 128×16-Bit EEPROM
- 256×8-Bit SRAM
- 8-Level Stack Space
- 7-Level Programmable Voltage Reset (LVR)
  1.8V, 2.0V, 2.2V, 2.3V
  2.5V, 2.7V, 3.1V
- Operating current < 2mA (8MHz/5V)
- Operating current < 10uA (32KHz/3V)
- Sleep current < 3uA (sleep mode)

I/O Configuration

- 3 groups of 22 bidirectional IO ports:
  P5, P6, P7
- Wake-up ports: P5, P6, P7
- 22 programmable pull-up I/O pins
- 22 programmable pull-down I/O pins
- P60, P61, P62, P63 three-level drive options
- External interrupts:
  INT0: P50/P54 INT1: P60/P65

Operating Voltage

- Operating Voltage Range:
  V_{LVR} 2.2V～5.5V | Fcpu=0～8MHz
  V_{LVR} 1.8V～5.5V | Fcpu=0～4MHz
  V_{LVR} 1.8V～5.5V | Fcpu=0～2MHz

Operating Frequency Range

- External Crystal LXT with Optional Built-in Capacitors:
  14pF, 18pF, 25pF
- Internal IHRC Oscillator Circuit:
  32MHz / 16MHz / 6MHz / 1MHz
- Internal ILRC Oscillation Circuit:
  40KHz(5V)/41KHz(3V)
- Clock cycle division selection:
  2T, 4T, 8T, 16T, 32T

Peripheral modules

- 17-channel 12Bit ADC
- 16Bit real-time clock/counter TC0
- 16Bit timer counter TC3
- 6 channels 2 groups 12Bit-PWM (two pairs complementary)
- 1 UART (supports full-duplex and half-duplex)
- 1 comparator CMP
- P60/P64 pin level capture (4 capture modes)
- PWM-triggered AD sampling
- 2-channel RGB LED cascade controller (drives colorful lights)
- LCD driver: 4com*16seg (1/2 bias)
- LED driver: 4com*8seg

Interrupt sources

- TC0/TC3 overflow interrupt
- External interrupt 0/1
- P5/P6/P7 Port Input Change Interrupt
- ADC Conversion Complete Interrupt
- PWM1 Period Match/TC1 Timer Interrupt
- PWM4 Period Match/TC2 Timer Interrupt
- PWM2 Duty Cycle Match Interrupt
- CMP Status Change Interrupt
- Port Capture Interrupt
- UART Transmit/Receive Interrupt

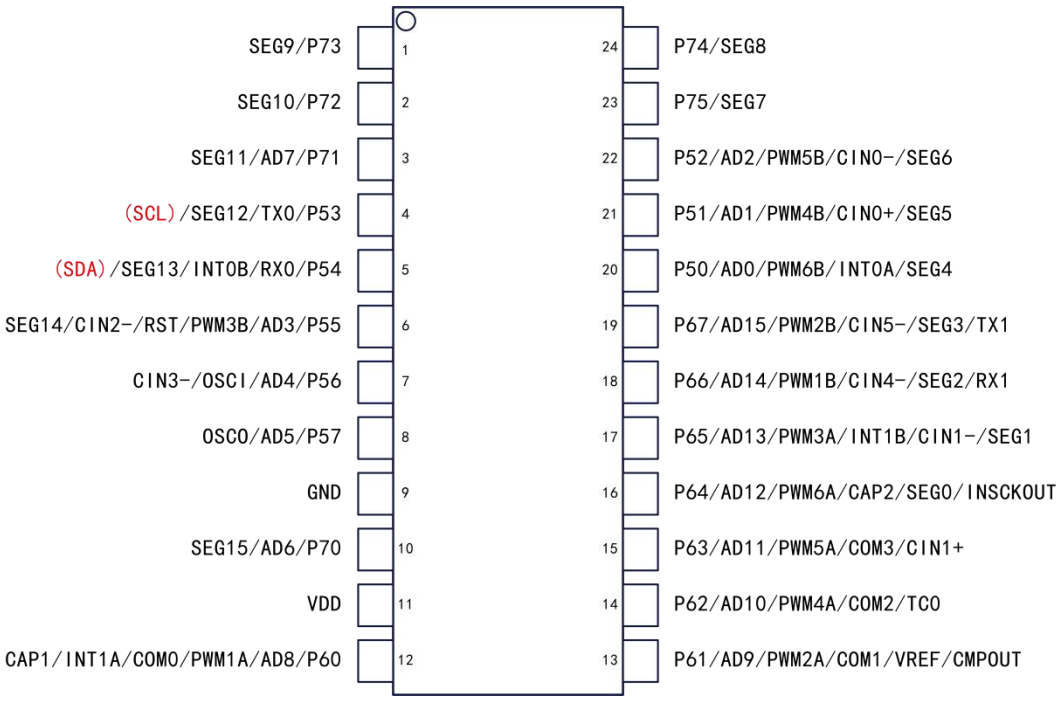
Features

- Programmable WDT timer
- Four operating mode switches
- Supports Type-C port upgrade, supports in-circuit programming

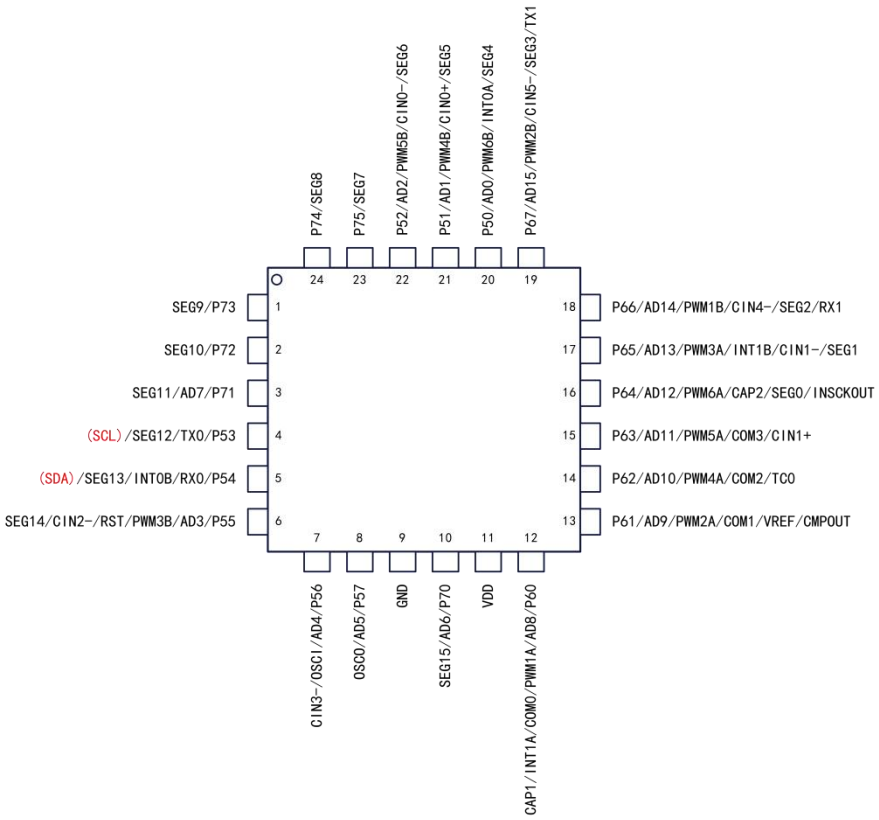
Package Types

- JZ8M4601-TSSOP24/QFN24
- JZ8M4601-TSSOP20/QFN20
- JZ8M4601-SOP16/QFN16/SOP8

1.2 Pin Assignment

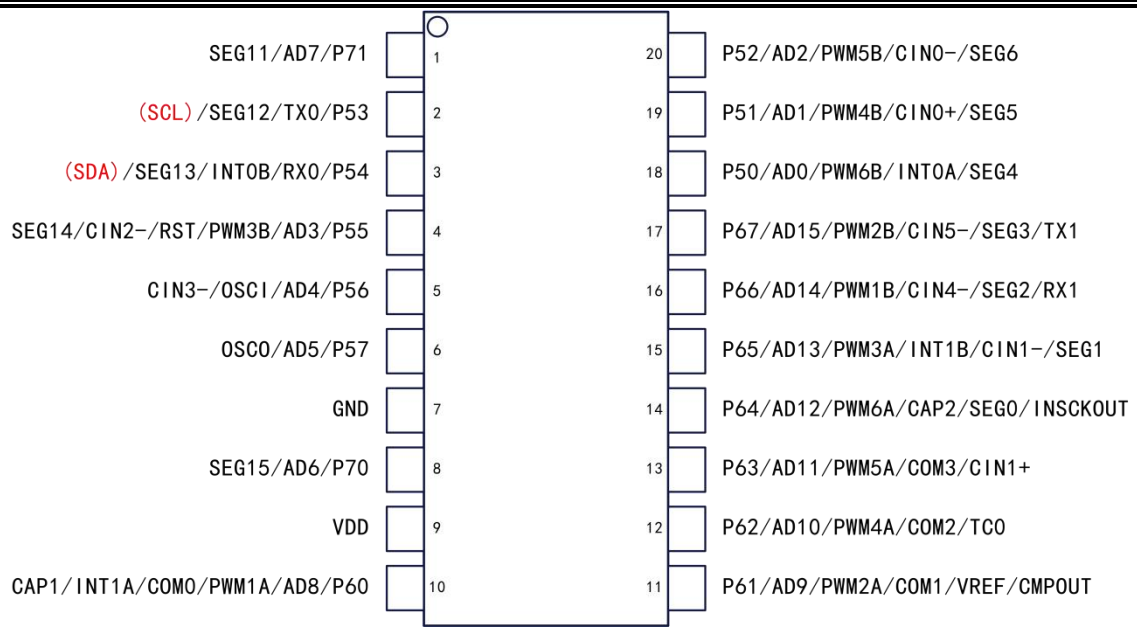


JZ8M4601-TSSOP24 Pin Diagram

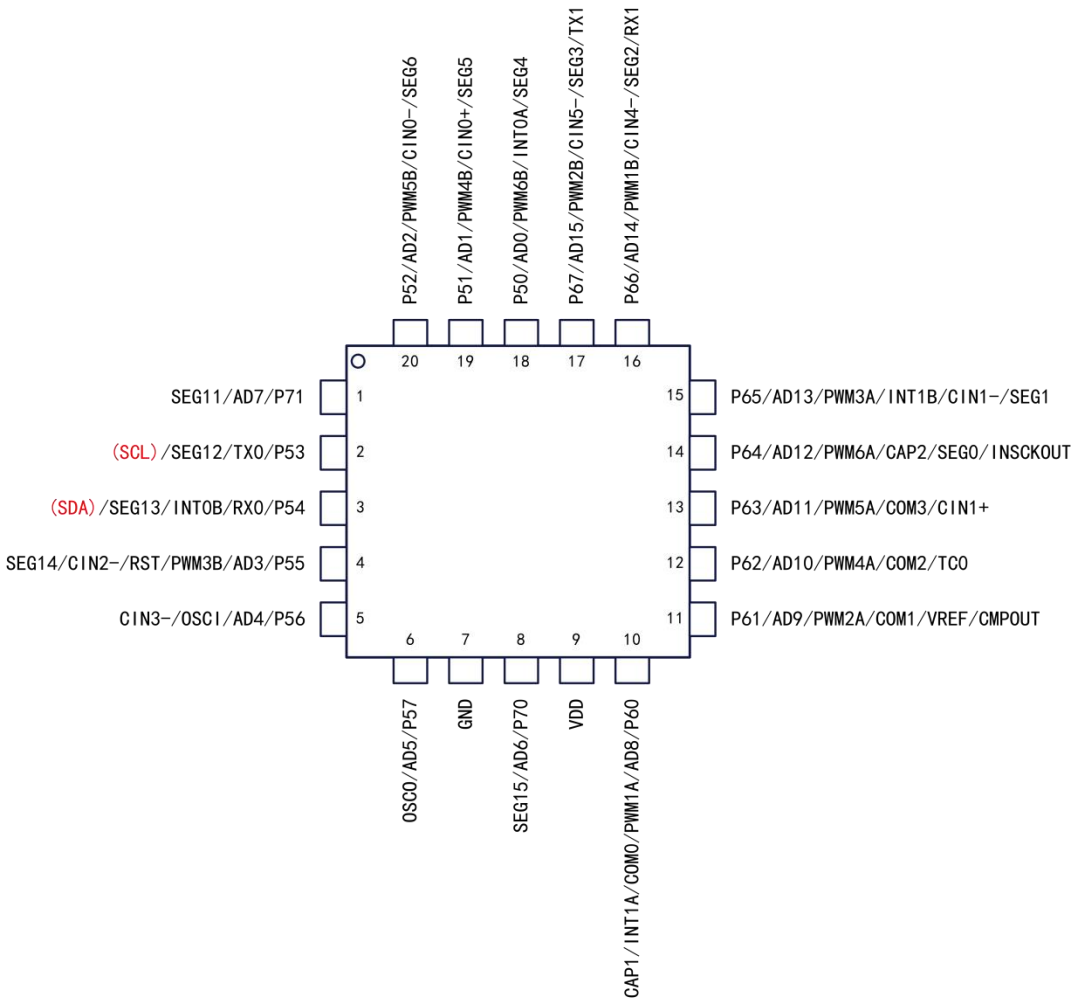


JZ8M4601-QFN24 Pinout Diagram

Note: The programming pins are P53 and P54 pins.

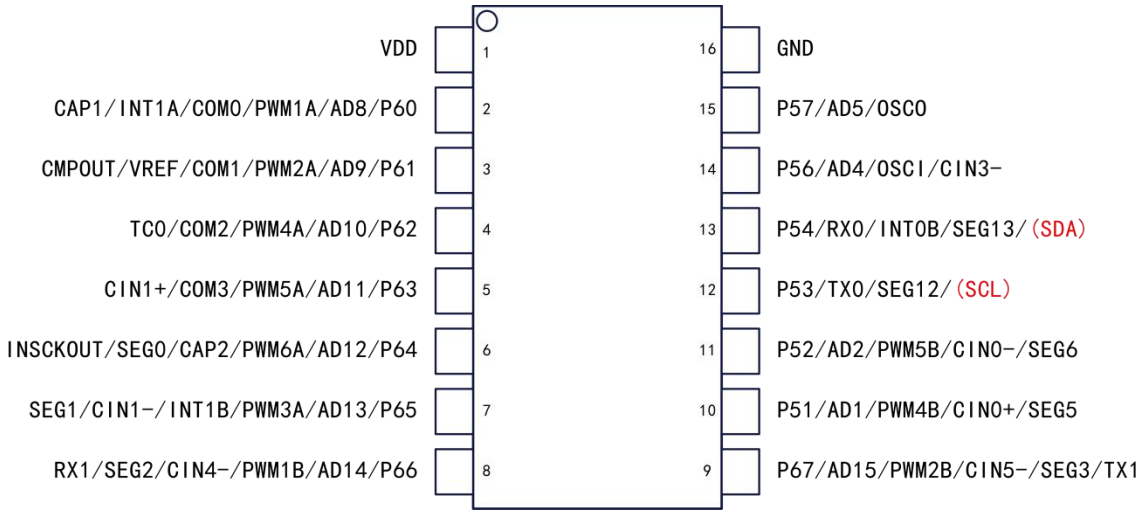


JZ8M4601-TSSOP20 Pin Diagram

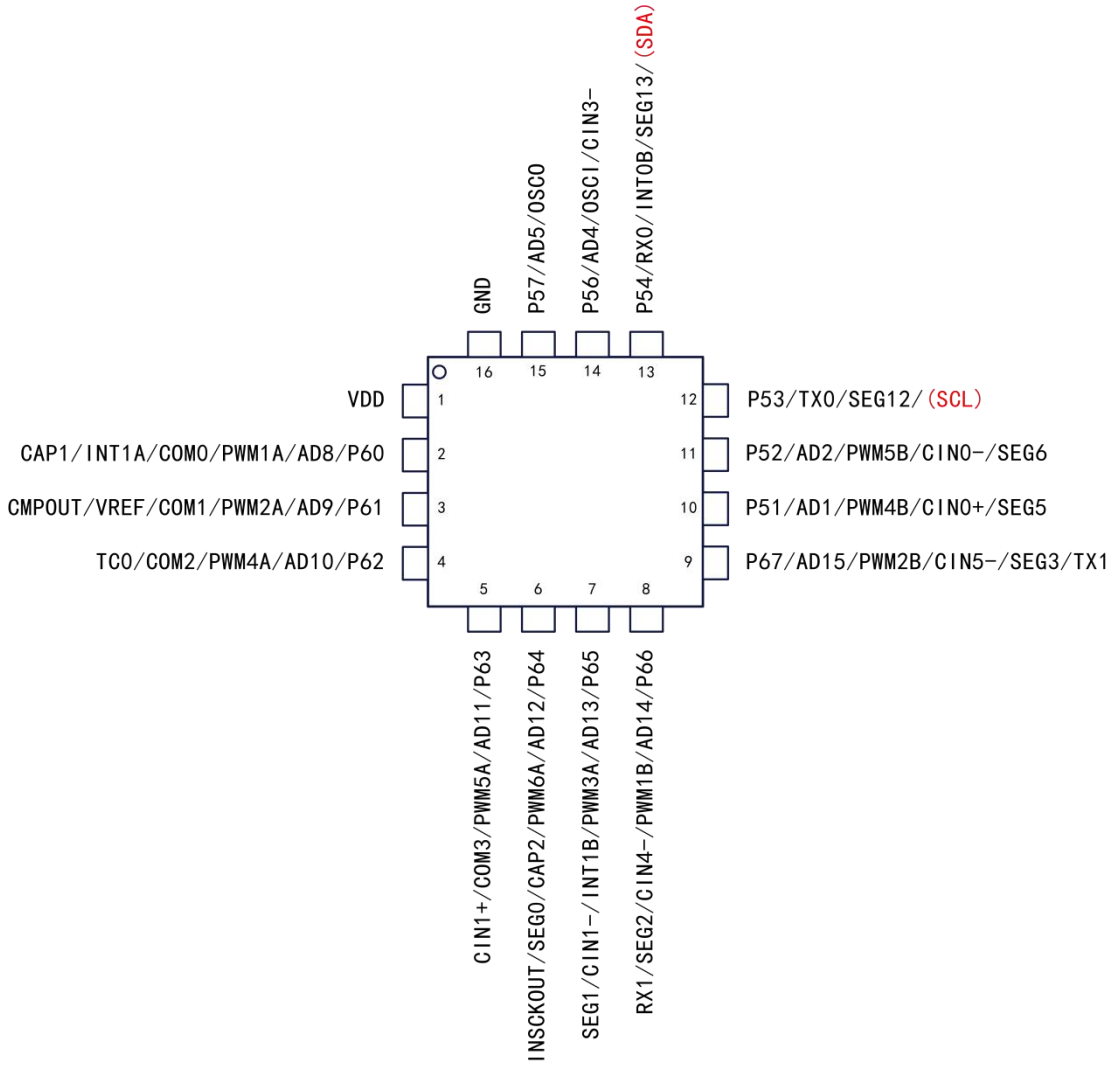


JZ8M4601-QFN20 Pin Diagram

Note: The programming pins are P53 and P54 pins.

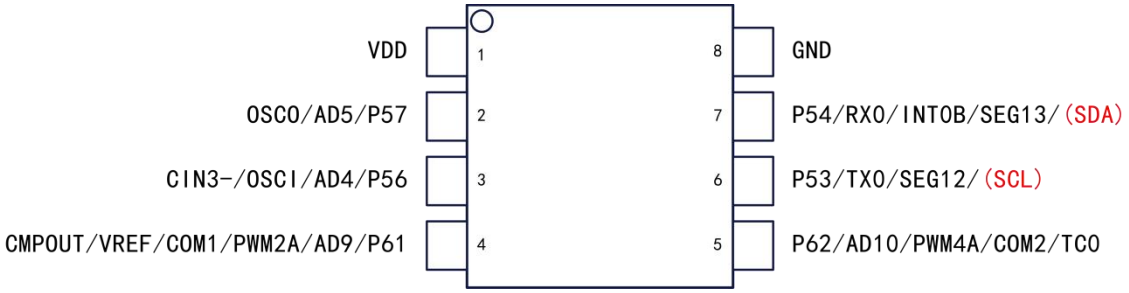


JZ8M4601-SOP16 Pin Diagram



JZ8M4601-QFN16 Pin Diagram

Note: The programming pins are P53 and P54 pins.



JZ8M4601-8PIN Pin Diagram

Note: The programming pins are P53 and P54 pins.

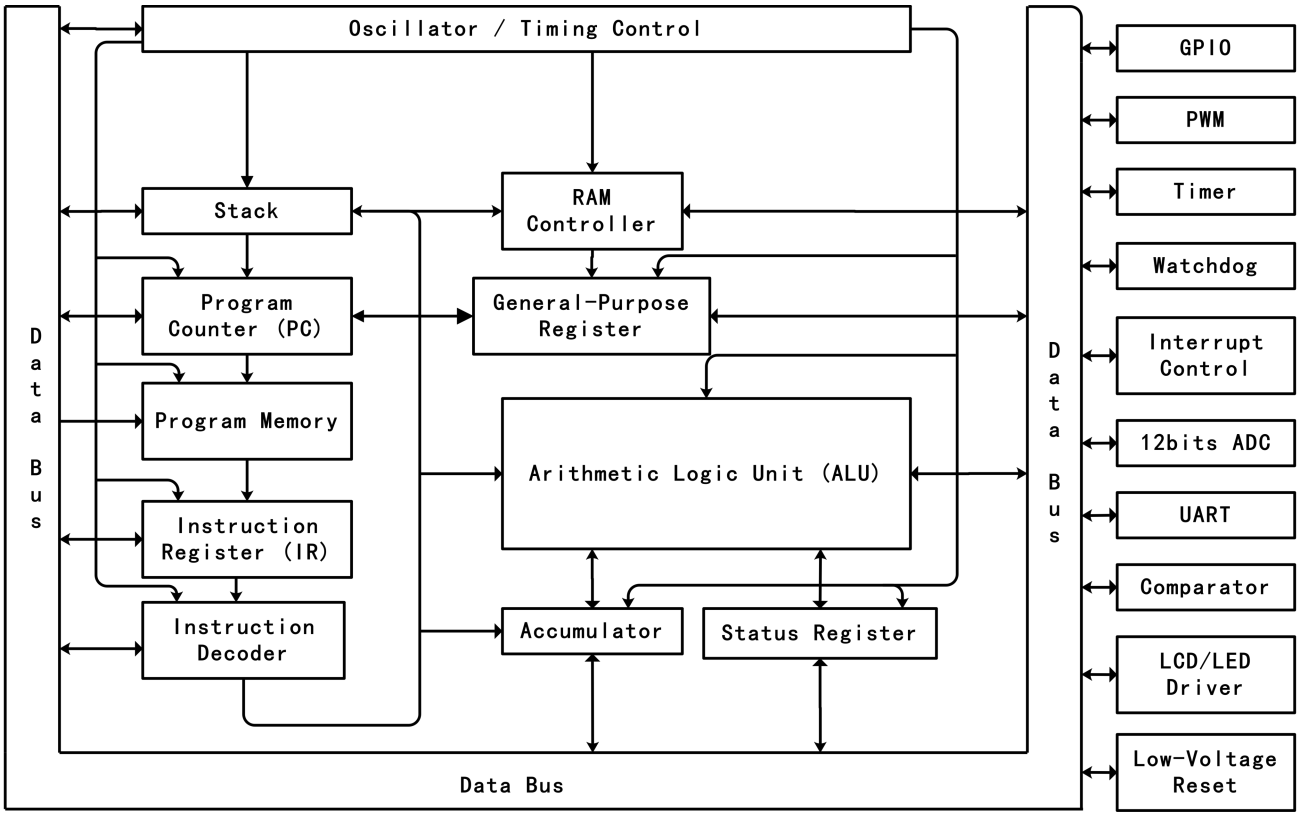
1.3 Pin Description

Number	Pin Name	I/O	Function Description
P50	P50	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN0	AN	Analog input channel
	PWM6B	O	PWM6B output
	INT0A	I	External interrupt INT0 input port
	SEG4	O	LCD drive SEG4 port
P51	P51	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN1	AN	Analog input channel
	PWM4B	O	PWM4B output
	CIN0+	AN	Comparator positive input port
	SEG5	O	LCD drive SEG5 port
P52	P52	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN2	AN	Analog input channel
	PWM5B	O	PWM5B output
	CIN0-	AN	Comparator negative input
	SEG6	O	LCD drive SEG6 port
P53	P53	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	TX0	O	UART communication transmission port
	SEG12	O	LCD drive SEG12 port
P54	P54	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	INT0B	I	External interrupt INT0 input port
	RX0	O	UART communication receive port
	SEG13	O	LCD drive SEG13 port
P55	P55	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN3	AN	Analog input channel
	PWM3B	O	PWM3B Output
	RST	I	External Reset Input Port
	CIN2-	AN	Comparator negative input
	SEG14	O	LCD Drive SEG14 Port
P56	P56	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN4	AN	Analog input channel
	OSCI	I	External crystal oscillator port
	CIN3-	AN	Comparator negative input
P57	P57	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN5	AN	Analog input channel
	OSCO	I	External crystal oscillator port

P60	P60	I/O	GPIO, programmable pull-up/pull-down, port wake-up, optional enhanced level 2 drive
	AIN8	AN	Analog input channel
	PWM1A	O	PWM1A output
	INT1A	I	External Interrupt 1 Input Port
	COM0	O	LCD Drive COM0 Port
	CAP1	I	Capture Input Port
P61	P61	I/O	GPIO, Programmable Pull-up/Pull-down, Port Wake-up, Optional Enhanced Level 2 Drive
	AIN9	AN	Analog input channel
	PWM2A	O	PWM2A Output
	COM1	O	LCD drive COM1 port
	VREF	AN	ADC external reference voltage input port
	CMPOUT	O	Comparator result output port
P62	P62	I/O	GPIO, Programmable Pull-up/Pull-down, Port Wake-up, Optional Enhanced Level 2 Drive
	AIN10	AN	Analog input channel
	PWM4A	O	PWM4A output
	COM2	O	LCD drive COM2 port
	TC0	I	TC0 external clock input port
P63	P63	I/O	GPIO, Programmable Pull-up/Pull-down, Port Wake-up, Optional Enhanced Level 2 Drive
	AIN11	AN	Analog input channel
	PWM5A	O	PWM5A output
	COM3	O	LCD drive COM3 port
	CIN1+	AN	Comparator positive input port
P64	P64	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN12	AN	Analog input channel
	PWM6A	O	PWM6A Output
	CAP2	I	Capture Input Port
	SEG0	O	LCD Drive SEG0 Port
	INSCKOUT	O	Internal Instruction Clock Frequency Output
P65	P65	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN13	AN	Analog input channel
	PWM3A	O	PWM3A Output
	INT1B	I	External Interrupt 1 Input Port
	CIN1-	AN	Comparator negative input
	SEG1	O	LCD Drive SEG1 Port
P66	P66	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN14	AN	Analog input channel
	PWM1B	O	PWM1B Output
	CIN4-	AN	Comparator negative input

	SEG2	O	LCD drive SEG2 port
	RX1	O	UART communication receive port
P67	P67	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN15	AN	Analog input channel
	PWM2B	O	PWM2B output
	CIN5-	AN	Comparator negative input
	SEG3	O	LCD drive SEG3 port
	TX1	O	UART communication transmission port
P70	P70	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN6	AN	Analog input channel
	SEG15	O	LCD drive SEG15 port
P71	P71	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN7	AN	Analog input channel
	SEG11	O	LCD drive SEG11 port
P72	P72	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	SEG10	O	LCD drive SEG10 port
P73	P73	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	SEG9	O	LCD drive SEG9 port
P74	P74	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	SEG8	O	LCD drive SEG8 port
P75	P75	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	SEG7	O	LCD drive SEG7 port
	VDD	--	Power Supply
	GND	--	Ground

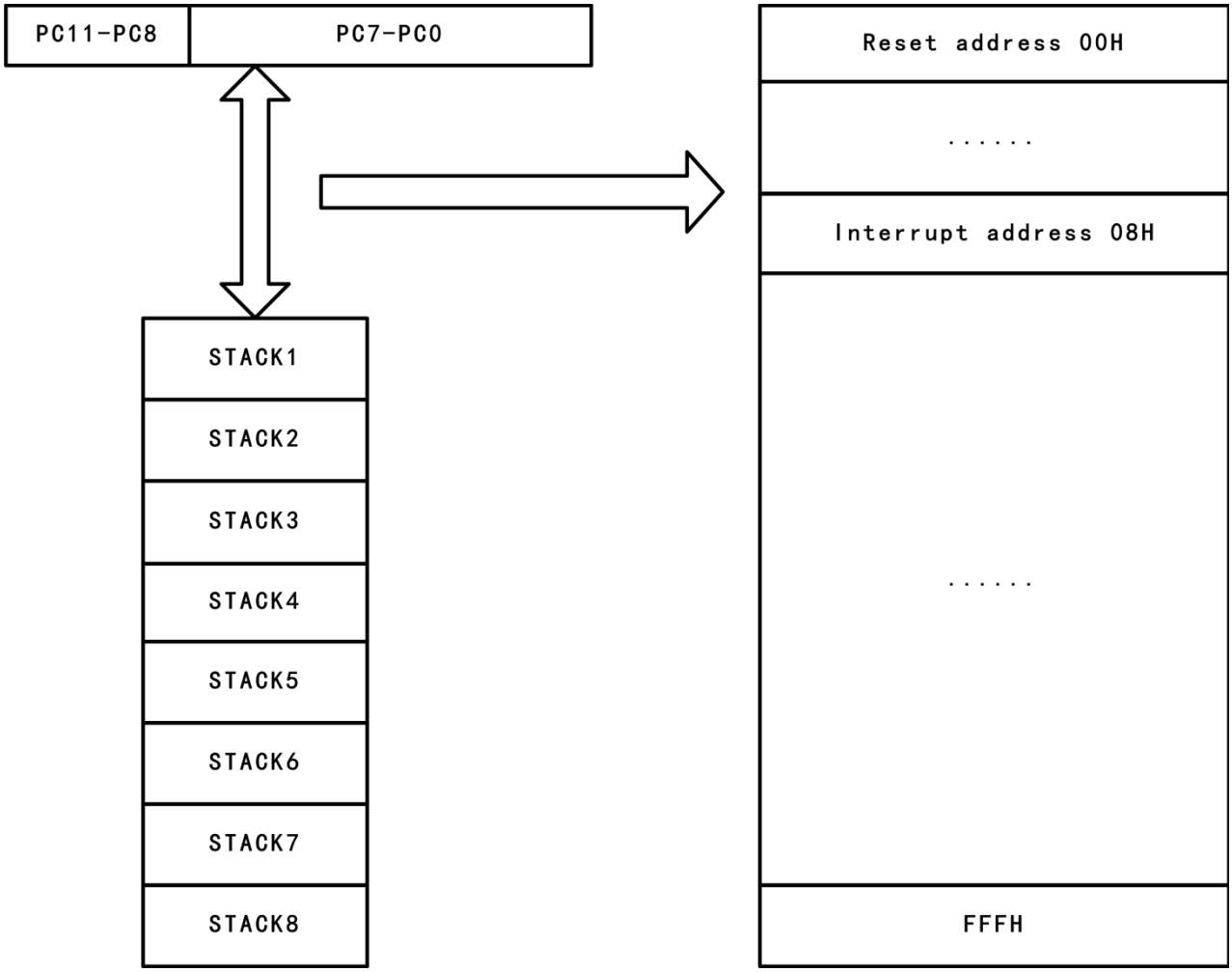
1.4 System Block Diagram



System Circuit Block Diagram

2. Memory Structure

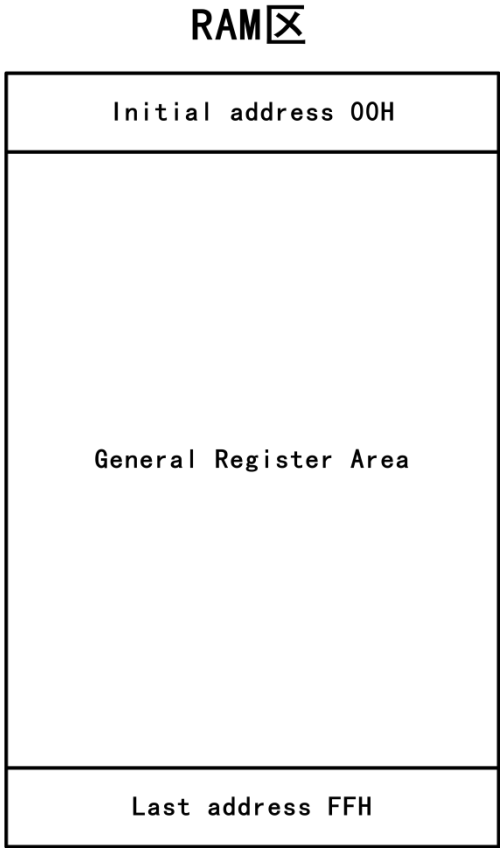
2.1 Program Memory Structure



Program Memory Structure Diagram

2.2 Data Storage Area

2.2.1 Data Storage Area Structure



Data Storage Area

2.2.2 Overview of Special Function Registers

Address	0X18_	0X19_	0X1A_	0X1B_	0X1C_	0X1D_	0X1E_	0X1F_
0	RSR	P5PH	P5P7AE	TC1CON	TC0CON		E2PCON	
1	PCH	P6PH	P6AE	TC1PRDL	TC0CL		E2PDATL	
2	PCL	P7PH		PWM1DTL	TC0CH		E2PDATH	
3	STATUS	P5PD	ADATH	PWM2DTL	TC0RL		SCON0	
4		P6PD	ADATL	PWM3DTL	TC0RH		SBUF	
5		P7PD	ADCON0	TC1PRDTH	CAPCON		SCON1	
6	TBRDH		ADCON1	PWM21DTH		INTE0	LCDCON	
7	TBRDL		ADCON2	PWMCON1		INTE1	SEGCON0	
8	CPUCON			TC2CON	TC3CON		SEGCON1	
9	IHRCCAL			TC2PRDL	TC3CL		LCDDB	
A (10)	P5			PWM4DTL	TC3CH	INTF0	CMPCON0	
B (11)	P6			PWM5DTL		INTF1	CMPCON1	
C (12)	P7	P5IWE		PWM6DTL				
D (13)	P5CON	P6IWE		TC2PRDTH				
E (14)	P6CON	P7IWE	EXINTCON	PWM54DTH				
F(15)	P7CON		WDTCON	PWMCON2				IAR

3. Function Description

3.1 Operation Registers

3.1.1 R180/RSR (RAM Select Register)

0X180	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSR	RSR<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

1. RSR<7:0> is used to select the SRAM address in indirect addressing mode (address range: 0X00 - 0XFF).

The RSR register is used together with the R1FF register to perform indirect addressing operations. The user can place the address corresponding to a certain SRAM into the RSR register, and then access the indirect addressing register R1FF; at this time, the address will point to the SRAM at the address in RSR.

2. RSR<3:0> is used in the LCD function to select the LCD RAM address, corresponding to selecting SEG0 - SEG15.

3.1.2 R181/PCH (Program Counter High Register)

0X181	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCH	-	-	-	-	PC<11:8>			
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

3.1.3 R182/PCL (Program Counter Low Register)

0X182	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCL	PC<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

The program counter (PC) is a pointer used to record the instruction that the CPU needs to process in each instruction cycle. During the CPU operation cycle, the PC advances the instruction pointer through the program memory, then increments the pointer by 1 to enter the next cycle. The JZ8M4601 has a 12-bit wide program counter (PC), with its low byte coming from the readable and writable PCL register, and the high byte coming from the readable PCH register.

The stack is used to record the instruction pointer for program returns. When a subroutine is called, the PC pushes the instruction pointer onto the stack. When a return instruction is executed, the stack sends the instruction pointer back to the PC to continue the original process. The JZ8M4601 has an 8-level stack, which occupies neither program memory space nor data memory space, and the stack pointer cannot be read or written.

The program counter (PC) and stack are detailed as follows:

(1) The PC register and built-in 8-level stack are both 12 bits wide, used for addressing the 4K×16Bit MTP ROM.

(2) Under normal circumstances, the PC increments by one; upon reset, all bits of the PC are cleared to zero.

(3) The "JMP" instruction allows direct loading of a 12-bit address, then pushes PC+1 onto the stack. Therefore, the JMP instruction allows the PC to jump to any position in the program.

(4) The "CALL" instruction allows loading the 12-bit address into the PC, then pushes PC+1 onto the stack. Therefore, the subroutine entry address can be located at any position in the program.

(5) When executing the "RET" instruction, the top data of the stack is sent to the PC.

(6) Executing the "ADD PCL,A" instruction adds a relative address to the current PC, with the ninth bit and above of the PC incrementing sequentially.

(7) Executing the "MOV PCL,A" instruction can load an address from the "A" register into the lower 8 bits of the PC, while the ninth bit and above of the PC remain unchanged.

(8) Any instruction that writes a value to PCL (except the "ADD PCL,A" instruction), such as "MOV PCL,A" or "BTC PCL,1", will keep the ninth and tenth bits of the PC unchanged.

(9) The stack operates like a circular buffer, meaning that after pushing 8 times, the data pushed on the 9th time will overwrite the data pushed on the 1st time, the data pushed on the 10th time will overwrite the data pushed on the 2nd time, and so on.

3.1.4 R183/STATUS (Status Flag Register)

0X183	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	RST	GIE	LXT_ERR	T	P	Z	DC	C
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	1	1	X	X	X

Bit<7>: RST – Reset or Wake-up Flag

0: Other Reset Types

1: Wake-up triggered by pin state change

Bit<6>: GIE – Interrupt enable flag bit

0: Masked by DIT instruction or hardware interrupt

1: Interrupt enabled by EIT/RTI instruction

Bit<5>: LXT_ERR – Low-speed crystal oscillator malfunction flag bit

0: Abnormal

1: Normal

Bit<4>: T-time overflow bit

0: WDT overflow

1: Execution of “SLEEP” and “CWDT” instructions or low-voltage reset

Bit<3>: P-Power Down Flag Bit

0: Execute the "SLEEP" instruction

1: Power-on reset or execute the "CWDT" instruction

The events affecting T/P are shown in the following table:

Type	RST	T	P
Power-on reset	0	1	1
Press RESET in working mode	0	Hold	Hold
RESET wake-up	0	1	0
WDT overflow in working mode	0	0	Hold
WDT overflow wake-up	0	0	0
Port input change wake-up	1	1	0
Execute CWDT instruction	Hold	1	1
Execute SLEEP instruction	Hold	1	0

Bit<2>: Z – Zero flag, set to "1" when the result of an arithmetic or logical operation is zero

0: When the result of an arithmetic or logical operation is not zero

1: When the result of an arithmetic or logical operation is zero

Bit<1>: DC – Auxiliary carry flag

0: No carry generated in the lower four bits during addition; / borrow generated in the lower four bits during subtraction

1: Carry generated in the lower four bits during addition; / no borrow generated in the lower four bits during subtraction

Bit<0>: C – Carry flag

0: When performing addition, no carry is generated in the high four bits; when performing subtraction, a borrow is generated in the high four bits.

1: When performing addition, there is a carry generated in the high four bits; when performing subtraction, there is no borrow generated in the high four bits.

3.1.5 R186/TBRDH (Table Lookup Pointer High Byte Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	PWM4_LEDEN	PWM1_LEDEN	-	-	RBIT<11:8>			
Read/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM4_LEDEN - PWM4 LED Cascade Control Bit

0: Disabled

1: Enabled

Bit<6>: PWM1_LEDEN - PWM1 LED Cascade Control Bit

0: Disabled

1: Enabled

Bit<3:0>: RBIT<11:8> - High 4 bits of the TBRD pointer address.

3.1.6 R187/TBRDL (Table Lookup Pointer Low Register)

0X187	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDL	RBIT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: RBIT<7:0> - Low 8 bits of the TBRD pointer address.

1. RBIT <7:0> is used to select the low 8 bits of the table lookup ROM address in table lookup mode.
2. RBIT <6:0> is used to select the EEPROM address in EEPROM read/write operations.

3.1.7 R188/CPUCON (CPU Mode Control Register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	ADCWE	TC3WE	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: ADCWE - ADC Wake-up Enable Bit

0: Wake-up Disabled

1: Wake-up Enabled, Can Wake Up from Idle Mode

Bit<6>: TC3WE - TC3 Wake-up Enable Bit

0: Wake-up Disabled

1: Wake-up Enabled, Can Wake Up from Idle Mode

Bit<5>: TC2WE - TC2 Wake-up Enable Bit

0: Wake-up Disabled

1: Wake-up Enabled, Can Wake Up from Idle Mode

Bit<4>: TC1WE - TC1 Wake-up Enable Bit

0: Wake-up Disabled

1: Wake-up Enabled, Can Wake Up from Idle Mode

Bit<3>: TC0WE - TC0 Wake-up Enable Bit

0: Wake-up Disabled

1: Wake-up Enabled, Can Wake Up from Idle Mode

Bit<2>: STPHX - High-Speed Clock Control Bit

0: High-speed clock operating normally

1: Stop high-speed clock

Bit<1>: CLKMD - System Clock Control Bit

0: System clock uses high-speed oscillator (IHRC) clock

1: System clock uses low-speed oscillator (ILRC) clock

When the system switches from high-speed mode to low-speed mode, first set CLKMD=1, then set STPHX=1;

When the system switches from low-speed mode to high-speed mode, it first sets STPHX=0, then sets CLKMD=0.

Bit<0>: IDLE - Idle mode enable bit

0: The system enters sleep mode when executing the SLEEP instruction

1: The system enters idle mode when executing the SLEEP instruction, and the system clock operates normally

TC0, TC3, and PWM can continue to operate using the system clock in idle mode if selected, and can wake up the system.

3.1.8 R189/IHRCCAL (IHRC Frequency Fine-tuning Register)

0X189	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IHRCCAL	IHRCCAL<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

IHRC High-Speed Oscillator Frequency Fine-tuning

3.1.9 R18A/P5 (P5 Data Register)

0X18A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5	P5<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 Port Data Control

3.1.10 R18B/P6 (P6 Data Register)

0X18B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6	P6<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 Port Data Control

3.1.11 R18C/P7 (P7 Data Register)

0X18C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7	-	-	P7<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P7 Port Data Control

3.1.12 R18D/P5CON (P5 Control Register)

0X18D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5CON	P5CON<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 Port Input/Output Control Bits:

0: Output

1: Input

3.1.13 R18E/P6CON (P6 Control Register)

0X18E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6CON	P6CON<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 Port Input/Output Control Bits:

0: Output

1: Input

3.1.14 R18F/P7CON (P7 Control Register)

0X18F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7CON	-	-	P7CON<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P7 Port Input/Output Control Bits:

0: Output

1: Input

3.1.15 R190/P5PH (P5 Pull-up Control Register)

0X190	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PH	P5PH<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 Port Pull-up Control Bits:

0: Enable

1: Disable

3.1.16 R191/P6PH (P6 Pull-up Control Register)

0X191	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PH	P6PH<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 Port Pull-up Control Bits:

0: Enable

1: Disable

3.1.17 R192/P7PH (P7 pull-up control register)

0X192	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7PH	-	-	P7PH<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P7 Port Pull-up Control Bits:

0: Enable

1: Disable

3.1.18 R193/P5PD (P5 pull-down control register)

0X193	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PD	P5PD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 Port Pull-down Control Bits:

0: Enable

1: Disable

3.1.19 R194/P6PD (P6 pull-down control register)

0X194	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PD	P6PD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 Port Pull-down Control Bits:

0: Enable

1: Disable

3.1.20 R195/P7PD (P7 pull-down control register)

0X195	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7PD	-	-	P7PD<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P7 Port Pull-down Control Bits:

0: Enable

1: Disable

3.1.21 R19C/P5IWE (P5 input change interrupt and wake-up enable register)

0X19C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5IWE	P5IWE<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 Port input change wake-up control bits:

0: Disabled

1: Enabled

3.1.22 R19D/P6IWE (P6 input change interrupt and wake-up enable register)

0X19D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6IWE	P6IWE <7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 port input change wake-up control bits:

0: Disabled

1: Enabled

3.1.23 R19E/P7IWE (P7 input change interrupt and wake-up enable register)

0X19E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7IWE	-	-	P7IWE <5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P7 port input change wake-up control bits:

0: Disabled

1: Enabled

3.1.24 R1A0/P5P7AE (P5P7 Analog Port Enable Register)

0X1A0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5P7AE	P7AE<1>	P7AE<0>	P5AE<7>	P5AE<6>	P5AE<5>	P5AE<2>	P5AE<1>	P5AE<0>
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5P7 Port Analog Port Selection Control Bit:

0: Port set as GPIO

1: Port set as Analog Input

3.1.25 R1A1/P6AE (P6 Analog Port Enable Register)

0X1A1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6AE	P6AE <7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 port Analog Port Selection Control Bits:

0: Port set as GPIO

1: Port set as Analog Input

3.1.26 R1A3/ADATH (ADC Data High 8-bit Register)

0X1A3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATH	ADAT< 11:4>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	X	X	X	X	X	X	X	X

Bit<7:0>: ADAT<11:4> - High 8 bits of ADC conversion result

3.1.27 R1A4/ADATL (ADC Data Low 8-bit Register)

0X1A4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATL	ADAT<7:0>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	X	X	X	X	X	X	X	X

Bit<7:0>: ADAT<7:0> - Lower 8 bits of ADC conversion result

3.1.28 R1A5/ADCON0 (ADC Control Register 0)

0X1A5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON0	ADPSR<1:0>		SHS<1:0>		ADAT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Reset Value	0	0	0	0	X	X	X	X

Bit<7:6>: ADPSR<1:0> - ADC clock division selection (Fosc is the system clock frequency)

ADPSR<1>	ADPSR<0>	ADC Clock
0	0	Fosc/16
0	1	Fosc/4
1	0	Fosc/64
1	1	Fosc/1

Bit<5:4>:SHS<1:0>- ADC Sample and Hold Time Selection

SHS<1>	SHS<0>	ADC Sample and Hold Time
0	0	ADC sampling hold time 2TAD
0	1	ADC sampling hold time 4TAD
1	0	ADC sampling hold time 8TAD
1	1	ADC sampling hold time 12TAD

Bit<3:0>: ADAT<11:8> - High 4 bits of AD conversion result

3.1.29 R1A6/ADCON1 (ADC Control Register 1)

0X1A6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON1	ADIS<4:0>					VREF<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	0

Bit<7:3>: ADIS<4:0> - AD input port selection

ADIS<4>	ADIS<3>	ADIS<2>	ADIS<1>	ADIS<0>	Channel Selection
0	0	0	0	0	AD0/P50
0	0	0	0	1	AD1/P51
0	0	0	1	0	AD2/P52
0	0	0	1	1	AD3/P55
0	0	1	0	0	AD4/P56
0	0	1	0	1	AD5/P57
0	0	1	1	0	AD6/P70
0	0	1	1	1	AD7/P71
0	1	0	0	0	AD8/P60
0	1	0	0	1	AD9/P61
0	1	0	1	0	AD10/P62
0	1	0	1	1	AD11/P63
0	1	1	0	0	AD12/P64
0	1	1	0	1	AD13/P65
0	1	1	1	0	AD14/P66
0	1	1	1	1	AD15/P67
1	0	0	0	0	0.254*VDD
1	1	1	1	1	Channel Test

Note: The channel test option is for factory testing only; users should avoid operating this option.

Bit<2:0>: VREF<2:0> - Reference Voltage Selection

VREF<2>	VREF<1>	VREF<0>	Reference Voltage
0	0	0	VBG Voltage 1.29V
0	0	1	Reference 2V

0	1	0	Reference 3V
0	1	1	Reference 4V
1	0	0	VDD
1	1	1	VREFS (P61)

3.1.30 R1A7/ADCON2 (ADC Control Register 2)

0X1A7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON2	ADRUN	ADEN	ADCGATE	CALI	SIGN	VOF<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: ADRUN

0: ADC no sampling or sampling ended

1: ADC starts sampling

Bit<6>: ADEN

0: ADC disabled (ADC turned off in sleep mode, otherwise power consumption occurs)

1: ADC enabled

Bit<5>: ADCGATE - ADC gate control selection bit

0: Gate disabled, enabled by software ADCEN

1: Gate enabled, ADC sampling enabled triggered by falling edge of PWM2 duty cycle

Bit<4>: CALI

0: ADC adjustment 0 calibration disabled

1: ADC adjustment 0 calibration enabled

Bit<3>: SIGN

0: ADC adjustment 0 negative polarity

1: ADC adjustment 0 positive polarity

Bit<2:0>: VOF<2:0> - ADC adjustment 0 calibration bits

VOF<2>	VOF<1>	VOF<0>	Calibration Amplitude
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

3.1.31 R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	EXINT1MS<1:0>		EXINTOMS<1:0>		EXINT1S	EXINTOS	TCOGATE	LXT_STEN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1

Bit<7:6>:EXINT1MS<1:0>- INT1 mode selection bits

EXINT1MS<1>	EXINT1MS<0>	EXINT1 mode selection
0	0	Function Disabled
0	1	Rising edge trigger
1	0	Falling edge trigger
1	1	Level change trigger

Bit<5:4>:EXINTOMS<1:0>- INTO mode selection bits

EXINTOMS<1>	EXINTOMS<0>	EXINTO mode selection
0	0	Function Disabled
0	1	Rising edge trigger
1	0	Falling edge trigger
1	1	Level change trigger

Bit<3>:EXINT1S- INT1 port selection bit

0: EXINT1 port selects P60

1: EXINT1 port selects P65

Bit<2>: EXINTOS - INTO port selection bit

0: EXINTO port selects P50

1: EXINTO port selects P54

Bit<1>: TCOGATE - TCO capture gate enable bit

0: Disabled

1: Enable gate, CMPOUT as capture source

Bit<0>: LXT_STEN - Low-speed crystal oscillator drive enhancement control bit

0: Disabled

1: Enable

3.1.32 R1AF/WDTCON (WDT, Wake-up Control Register)

0X1AF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	WDTPSR<1:0>		LVREN	UARTWE	CMPWE	EXINT1WE	EXINTOWE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Bit<7>: WDTE - WDT Enable Control

0: Disabled

1: Enabled

Bit<6:5>: WDTPSR<1:0> - WDT Prescaler Selection Bits:

WDTPSR<1>	WDTPSR<0>	WDT Prescaler Coefficient
0	0	1:2
0	1	1:4
1	0	1:8
1	1	1:16

Bit<4>: LVREN - LVR enable control

0: Enable

1: Disable

Bit<3>: UARTWE - UART wake-up enable bit

0: Disabled

1: Enabled

Bit<2>: CMPWE - CMP wake-up enable bit

0: Disabled

1: Enabled

Bit<1>: EXINT1WE - EXINT1 wake-up enable bit

0: Disabled

1: Enabled

Bit<0>: EXINT0WE - EXINT0 wake-up enable bit

0: Disabled

1: Enable

3.1.33 R1B0/TC1CON (TC1 Control Register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GATE	TC1CKS	TC1PTEN	TC1PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC1EN - TC1/PWM123 counter enable control

0: Disabled

1: Enabled

(If the TC1PRD register is set, TC1 resets when counting to the preset value and starts counting from 1)

Bit<6>: TC21EN - simultaneous enable control bit for TC1/PWM123 and TC2/PWM456 counters

0: Disabled

1: Enabled

Bit<5>: PWM1GATE - PWM1 Gate Output Enable Control Bit

0: No restriction

1: PWM1 output is controlled by the comparator result; when CMPOUT=0, the PWM waveform is output; when CMPOUT=1, PWM1 is held low

Bit<4>: TC1CKS - TC1 Clock Selection

0: Instruction clock

1: System clock

Bit<3:0>: TC1PTEN, TC1PSR2～TC1PSR0 Prescaler Selection Bits:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	WDT Prescaler Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.34 R1B1/TC1PRDL (TC1/PWM123 Period Low 8-bit Register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM2, PWM3) Period Low 8 bits

3.1.35 R1B2/PWM1DTL (PWM1 Duty Cycle Low 8-bit Register)

0X1B2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DTL	PWM1DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Lower 8 bits of PWM1 duty cycle

3.1.36 R1B3/PWM2DTL (PWM2 duty cycle lower 8-bit register)

0X1B3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2DTL	PWM2DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Lower 8 bits of PWM2 duty cycle

3.1.37 R1B4/PWM3DTL (PWM3 duty cycle lower 8-bit register)

0X1B4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM3DTL	PWM3DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM3 Duty Cycle Low 8 Bits

3.1.38 R1B5/TC1PRDTH (High 4 bits of TC1/PWM123 period and high 4 bits of PWM3 duty cycle register)

0X1B5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<11:8>				PWM3DT<11:8>			
Read/Write	R/W	R/W	R	R	R/W	R/W	R	R
Reset Value	0	0	0	0	0	0	0	0

High 4 bits of TC1 (PWM1, PWM2, PWM3) period and high 4 bits of PWM3 duty cycle

3.1.39 R1B6/PWM21DTH (High 4 bits of PWM21 duty cycle register)

0X1B6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM21DTH	PWM2DT<11:8>				PWM1DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

High 4 bits of PWM2 duty cycle, high 4 bits of PWM1 duty cycle

3.1.40 R1B7/PWMCON1 (PWM Control Register 1)

0X1B7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON1	BZ1EN	PWM3S	PWM2S	PWM1S	IPWM1EN	PWM3EN	PWM2EN	PWM1EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ1EN - BZ1 waveform output enable control bit

0: Disabled

1: Output BZ1 waveform (BZ1EN=1 and PWM1EN=0 must be set)

(Set P60/P66 as output to output BZ1 waveform)

Bit<6>: PWM3S - PWM3 output selection control bit

0: PWM3 outputs from P65

1: PWM3 outputs from P55

Bit<5>: PWM2S - PWM2 output selection control bit

0: PWM2 outputs from P61

1: PWM2 outputs from P67

Bit<4>: PWM1S - PWM output selection control bit

0: PWM1 outputs from P60

1: PWM1 output from P66

Bit<3>: IPWM1EN - IPWM1 enable control bit

0: Disabled

1: Output XOR of PWM2 and PWM3

(Output port selected based on PWM2EN (P64/P67) or PWM3EN (P55/P65))

Bit<2>: PWM3EN - PWM3 enable control bit

0: Disabled

1: Enable output of PWM3 waveform

(Corresponding port must be set as output to output PWM3 waveform)

Bit<1>: PWM2EN - PWM2 enable control bit

0: Disabled

1: Enable output of PWM2 waveform

(The corresponding port needs to be set as output to output the PWM2 waveform)

Bit<0>: PWM1EN - PWM1 enable control bit

0: Disabled

1: Enable output of PWM1 waveform

(The corresponding port needs to be set as output to output the PWM1 waveform, and BZ1EN=0)

3.1.41 R1B8/TC2CON (TC2 Control Register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC2EN - TC2/PWM456 counter enable control

0: Disabled

1: Enabled

Bit<6>: PWM4GATE<1> - PWM4 gate output enable control bit 1

0: No restriction

1: PWM4 output is controlled by external interrupt EXINT0; when EXINT0=1, PWM is output, otherwise low level is output

Bit<5>: PWM4GATE<0> - PWM4 gate output enable control bit 0

0: No restriction

1: PWM4 output is controlled by comparator result; when CMPOUT=0, PWM is output, when CMPOUT=1, PWM4 is low level

Bit<4>: TC2CKS - TC2 clock selection

0: Instruction clock

1: System clock

Bit<3:0>: TC2PTEN, TC2PSR2～TC2PSR0 prescaler selection bits:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 Prescaler Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.42 R1B9/TC2PRDL (TC2/PWM456 Period Low 8-bit Register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Low 8 bits of TC2 (PWM4, PWM5, PWM6) period

3.1.43 R1BA/PWM4DTL (PWM4 Duty Cycle Low 8-bit Register)

0X1BA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM4DTL	PWM4DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Low 8 bits of PWM4 duty cycle

3.1.44 R1BB/PWM5DTL (PWM5 Duty Cycle Low 8-bit Register)

0X1BB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM5DTL	PWM5DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Lower 8 bits of PWM5 duty cycle

3.1.45 R1BC/PWM6DTL (PWM6 duty cycle lower 8-bit register)

0X1BC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM6DTL	PWM6DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Lower 8 bits of PWM6 duty cycle

3.1.46 R1BD/TC2PRDTH (TC2/PWM456 period high 4 bits and PWM6 duty cycle high 4 bits register)

0X1BD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD <11:8>				PWM6DT<11:8>			
Read/Write	R/W	R/W	R	R	R/W	R/W	R	R
Reset Value	0	0	0	0	0	0	0	0

High 4 bits of the TC2 (PWM4, PWM5, PWM6) period and high 4 bits of the PWM6 duty cycle

3.1.47 R1BE/PWM54DTH (PWM54 High 4-bit Duty Cycle Register)

0X1BE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM54DTH	PWM5DT<11:8>				PWM4DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

High 4 bits of PWM5 duty cycle, high 4 bits of PWM4 duty cycle

3.1.48 R1BF/PWMCON2 (PWM Control Register 2)

0X1BF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON2	BZ2EN	PWM6S	PWM5S	PWM4S	IPWM4EN	PWM6EN	PWM5EN	PWM4EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ2EN - BZ2 waveform output enable control bit

0: Disabled

1: Output BZ2 waveform (requires setting BZ2EN=1, PWM4EN=0)

(P51/P62 must be set as output to output the BZ2 waveform)

Bit<6>: PWM6S - PWM6 output selection control bit

0: PWM6 outputs from P64

1: PWM6 output from P50

Bit<5>: PWM5S - PWM5 output selection control bit

0: PWM5 output from P63

1: PWM5 output from P52

Bit<4>: PWM4S - PWM4 output selection control bit

0: PWM4 output from P62

1: PWM4 output from P51

Bit<3>: IPWM4EN - IPWM4 enable control bit

0: Disabled

1: Output XOR of PWM5 and PWM6

(Output port selected according to PWM5EN (P52/P63) or PWM6EN (P50/P64))

Bit<2>: PWM6EN - PWM6 enable control bit

0: Disabled

1: PWM6 output waveform enable

(The corresponding port needs to be set as output to output the PWM6 waveform)

Bit<1>: PWM5EN - PWM5 enable control bit

0: Disabled

1: PWM5 output waveform enable

(The corresponding port needs to be set as output to output the PWM5 waveform)

Bit<0>: PWM4EN - PWM4 enable control bit

0: Disabled

1: PWM4 output waveform enable

(The corresponding port needs to be set as output to output the PWM4 waveform, and BZ2EN=0)

3.1.49 R1C0/TC0CON (TC0 Control Register)

0X1C0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CON	TC0EN	RTCS	TC0CKS<1:0>		TC0PTEN	TC0PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC0EN - TC0 timer count enable bit

0: Disable TC0

1: Enable TC0

Bit<6>: RTCS - RTC mode select bit

0: Disable RTC clock

1: Enable RTC clock

Bit<5:4>: TC0CKS<1:0>- TC0 signal source selection bits

00: System clock

01: ILRC clock (low-speed oscillator)

10: External input signal (P62), count on rising edge of signal

11: External input signal (P62), count on falling edge of signal

Bit<3>: TC0PTEN - Prescaler enable bit

0: Disable TC0 prescaler

1: Enable TC0 prescaler

Bit<2:0>: TC0PSR<2:0> - TC0 prescaler selection control bits:

TC0PSR<2>	TC0PSR<1>	TC0PSR<0>	TC0 Prescaler Coefficient
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.50 R1C1/TC0CL (TC0 low 8-bit count register)

0X1C1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CL	TC0C<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.51 R1C2/TC0CH (TC0 high 8-bit count register)

0X1C2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CH	TC0C<15:8>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.52 R1C3/TC0RL (TC0 reload low 8-bit register)

0X1C3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0RL	TC0R<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.53 R1C4/TC0RH (TC0 Reload High 8-bit Register)

0X1C4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0RH	TC0R<15:8>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.54 R1C5/CAPCON (Capture Control Register)

0X1C5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CAPCON	CAPEN	TC0MD	CAPEDGE	CAPS	CAPMD<1:0>		CAPTIME<1:0>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CAPEN - Capture Enable Bit

0: Disable TC0 capture function

1: Enable TC0 capture function

Bit<6>: TC0MD - TC0 Mode Select Bit

0: Auto-reload mode

1: Capture mode

Bit<5>: CAPEDGE - Capture Edge Select Bit

0: Capture starts on rising edge trigger

1: Capture starts on falling edge trigger

Bit<4>: CAPS - Capture Input Source Selection Bit (CAPS selection is invalid when TC0GATE=1)

0: P60

1: P64

Bit<3:2>: CAPMD<1:0> - Capture Mode Selection Bits

CAPMD<1>	CAPMD<0>	Capture Mode Selection
0	0	Mode 1
0	1	Mode 2
1	0	Mode 3
1	1	Mode Four

Capture Mode	Capture Mode Description
Mode 1	Periodic capture, selectable number of periods (1, 4, 8, 16)
Mode 2	Continuous capture of high and low levels
Mode 3	Level controls TC0 counting, selectable number of levels (1, 4, 8, 16)
Mode 4	Single level capture

Bit<1:0>: CAPTIME<1:0> - Capture count selection bits

CAPTIME<1>	CAPTIME<0>	Capture count value selection
0	0	1
0	1	4
1	0	8
1	1	16

3.1.55 R1C8/TC3CON (TC3 Control Register)

0X1C8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC3CON	TC3EN	TC3CKS	RELOAD	TC3HEN	TC3PTEN	TC3PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC3EN - TC3 Timer Count Enable Bit

0: Disable TC3

1: Enable TC3

Bit<6>: TC3CKS - TC3 Clock Source Selection Bit

0: System Clock (SYSCK)

1: Low-Speed Clock (ILRC)

Bit<5>: RELOAD - TC3 Reload Mode Selection Bit

0: TC3 is an 8/16-bit counter without reload function

1: TC3 is an 8-bit reloadable counter; the TC3CH register is the reload assignment register, keep TC3HEN=0

Note: When TC3 is in 8-bit reloadable counting mode and TC3CKS selects SYSCK, SYSCK must be ≤ 8MHz.

Bit<4>: TC3HEN - TC3 High 8-bit Counter Selection Bit

0: TC3 is an 8-bit counter

1: TC3 is a 16-bit counter

Bit<3>: TC3PTEN - TC3 prescaler enable bit

0: Disable TC3 prescaler

1: Enable TC3 prescaler

Bit<2:0>: TC3PSR<2:0> - TC3 prescaler selection control bits:

TC3PSR<2>	TC3PSR<1>	TC3PSR<0>	TC3 Prescaler Coefficient
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.56 R1C9/TC3CL (TC3 lower 8-bit count register)

0X1C9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC3CL	TC3C<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.57 R1CA/TC3CH (TC3 High 8-bit Count Register)

0X1CA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC3CH	TC3C<15:8>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.58 R1D6/INTE0 (Interrupt Enable Control Register 0)

0X1D6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE0	PWM2DTIE	ADIE	CMPIE	EX1IE	EX0IE	P7ICIE	P6ICIE	P5ICIE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM2DTIE - PWM2 duty cycle interrupt enable bit

0: Disabled

1: Enable (PWM2EN must also be enabled)

Bit<6>: ADIE - AD interrupt enable bit

0: Disabled

1: Enabled

Bit<5>: CMPIE - CMP interrupt enable bit

0: Disabled

1: Enabled

Bit<4>: EX1IE - EXINT1 interrupt enable bit

0: Disabled

1: Enabled

Bit<3>: EX0IE - EXINT0 interrupt enable bit

0: Disabled

1: Enabled

Bit<2>: P7ICIE - P7IC interrupt enable bit

0: Disabled

1: Enabled

Bit<1>: P6ICIE - P6IC Interrupt Enable Bit

0: Disabled

1: Enabled

Bit<0>: P5ICIE - P5IC Interrupt Enable Bit

0: Disabled

1: Enabled

3.1.59 R1D7/INTE1 (Interrupt Enable Control Register 1)

0X1D7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE1	-	RXIE	TXIE	CAPIE	TC3IE	TC2IE	TC1IE	TC0IE
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: Unused

Bit<6>: RXIE - UART Receive Interrupt Enable Bit

0: Disabled

1: Enabled

Bit<5>: TXIE - UART Transmit Interrupt Enable Bit

0: Disabled

1: Enabled

Bit<4>: CAPIE - Capture Complete Interrupt Enable Bit

0: Disabled

1: Enabled

Bit<3>: TC3IE - TC3 Interrupt Enable Bit

0: Disabled

1: Enabled

Bit<2>: TC2IE - TC2 Interrupt Enable Bit

0: Disabled

1: Enabled

Bit<1>: TC1IE - TC1 Interrupt Enable Bit

0: Disabled

1: Enabled

Bit<0>: TC0IE - TC0 Interrupt Enable Bit

0: Disabled

1: Enabled

3.1.60 R1DA/INTF0 (Interrupt Flag Register 0)

0X1DA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF0	PWM2DTIF	ADIF	CMPIF	EX1IF	EX0IF	P7ICIF	P6ICIF	P5ICIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM2DTIF - PWM2 duty cycle interrupt flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<6>: ADIF - AD Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<5>: CMPIF - CMP Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<4>: EX1IF - EXINT1 Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<3>: EX0IF - EXINT0 Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<2>: P7 ICIF - P7 IC Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<1>: P6 ICIF - P6 IC Interrupt Enable Bit

0: Interrupt not triggered

1: Interrupt Trigger

Bit<0>: P5 ICIF - P5 IC Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

3.1.61 R1DB/INTF1 (Interrupt Flag Register 1)

0X1DB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF1	-	RXIF	TXIF	CAPIF	TC3IF	TC2IF	TC1IF	TC0IF
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: Unused

Bit<6>: RXIF - UART Receive Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<5>: TXIF - UART Transmit Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<4>: CAPIF - Capture Complete Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<3>: TC3IF - TC3 Interrupt Flag

0: Interrupt not triggered

1: Interrupt Trigger

Bit<2>: TC2IF - TC2 Interrupt Flag Bit

0: Interrupt not triggered

1: Interrupt Trigger

Bit<1>: TC1IF - TC1 Interrupt Flag Bit

0: Interrupt not triggered

1: Interrupt Trigger

Bit<0>: TC0IF - TC0 Interrupt Flag Bit

0: Interrupt not triggered

1: Interrupt Trigger

3.1.62 R1E0/E2PCON (EEPROM Control Register)

0X1E0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2PCON	E2PLOCK<3:0>				-	E2PTIME	E2PRDEN	E2PWREN
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:4>: E2PLOCK<3:0> - EEPROM Function Unlock Bits

1001: Enter data 1001 Unlock EEPROM write operation

0110: Enter data 0110 Unlock ISP Function

Bit<3>: Not Used

Bit<2>: E2PTIME - EEPROM Write Time Selection Bit

0: EEPROM Write Time Fast Setting

1: EEPROM Write Time Slow Setting

Bit<1>: E2PRDEN - EEPROM Read Enable Bit

0: Disabled

1: Enabled

Bit<0>: E2PWREN - EEPROM Write Enable Bit

0: Disabled

1: Enabled

3.1.63 R1E1/E2PDATL (EEPROM Data Low 8-bit Register)

0X1E1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2PDATL	E2PDAT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.64 R1E2/E2PDATH (EEPROM Data High 8-bit Register)

0X1E2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2PDATH	E2PDAT<15:8>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.65 R1E3/SCON0 (UART Serial Port Control Register 0)

0X1E3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON0	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:6>: SM0:SM1 Mode Selection

SM0	SM1	Operating Mode	Transmit Baud Rate	Receive Baud Rate
0	1	8-bit UART	1/32 of Timer Overflow Frequency	Timer Overflow, RCLK Selection
1	0	9-bit UART	1/32 or 1/64 of the system clock Determined by SMOD	System clock or system clock divided by two Determined by SMOD
1	1	9-bit UART	1/32 of Timer Overflow Frequency	Timer Overflow, RCLK Selection

Bit<5>:SM2- Multi-processor communication control bit

0: When receiving, regardless of the 9th bit (RB8) being 0 or 1, data is sent to SBUF, and RI is set to 1 to generate an interrupt request

1: When receiving, if the 9th bit (RB8) is 1, data is sent to SBUF, and RI is set to 1 to generate an interrupt request

Bit<4>:REN- UART receive enable control

0: Reception disabled

1: Reception enabled

Bit<3>:TB8- The 9th bit of UART transmit data

Bit<2>: RB8 - The 9th bit of UART received data

Bit<1>: TI - Transmit Interrupt Flag

Transmit stop bit is set to 1 by hardware, cleared to 0 by software

Bit<0>: RI - Receive Interrupt Flag

Receive stop bit is set to 1 by hardware, cleared to 0 by software

3.1.66 R1E4/SBUF (UART Transmit and Receive Data Register)

0X1E4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF	SBUF<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

During serial transmission, MCU writes data to SBUF

During serial reception, MCU reads data from SBUF

3.1.67 R1E5/SCON1 (UART Serial Port Control Register 1)

0X1E5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON1	-	-	UARTS	TXDS	RXDS	SMOD	TCLK	RCLK
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:6>: Unused bits

Bit<5>: UARTS - UART port selection

0: Select UART0 group ports, corresponding to TX0, RX0

1: Select the UART1 group ports, corresponding to TX1 and RX1

Bit<4>:TXDS- UART Transmit Port Control

0: Disable UART transmit port

1: Enable UART transmit port (UARTS = 0 selects P53, UARTS = 1 selects P67)

Bit<3>:RXDS- UART Receive Port Control

0: Disable UART receive port

1: Enable UART receive port (UARTS = 0 selects P54, UARTS = 1 selects P66)

Bit<2>:SMOD- UART Baud Rate Control Bit (only effective for mode 2)

0: UART baud rate uses 1/64 of the system clock

1: UART baud rate uses 1/32 of the system clock

Bit<1>:TCLK- UART Transmit Baud Rate Control Bit (only effective for modes 1 and 3)

0: UART transmission baud rate uses TC0 overflow frequency

1: UART transmission baud rate uses TC3 overflow frequency

Bit<0>: RCLK - UART reception baud rate control bit (effective only for modes 1 and 3)

0: UART reception baud rate uses TC0 overflow frequency

1: UART reception baud rate uses TC3 overflow frequency

3.1.68 R1E6/LCDCON (LCD Control Register)

0X1E6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON	LCDEN	LCDMD	DS<1:0>		TYPE	LCDCKS	LCDPSR<1:0>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: LCDEN - LCD Enable Bit

0: Disabled

1: Enabled

Bit<6>: LCDMD - LCD Mode Select Bit

0: LED Mode

1: LCD Mode

Bit<5:4>: DS<1:0> - LCD Duty Cycle Select Bits

DS<1>	DS<0>	LCD Duty Cycle
0	0	1/2
0	1	1/3
1	X	1/4

Bit<3>: TYPE - LCD Type SelectionBit

0: LCD-A Type / LED Common Cathode Mode

1: LCD-B Type / LED Common Anode Mode

Bit<2>: LCDCKS - LCD Clock Source SelectionBit

0: System Clock

1: Low-Speed Clock

Bit<1:0>: LCDPSR<1:0> - LCDClock Division SelectionBits

LCDPSR<1>	LCDPSR<0>	Clock division
0	0	Divide by 16
0	1	Divide by 32
1	0	Divide by 64
1	1	Divide by 128

3.1.69 R1E7/SEGCON0 (SEG Control Register 0)

0X1E7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEGCON0	SEGEN<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0> : SEGEN<7:0> - SEG enable bits

0: Disabled

1: Enabled

3.1.70 R1E8/SEGCON1 (SEG Control Register 1)

0X1E8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEGCON1	SEGEN<15:8>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0> : SEGEN<15:8> - SEG Enable Bits

0: Disabled

1: Enabled

3.1.71 R1E9/LCDDB (LCD Data Register)

0X1E9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDDB	LCDDB<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0> : LCDDB<7:0> - LCD RAM Data Read/Write Bits

3.1.72 R1EA/CMPCON0 (CMP Control Register 0)

0X1EA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON0	CMPEN	CMPOUT	CMPRS<5:0>					
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPEN - CMP enable control bit

0: Disabled

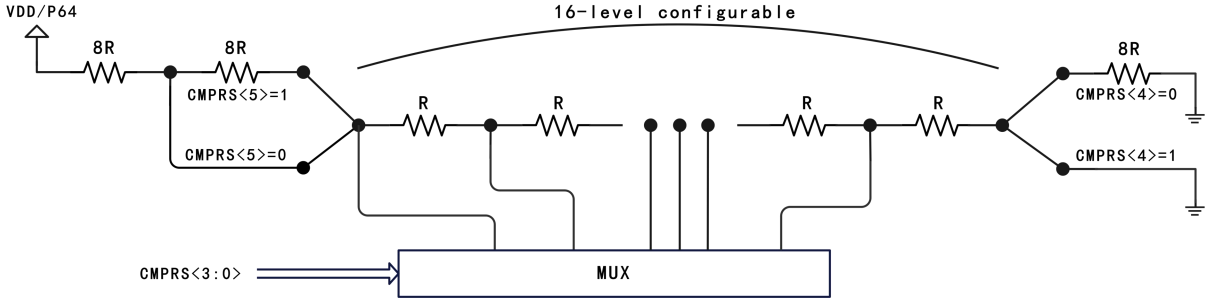
1: Enabled

Bit<6>: CMPOUT - CMP result output bit

0: Comparator positive input voltage is less than negative input voltage

1: Comparator positive input voltage is greater than negative input voltage

Bit<5:0>: CMPRS<5:0> - Comparator trim bits



When the CMPCON1 register = 0x07, the ADCON1 register VREF<2:0> selects VDD, the comparator positive input selects resistor voltage division, the comparator negative input selects VBG, and different resistor voltage division levels CMPRS<5:0> correspond to different detection voltages, as shown in the following table (detection voltages in the gray area are prohibited for use):

CMPRS	Detection Voltage	CMPRS	Detection Voltage	CMPRS	Detection Voltage	CMPRS	Detection Voltage
00H	4.44V	10H	30.00V	20H	5.56V	30H	40.00V
01H	4.00V	11H	15.00V	21H	5.00V	31H	20.00V
02H	3.64V	12H	10.00V	22H	4.55V	32H	13.33V
03H	3.33V	13H	7.50V	23H	4.17V	33H	10.00V
04H	3.08V	14H	6.00V	24H	3.85V	34H	8.00V
05H	2.86V	15H	5.00V	25H	3.57V	35H	6.66V
06H	2.67V	16H	4.29V	26H	3.33V	36H	5.71V
07H	2.50V	17H	3.75V	27H	3.13V	37H	5.00V
08H	2.35V	18H	3.33V	28H	2.94V	38H	4.44V
09H	2.22V	19H	3.00V	29H	2.78V	39H	4.00V
0AH	2.10V	1AH	2.73V	2AH	2.63V	3AH	3.64V
0BH	2.00V	1BH	2.50V	2BH	2.50V	3BH	3.33V
0CH	1.90V	1CH	2.31V	2CH	2.38V	3CH	3.08V
0DH	1.82V	1DH	2.14V	2DH	2.27V	3DH	2.86V
0EH	1.74V	1EH	2.00V	2EH	2.17V	3EH	2.67V
0FH	1.67V	1FH	1.88V	2FH	2.08V	3FH	2.50V

3.1.73 R1EB/CMPCON1 (CMP Control Register 1)

0X1EB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON1	CMPOE	CMPINV	CMPIS<5:0>					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPOE - Comparator result output enable

0: P61 as GPIO

1: Comparator result output from P61

Bit<6>: CMPINV - CMPOUT output result inversion

0: No inversion

1: Inversion

Bit<5>: CMPIS<5> - Voltage input of voltage divider resistor

0: ADC reference voltage, requires setting ADCON1 register VREF<2:0> bits

1: P64 input

Bit<4:3>: CMPIS<4:3> - Comparator positive input source selection

CMPIS<4>	CMPIS<3>	Positive input source
0	0	Resistive voltage division
0	1	CIN0+/P51
1	0	CIN1+/P63
1	1	VBG (Bandgap voltage 1.29V)

Bit<2:0>: CMPIS<2:0> - Comparator negative input source selection

CMPIS<2>	CMPIS<1>	CMPIS<0>	Negative Input Source
0	0	0	CIN0-/P52
0	0	1	CIN1-/P65
0	1	0	CIN2-/P55
0	1	1	CIN3-/P56
1	0	0	CIN4-/P66
1	0	1	CIN5-/P67
1	1	0	Resistive voltage division
1	1	1	VBG (Bandgap voltage 1.29V)

3.1.74 R1FF/IAR (Indirect Address Register)

0X1FF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAR	IAR<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

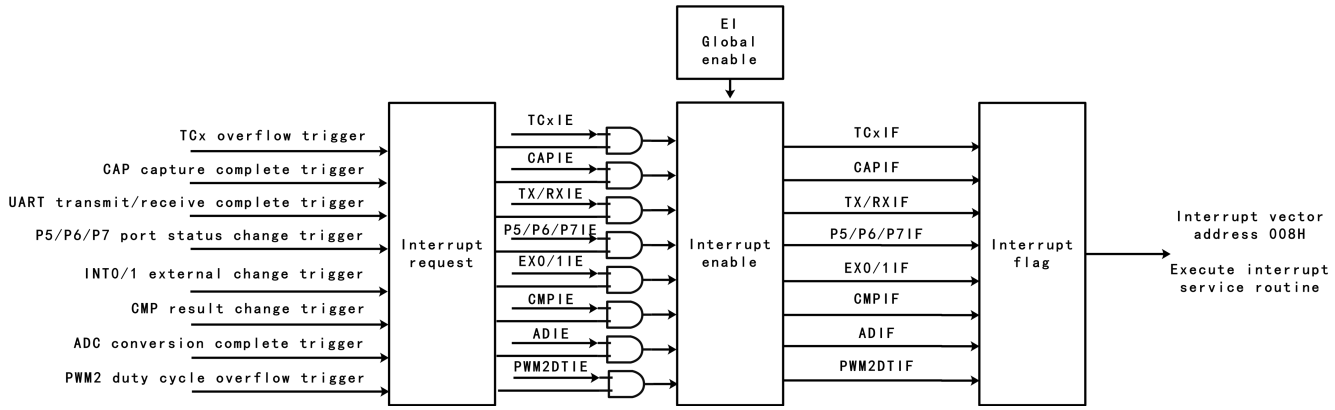
The indirect addressing register is not an actual physical register; its main function is to serve as a pointer for indirect addressing. Any instruction using R1FF as a pointer actually corresponds to the address R180 (RAM selection register) RSR<7:0> pointing to data in the SRAM.

3.2 Interrupts

The JZ8M4601 has 15 interrupt sources. Regardless of which interrupt is used, the global interrupt must be enabled by the "EI" instruction. The interrupt vector address is fixed at 008H. The characteristics of each interrupt are as follows:

Interrupt sources	Enable condition	Interrupt flag
TC0 overflow interrupt	EI + TC0IE=1	TC0IF
TC1 overflow interrupt	EI + TC1IE=1	TC1IF
TC2 overflow interrupt	EI + TC2IE=1	TC2IF
TC3 Overflow Interrupt	EI + TC3IE=1	TC3IF
CAP Capture Complete Interrupt	EI + CAPIE=1	CAPIF
UART Transmission Complete Interrupt	EI + TXIE=1	TXIF
UART Reception Complete Interrupt	EI + RXIE=1	RXIF
P5 Port Input Change Interrupt	EI + P5ICIE=1	P5ICIF
P6 Port Input Change Interrupt	EI + P6ICIE=1	P6ICIF
P7 Port Input Change Interrupt	EI + P7ICIE=1	P7ICIF
INT0 External Interrupt	EI + EX0IE=1	EX0IF
INT1 External Interrupt	EI + EX1IE=1	EX1IF
CMP Comparison Complete Interrupt	EI + CMPIE=1	CMPIF
ADC Conversion Complete Interrupt	EI + ADIE=1	ADIF
PWM2 Duty Cycle Overflow Interrupt	EI + PWM2DTIE=1	PWM2DTIF

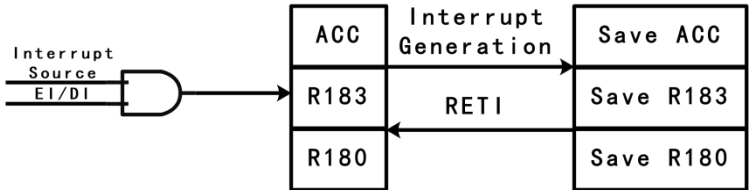
R1DA/R1DB are interrupt flag registers that record the interrupt flag bits after an interrupt request is generated. R1D6/R1D7 are interrupt enable control registers where the enabling and disabling of interrupts are set. The overall interrupt enable is controlled by the "EI" instruction, while the overall interrupt disable is controlled by the "DI" instruction. When an interrupt occurs, the execution of the next instruction will jump to the interrupt vector address 008H. Before exiting the interrupt service routine, the corresponding interrupt flag bit must be cleared to avoid false triggering of the interrupt.



Interrupt Principle Diagram

3.2.1 Interrupt Context Protection

During the interrupt response process, the hardware has a built-in interrupt protection function that saves the contents of ACC, R183, and R180. When leaving the interrupt service routine, the saved values are reloaded into ACC, R183, and R180. This is to prevent instructions in the interrupt subroutine from changing the values of ACC, R183, and R180, which could cause errors when returning to the main program. As shown in the figure below:



Interrupt Context Protection Diagram

3.3 Reset

3.3.1 Overview of Reset Function

The JZ8M4601 system provides four reset methods:

- Power-On Reset (POR)
- RESET pin input low-level reset
- WDT watchdog overflow reset
- LVR low voltage reset

When any of the above resets occur, all system registers are initialized to their reset values, the program stops running, and the program counter (PC) is cleared. After the reset ends, the system restarts running from vector address 0000H.

Each type of reset requires a certain response time. The system reset mechanism ensures reliable MCU reset. Different types of oscillators require different times to complete the reset. Therefore, the rise speed of VDD and the startup time of different oscillators are not fixed. The RC oscillator has the shortest startup time, while the crystal oscillator has a longer startup time. During user terminal operation, attention should be paid to the application scenario’s requirements for power-on reset time.

3.3.2 Power-On Reset (POR)

Power-on reset is closely related to LVR operation. The system power-up process follows a gradually rising curve and requires some time to reach the normal voltage level.

- Power-on: The system detects the rising power supply voltage and waits for it to stabilize;
- System initialization: All system registers are set to their initial values;
- The oscillator starts working: the oscillator begins to provide the system clock;
- Program execution: power-on is complete, and the program starts running;

The power-on reset time is determined by the [Reset Time] selection in OPTION, as shown in the table below:

PWRT and WDT	Reset establishment time
PWRT = WDT	4.5ms (follows watchdog reset time)
PWRT = WDT	16ms (follows watchdog reset time)
PWRT = WDT	64ms (follows watchdog reset time)
PWRT = WDT	256ms (follows watchdog reset time)
PWRT≠WDT	350us (Independent fixed reset time)

3.3.3 WDT Watchdog Reset

The watchdog reset is a type of system protection setting. Under normal conditions, the program clears the watchdog timer. If an error occurs and the system is in an unknown state, the watchdog timer overflows, causing the system to reset. After the watchdog reset, the system restarts and enters a normal state.

- Watchdog timer status: The system checks whether the watchdog timer has overflowed; if it has, the system resets;
- System initialization: All system registers are set to their default initialization values;
- The oscillator starts working: the oscillator begins to provide the system clock;
- Program execution: power-on is complete, and the program starts running;

Explanation of watchdog wake-up:

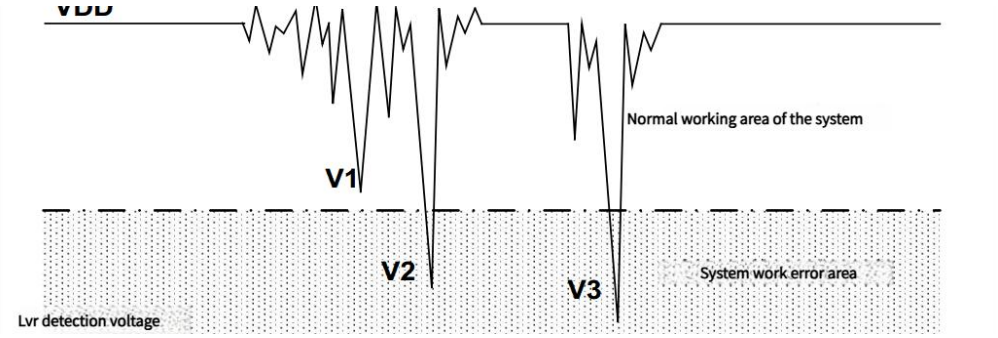
The watchdog reset can reset the system in both idle and sleep modes. After the system resets, the program executes from address 0X00. The user can check bit 4 (time overflow bit) of the R183 (STATUS) register. If it indicates a WDT overflow, it can be determined as a watchdog reset, and the corresponding wake-up subroutine can be executed. Note that the watchdog wake-up is essentially a special application of the watchdog reset.

Watchdog timer application precautions:

- Before clearing the watchdog, checking the status of I/O ports and RAM can enhance program reliability;
- Do not clear the watchdog in the interrupt; otherwise, it will be unable to detect the main program runaway condition.
- There should be only one watchdog clear action in the main program. This architecture can maximize the protective function of the watchdog.

3.3.4 LVR Low Voltage Reset

Power-down reset addresses situations where the system voltage drops due to external factors (such as interference or changes in external loads). Power-down may cause abnormal system operation or program execution errors.



A voltage drop may cause the system to enter a dead zone. The dead zone means the power supply cannot meet the system's minimum operating voltage requirement. The above figure is a typical power-down reset diagram. In the figure, VDD is severely disturbed, and the voltage drops very low. The area above the dashed line is where the system operates normally; below the dashed line, the system enters an unknown operating state called the dead zone. When VDD drops to V1, the system is still in a normal state; when VDD drops to V2 and V3, the system enters the dead zone, which easily leads to errors. The system may enter the dead zone under the following conditions:

In DC applications:

DC applications generally use battery power. When the battery voltage is too low or the microcontroller drives a load, the system voltage may drop and enter the dead

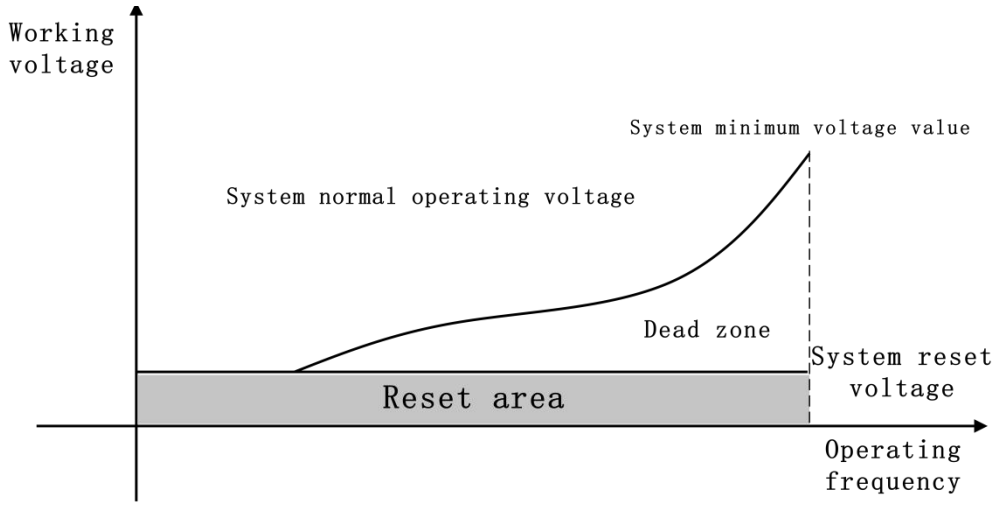
zone. At this time, the power supply will not further drop to the LVR detection voltage, so the system remains in the dead zone.

In AC applications:

When the system uses AC power, the DC voltage value is affected by noise in the AC power supply. When the external load is too high, such as driving a motor, the interference generated by the load operation also affects the DC power supply. If VDD drops below the minimum operating voltage due to interference, the system may enter an unstable operating state. In AC applications, the system's power-on and power-off times are relatively long. Among them, the power-on sequence protection allows the system to power on normally, but the power-off process is similar to the DC application scenario. After the AC power is turned off, the VDD voltage slowly drops and easily enters the dead zone.

3.3.5 Relationship Between Operating Frequency and LVR Low Voltage Detection

To improve the performance of the system power-down reset, it is first necessary to clarify the system's minimum operating voltage. The system's minimum operating voltage is related to the system execution speed, and the minimum operating voltage value varies at different execution speeds.



As shown in the above figure, the system's normal operating voltage range is generally higher than the system reset voltage, and the reset voltage is determined

by the Low Voltage Reset (LVR) level. When the system execution speed increases, the system's minimum operating voltage also rises accordingly. However, since the system reset voltage is fixed, a voltage region appears between the system's minimum operating voltage and the system reset voltage where the system cannot operate normally and will not reset. This region is called the dead zone.

To avoid the occurrence of dead zone voltage, when selecting the operating frequency, the corresponding LVR reset voltage point should be chosen. The table is as follows:

IRC Frequency	Clocks Division	LVR Reset Voltage Point
IRC-16MHz	2 Clocks	LVR=2.2V
IRC-6MHz	2 Clocks	LVR=1.8V
IRC-1MHz	2 Clocks	LVR=1.8V

Note: 1. Operating frequency = instruction cycle frequency = IRC frequency + Clocks division;

2. The correspondence between this operating frequency and the LVR reset voltage point is only a recommended value. Users can appropriately adjust the reset voltage point according to the specific application scenario during use.

3.4 Operating Modes

The JZ8M4601 can operate at different clock frequencies in four operating modes. These modes control the operation of the oscillator, program execution, and the power consumption of analog circuits.

- High-Speed Mode: The system clock selects the internal high-speed clock, and the low-speed clock operates normally;
- Low-Speed Mode: The system clock selects the internal low-speed clock, and the high-speed clock is suspended;
- Idle Mode: The system clock operates normally, while other parts of the system enter sleep (TC0, TC1, TC2, TC3 selecting the system clock can continue to work and wake the system, RTC mode can also wake it); waking can also be triggered via P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, ADCWE, CMPWE, UARTWE;
- Sleep Mode: All functions are suspended, and the system enters sleep. It can be woken up by TC0 (P62 external input or RTC mode), P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, CMPWE;

Functional Modules	High-Speed Mode	Low-Speed Mode	Idle Mode	Sleep Mode
IHRC	Run	Stop	Run	Stop
ILRC	Run	Run	Run	Stop
CPU	Execute	Execute	Stop	Stop
TC0	Operable	Operable	Operable	Operable (P62 Input Clock, RTC Mode)
TC1	Operable	Operable	Operable	Stop
TC2	Operable	Operable	Operable	Stop
TC3	Operable	Operable	Operable	Stop
Interrupt	All Valid	All Valid	All Valid (TC0, TC1, TC2, TC3 select system clock)	TC0IE, P5ICIE, P6ICIE, P7ICIE, INT0IE, INT1IE, CMPIE
Wake-up Function	-	-	(TC0, TC1, TC2, TC3 select system clock can wake up) P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, ADCWE, CMPWE, UARTWE	TC0WE, P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, CMPWE
Watchdog	WDT Option Control	WDT Option Control	WDT Option Control	WDT Option Control

3.4.1 High-Speed Mode

High-speed mode is the system high-speed clock operating mode, with the system clock source provided by the high-speed RC oscillator. The program is executed. After power-on reset or any reset trigger, the system enters high-speed mode to execute the program. In high-speed mode, the high-speed oscillator operates normally, and power consumption is at its maximum.

- The program is executed, and all functions are controllable;
- The system rate is high-speed;
- Both the high-speed oscillator and the internal low-speed oscillator operate normally;
- High-speed mode can switch to low-speed mode;
- Entering sleep mode from high-speed mode, and returning to high-speed mode after wake-up;
- Entering idle mode from high-speed mode, and returning to high-speed mode after wake-up;

3.4.2 Low-Speed Mode

Low-speed mode is the system low-speed clock operating mode. The system clock source is provided by the low-speed RC oscillator. Low-speed mode is controlled by the CLKMD bit in the CPU mode control register. When CLKMD=0, the system is in high-speed mode; when CLKMD=1, the system enters low-speed mode. After entering low-speed mode, the system cannot automatically disable the high-speed RC oscillator; it must be disabled by setting SPTHX=1 to reduce power consumption.

- The program is executed, and all functions are controllable;
- The system rate is low speed;
- The internal low-speed oscillator operates normally, and the high-speed oscillator stops working.
- Low-speed mode can switch to high-speed mode;
- Entering sleep mode from low-speed mode, returning to low-speed mode after wake-up;

- Entering idle mode from low-speed mode, returning to low-speed mode after wake-up;

3.4.3 Idle Mode

Idle mode is another ideal state. In sleep mode, all functions and hardware devices are disabled, but in idle mode, the system clock remains running. Power consumption in idle mode is higher than in sleep mode. In idle mode, the program does not execute, but modules with wake-up functions such as TC0, TC1, TC2, TC3, P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, ADCWE, CMPWE, and UARTWE continue to operate normally. The clock sources for timers TC0, TC1, TC2, and TC3 are the system clock, which remains active. Whether to enter idle mode is determined by the system clock and the IDLE bit in the status control register. When IDLE=1, executing SLEEP enters idle mode.

- Program execution stops, and all functions are disabled;
- Modules with wake-up functions operate normally;
- The system clock operates normally;
- Entering idle mode from high-speed mode, returning to high-speed mode after being awakened;
- Entering idle mode from low-speed mode, returning to low-speed mode after being awakened;
- Wake-up methods in idle mode are P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, ADCWE, CMPWE, UARTWE;
- TC0, TC1, TC2, and TC3 functions remain effective in idle mode;

3.4.4 Sleep Mode

Sleep mode is the ideal state of the system, where no program is executed and the oscillator stops working. The entire chip’s power consumption is below 1uA. Sleep mode can be awakened by TC0 (P62 input clock), P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, CMPWE. Entering sleep mode from high-speed or low-speed mode will return to the corresponding mode after being awakened. Whether to enter sleep mode is controlled by the system clock and the IDLE bit of the status control register. When IDLE=0, executing SLEEP enters sleep mode.

- Program execution stops, and all functions are disabled;
- All oscillators, including the external high-speed oscillator, internal high-speed oscillator, and internal low-speed oscillator, stop working;
- Power consumption is below 1uA;

- Entering sleep mode from high-speed mode, returning to high-speed mode after being awakened;
- Transition from low-speed mode to sleep mode, and return to low-speed mode after being awakened;
- The wake-up methods in sleep mode are TC0 (P62 input clock), P5IWE, P6IWE, P7IWE, INT0WE, INT1WE, CMPWE;

3.5 System Clock

The JZ8M4601 integrates three oscillators internally: a high-speed RC oscillator IHRC, a low-speed RC oscillator ILRC, and an external crystal oscillator. The system clock can switch between high and low-speed oscillators via the R188/CPUCON registers.

3.5.1 Internal IHRC Oscillator

The JZ8M4601 has a built-in IHRC high-speed oscillator that provides configurable IHRC frequency functionality. The default frequency is 6 MHz, and the IHRC frequency can be fine-tuned via the IHRCCAL register.

The IHRC oscillator includes four frequency options: 1M/6M/16M/32M Hz. By setting the OPTION configuration bits, the IHRC operating frequency can be selected. The following are their corresponding relationships:

RCM	IRC Frequency
1M	IHRC frequency selected as 1MHz
6M	IHRC frequency selected as 6MHz
16M	IHRC frequency selected as 16MHz
32M	IHRC frequency selected as 32MHz

The JZ8M4601 provides multiple instruction clock division options, which can be selected in OPTION, suitable for more scenarios. As shown in the table below:

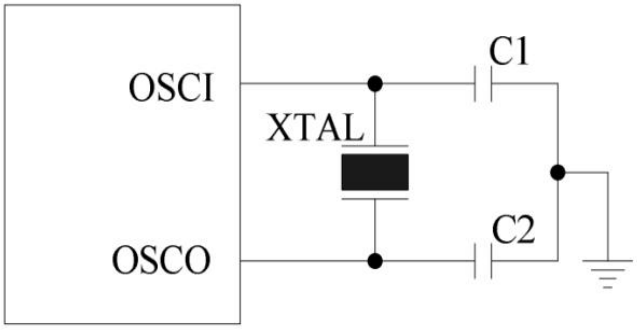
Clocks	Clocks Division
2clock	Frequency division is 2clock
4clock	Frequency division is 4clock
8clock	Frequency division is 8clock
16clock	Frequency division is 16clock
32clock	Frequency division is 32clock

3.5.2 Internal ILRC Oscillator

The JZ8M4601 has a built-in ILRC low-speed oscillator that provides a stable 40KHz low-speed clock.

3.5.3 External Crystal/Ceramic Oscillator

The JZ8M4601 features built-in HXT/LXT crystal oscillator start-up circuits and three selectable internal capacitors (14pF, 18pF, 25pF). In most applications, a crystal or ceramic resonator can be connected to the OSCO and OSCI pins to generate oscillation. The circuit diagram is shown below, and the table lists the recommended values for C1 and C2. Since the characteristics of each resonator vary, users should refer to their specifications to select appropriate values for C1 and C2.



Crystal Oscillator Application Circuit

Reference for Capacitor Selection of Crystal Oscillator or Ceramic Oscillator:

Oscillator Mode	Frequency Mode	Frequency	C1(pF)	C2(pF)	Recommended Built-in Capacitor Value
High-Speed Crystal Oscillator	HXT	400K~16MHz	5-30	5-30	14pf
Low-speed crystal oscillator	LXT	32.768KHz	5-30	5-30	25pf

Note: The above data is for reference only; all are subject to actual product testing.

3.5.4 Clock Module Application Instructions

- The internal oscillator is the most commonly used oscillation mode, which can eliminate the need for external circuits;
- When using an external clock input, the clock signal should be input from OSCI, and OSCO can be left floating;
- Due to different external conditions, the clock frequencies of various oscillation modes may have slight differences; reasonable selection should be made according to actual needs during use;

3.6 I/O Ports

The JZ8M4601 has 3 sets of bidirectional I/O ports, with a total of 22 inputs and 22 outputs. Most I/Os can be multiplexed for other functions.

22 programmable pull-up I/O pins: P50 - P57, P60 - P67, P70 - P75;

22 programmable pull-down I/O pins: P50 - P57, P60 - P67, P70 - P75;

22 optionally selectable drive-enhanced I/O pins: P50 - P57, P60 - P67, P70 - P75;

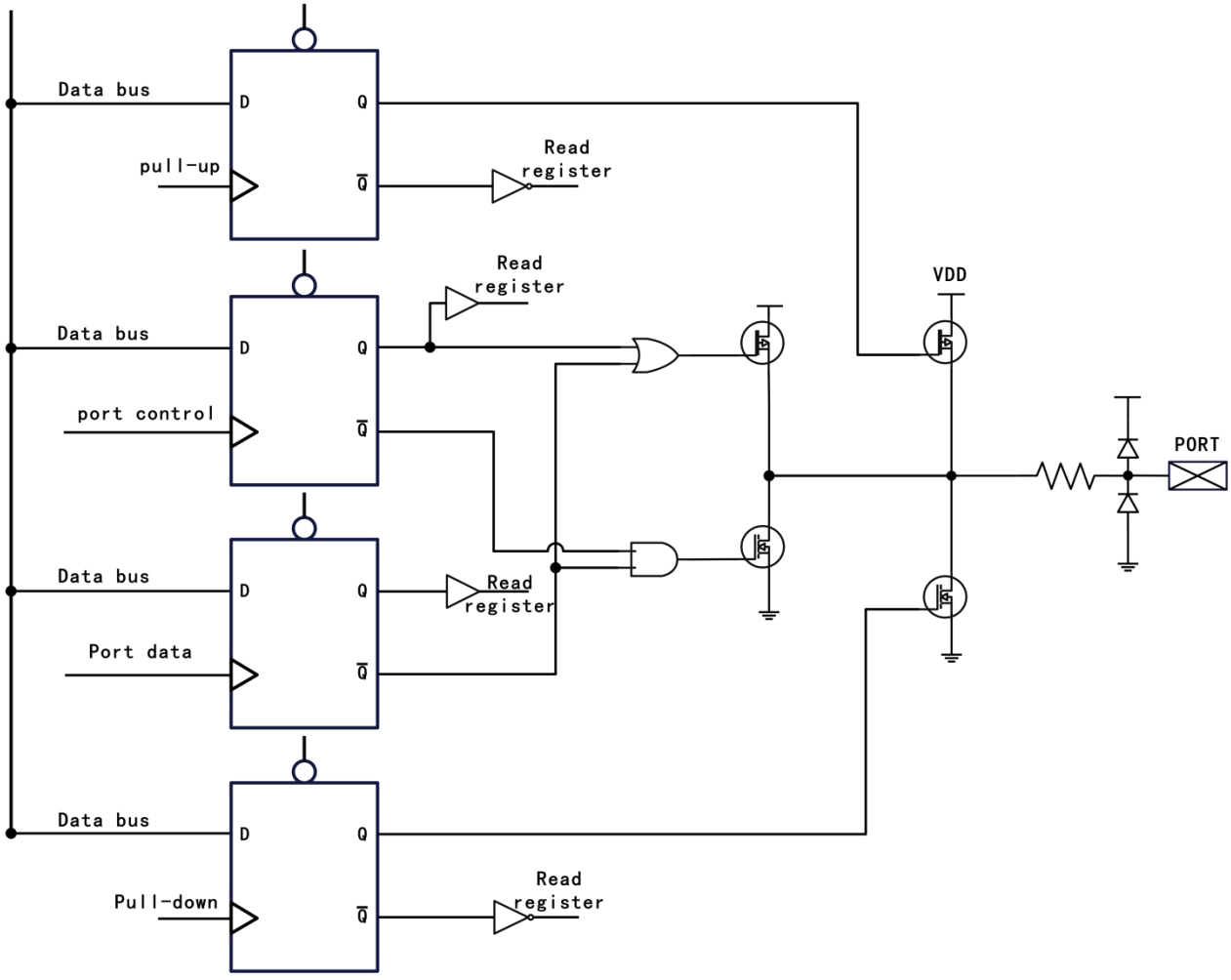
4 optionally selectable drive-level 2 enhanced I/O pins: P60 - P63;

22 programmable wake-up I/O pins: P50 - P57, P60 - P67, P70 - P75;

16 programmable analog ports: P50 - P52, P55 - P57, P60 - P67, P70 - P71;

3.6.1 GPIO Internal Block Diagram

The following internal block diagram is for reference and understanding only and does not represent the actual circuit.



IO Control Register/Data Register/Pull-up/Pull-down Structure Circuit

3.6.2 Port Input Change Wake-up

The JZ8M4601 includes 22 programmable port input change wake-up I/Os: P50 - P57, P60 - P67, P70 - P75. The chip can enter sleep mode or idle mode by executing the "SLEEP" instruction. At this time, the CPU does not execute instructions. The port input change wake-up can be programmed to either continue the original process (if DI is executed before SLEEP) or perform the corresponding jump (if EI is executed before SLEEP). The corresponding interrupt enable control must be turned on, and after the port input change wake-up, the program jumps to the interrupt service routine.

Port status change polling wake-up settings:

1. Set the port input change wake-up pin as input;
2. Select internal pull-up or pull-down for the wake-up pin as needed;
3. Enable port input change wake-up control P5IWE/P6IWE/P7IWE;
4. Execute the DI instruction to avoid entering the interrupt address;
5. Execute the "SLEEP" instruction, with IDLE=0 entering sleep mode or IDLE=1 entering idle mode;
6. After wake-up, execute the instruction following SLEEP;

Port status change interrupt wake-up settings:

1. Set the port input change wake-up pin as input;
2. Select internal pull-up or pull-down for the wake-up pin as needed;
3. Enable port input change wake-up control P5IWE/P6IWE/P7IWE;
4. Enable port input change interrupt P5ICIE/P6ICIE/P7ICIE;
5. Execute the "EI" instruction and wait to enter the interrupt address;
6. Execute the "SLEEP" instruction, IDLE=0 to enter sleep mode or IDLE=1 to enter idle mode;
7. After wake-up, it will enter the interrupt address, and after exiting the interrupt, execute the next instruction after SLEEP;

3.6.3 Port Schmitt parameters

Schmitt characteristics of JZ8M4601 ports are shown in the table below (for reference only):

Port	SMT	
P50～P57	0.25*VDD	0.54*VDD
P60～P67	0.25*VDD	0.54*VDD
P70～P75	0.25*VDD	0.54*VDD

The above parameters are for reference only. Please refer to the actual measured data of the target prototype.

3.7 Timer Counter

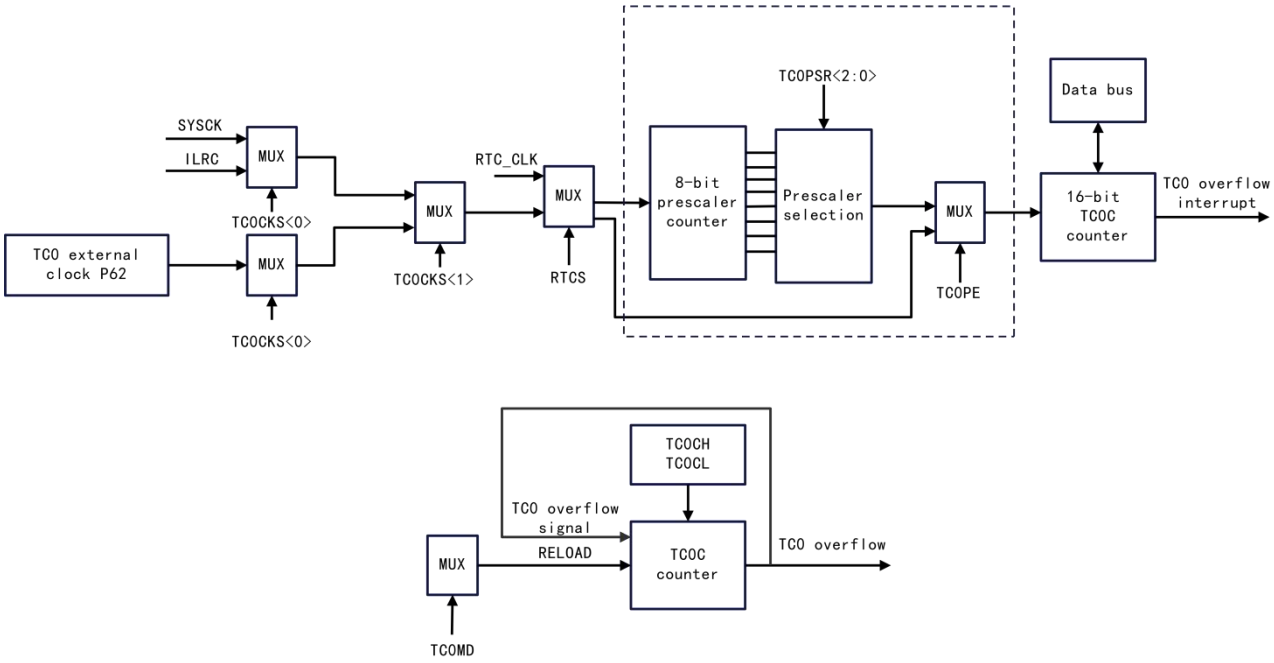
3.7.1 TC0 Timer Counter

The JZ8M4601 provides an 8-bit timer counter as the TC0 prescaler. The TC0PTEN bit in the TC0CON register determines the enablement of the prescaler, and the three bits TC0PSR<2:0> determine the prescale ratio.

TC0 is a 16-bit reloadable up-counter. When writing to the reload register, the same value is written to the TC0 count register by default. After enabling TC0EN, the clock source can be the internal low-speed clock, system clock, or an external clock (input via pin P62, with selectable trigger edge), or the external crystal oscillator clock in RTC mode. The counter increments by 1 on each clock arrival.

TC0 count overflow can generate an interrupt signal.

In IDLE mode, the TC0 interrupt can wake up the circuit. After waking up, it can either enter the interrupt or continue executing the original program; the method refers to wake-up by port input change. In sleep mode, when TC0 is set to the P62 external input clock or the RTC external crystal oscillator clock, it can interrupt on overflow and wake up the circuit.



Block Diagram of TC0

3.7.1.1 Description of TC0 Timing Settings

1. Assign initial values to TC0CL and TC0CH registers of TC0C;
2. Set the value of the TC0CON register (select clock source and prescaler);

3. When used as a counter, select the TC0 signal source as an external input signal in the TC0CON register; when selecting the RTC crystal oscillator as the signal source, select RTC mode in the TC0CON register and enable RTC_EN in OPTION;
4. If using the reload function, set TC0MOD in the CAPCON register to 0 for automatic reload mode, and set the reload values in TC0RL and TC0RH;
5. After all configurations are set, finally enable the timing counter by setting TC0EN in the TC0CON register;
6. If interrupt function is required, set TC0IE (Bit0) in the INTE1 register to 1 and execute the EI instruction;
7. When the system executes the interrupt service routine, ACC, STATUS, and RSR data are automatically saved; after executing the RETI instruction, the data is automatically restored. Before exiting the interrupt, the TC0 interrupt flag must be cleared;

3.7.1.2 Description of TC0 Timing Calculation

The TC0 timing function sets the initial value of the timer by writing values to the TC0RL, TC0RH, or TC0CL, TC0CH registers. The timer starts accumulating from the initial value until it overflows and generates an interrupt.

TC0 timing calculation formula (when selecting internal system clock):

$$\text{TC0 Timing duration} = (1/\text{Fosc}) \times (\text{TC0 prescaler}) \times (65536 - \text{TC0 } \textit{initial value})$$

Example:

Fosc = 6 MHz, TC0 prescaler selection = 8 prescaler, TC0 initial value = 64936;

$$\text{TC0 Timing duration} = (1/6) \times (8) \times (65536 - 64936) = 800\ \text{us}$$

TC0 timing calculation formula (when selecting external input clock):

$$TC0\ \text{Timingduration} =$$

$$(1/\text{External input clock}) \times (\text{TC0 prescaler}) \times (65536 - \text{TC0 } \textit{initial value})$$

Example:

External input clock = 1 MHz, TC0 prescaler selection = 4 prescaler, TC0 initial value = 65286;

$$\text{TC0 Timing duration} = (1/1) \times (4) \times (65536 - 65286) = 1000\ \text{us}$$

3.7.1.3 TC0 Idle Mode Wake-up Description

In idle mode, system instructions stop executing, modules with wake-up functions and the system clock operate normally, while other functions are disabled.

TC0 can wake up from idle mode by setting bit 3 (TC0WE) of the R188/CPUCON register to 1. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC0 timer operates normally (using the system clock). When the TC0 timer

overflows, the system is awakened. If TC0IE and EI are enabled, the system enters an interrupt after waking up; if DI is executed, the system executes the next instruction after waking up.

Wake-up and interrupt in reload mode are consistent with the TC0 timing counter.

When the clock source selects the P62 external clock or RTC crystal oscillator clock, enabling TC0WE = 1 and directly executing the SLEEP instruction can also wake up the system.

3.7.1.4 RTC Mode Description

Set bit 6 RTCS=1 of the R1C0/TC0CON register and enable the [RTC] option to activate RTC mode. In this mode, the TC0 interrupt clock source is an external 32.768KHz low-speed crystal oscillator (default 4 division), and the main clock is the selected IHRC clock. After enabling RTC, internal crystal oscillator capacitors of 14pF, 18pF, or 25pF can be selected, or the internal capacitors can be turned off and an external crystal capacitor in the range of 5~30pF can be added, setting the appropriate capacitance according to requirements.

Software enable: setting bit 0 LXT_STEN=1 in the R1AE/EXINTCON register can enhance the startup of the low-speed crystal oscillator. After the crystal starts oscillating, disable this enable to avoid increased power consumption. At the same time, the read-only flag bit LXT_ERR at bit 5 of the R183/STATUS register can be monitored; when LXT_ERR=1, the crystal oscillator is operating normally, and when LXT_ERR=0, the crystal oscillator is abnormal.

RTC timing accuracy is directly related to the external crystal oscillator and capacitors. It is recommended to use high-precision components. Power supply fluctuations also affect timing, so adding capacitor filtering and optimization at the power ground is necessary.

RTC timing calculation formula:

$$\text{RTC Timing duration} = (4/32768) \times (\text{TC0 prescaler}) \times (65536 - \text{TC0 } \textit{initial value})$$

Example:

TC0 division selection = 1 division, TC0 initial value = 57344;

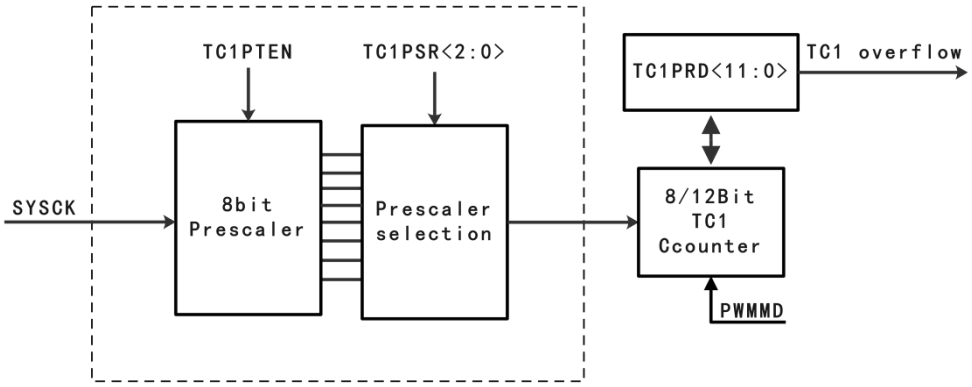
RTC timing = 4/32768 * 1 * (65536 - 57344) = 1s

3.7.2 TC1 Timer Counter

TC1 timer counter provides an 8-bit prescaler. The three bits TC1PSR<2:0> of the TC1CON register determine the prescaler ratio. In TC1 mode, each time TC1EN is enabled, the prescaler register is cleared.

TC1 is a 12-bit up-counter. The TC1 timer requires TC1EN to be enabled to operate. The clock source is the internal system clock, and the counter increments by 1 on each clock cycle. When the TC1 count value matches the TC1PRD set value, an overflow occurs. If TC1IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service routine.

In IDLE mode, the TC1 interrupt can wake up the circuit (the clock is the system clock). After waking up, it can either enter the interrupt or continue executing the original program. The method refers to wake-up by port input change.



TC1 block diagram

3.7.2.1 TC1 Timing Setup Description

1. Assign initial values to the TC1PRD<11:0> register;
2. Set the TC1CON register and configure the prescaler ratio as needed;
3. Enable the TC1IE interrupt enable in the R1D7/INTE1 register, and execute the EI instruction;
4. Enable TC1EN to start the TC1 timer counting;
5. The system will automatically save ACC, STATUS, and RSR data when executing the interrupt service routine. After executing the RETI instruction, the data will be automatically restored. Before exiting the interrupt, the TC1 interrupt flag must be cleared;

3.7.2.2 TC1 Timing Calculation Description

The TC1 timing function works by writing a value to TC1PRD<11:0>. The timer starts counting from the initial value 0x01 and increments until the timer count matches the TC1PRD<11:0> value, then overflows and executes the interrupt service routine.

TC1 timing calculation formula:

$$\text{TC1 Timing duration} = (1/\text{Fosc}) \times (\text{TC1 Prescaler}) \times (\text{TC1PRD} - 1)$$

Example:

Fosc = 16 MHz, TC1 prescaler selection = 16 prescaler, TC1PRD value = 512;

$$\text{TC1 Timing duration} = (1/16) \times (16) \times (512 - 1) = 511\text{us}$$

3.7.2.3 TC1 Idle Mode Wake-up Description

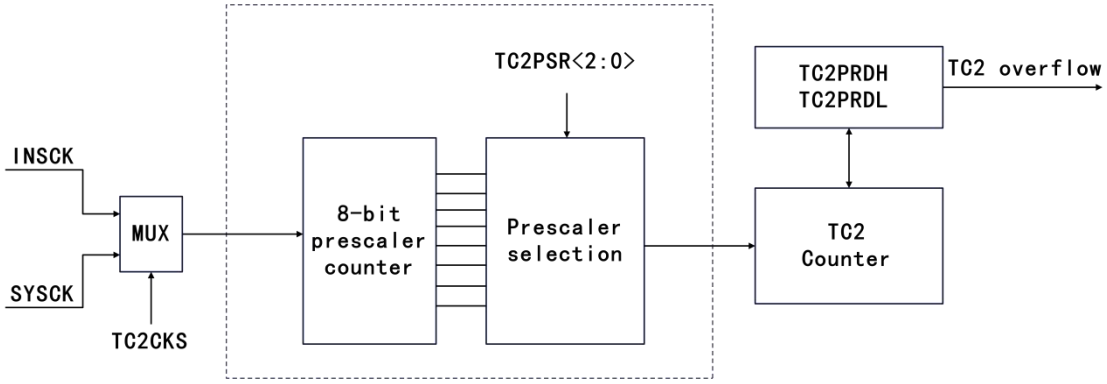
TC1 can wake up the idle mode by enabling bit 4 (TC1WE) of the R188/CPUCON register. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC1 timer continues to operate normally. When the TC1 timer overflows, the system is awakened. If TC1IE and EI are enabled, the system enters an interrupt after waking up; if DI is executed, the system executes the next instruction after waking up.

3.7.3 TC2 Timer Counter

TC2 timer counter provides an 8-bit prescaler. The three bits TC2PSR<2:0> of the TC2CON register determine the prescaler ratio. In TC2 mode, each time TC2EN is enabled, the prescaler register is cleared.

TC2 is a 12-bit up-counter. The TC2 timer requires TC2EN to be enabled to operate. The clock source is the internal system clock, and the counter increments by 1 on each clock cycle. When the TC2 count value matches the TC2PRD set value, an overflow occurs. If TC2IE and EI are enabled, the system jumps to the corresponding interrupt vector address and executes the interrupt service routine.

In IDLE mode, the TC2 interrupt can wake up the circuit (clocked by the system clock). After waking up, it can either enter the interrupt or continue executing the original program. The method refers to the wake-up by port input change.



TC2 Block Diagram

3.7.3.1 TC2 Timer Setting Description

1. Assign an initial value to the TC2PRD<11:0> register;
2. Set the TC2CON register and configure the prescaler ratio as needed;
3. Enable the TC2 interrupt by setting the R1D7/INTE1 register's TC2IE bit, and execute the EI instruction;
4. Enable TC2EN to start the TC2 timer counting;
5. When the system executes the interrupt service routine, it will automatically save the ACC, STATUS, and RSR data. After executing the RETI instruction, the data is automatically restored. Before exiting the interrupt, the TC2 interrupt flag must be cleared;

3.7.3.2 TC2 Timing Calculation Description

The TC2 timing function works by writing a value to TC2PRD<11:0>. The timer starts counting from the initial value 0x01 and increments until the timer count matches the TC2PRD<11:0> value, then overflows and triggers the interrupt service routine.

TC2 timing calculation formula:

$$\text{TC2 Timing duration} = (1/\text{Fosc}) \times (\text{TC2 Prescaler}) \times (\text{TC2PRD} - 1)$$

Example:

Fosc = 16 MHz, TC2 prescaler = 16, TC2PRD value = 512;

$$\text{TC2 Timing duration} = (1/16) \times (16) \times （512 - 1） = 511\text{us}$$

3.7.3.3 TC2 Idle Mode Wake-up Description

TC2 can wake the system from idle mode by enabling the TC2WE bit (Bit 4) in the R188/CPUCON register. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC2 timer continues to operate normally. When the TC2 timer overflows, the system wakes up. If TC2IE and EI are enabled, the system enters the interrupt after waking up; if DI is executed, the system executes the next instruction after waking up.

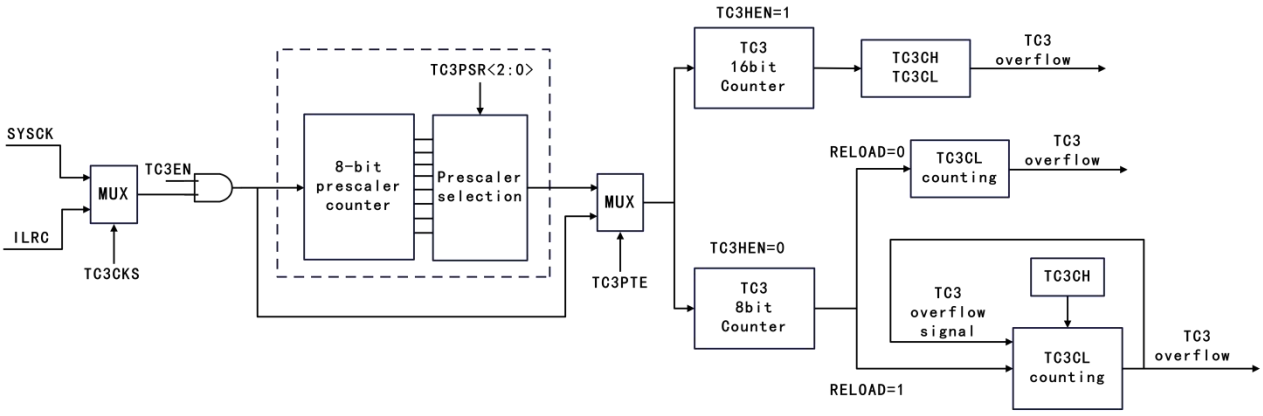
3.7.4 TC3 Timer Counter

TC3 timer counter provides an 8-bit prescaler, and the three bits TC3PSR<2:0> in the TC3CON register determine the prescale ratio.

TC3 is an 8/16-bit up-counter controlled by the TC3HEN high 8-bit counter selection bit. When the 8-bit counter function is selected, the high byte counter TC3CH does not operate, and only the low byte counter TC3CL counts. When RELOAD is enabled, selecting TC3 as an 8-bit reloadable counter, the TC3CH register serves as the reload value register, and TC3HEN is set to 0. The TC3 timer requires TC3EN to

be enabled to operate. The clock source is the internal system clock or a low-speed clock. With each clock cycle, the counter increments by 1. When the TC3 count value overflows, if TC3IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service routine.

In IDLE mode, the TC3 interrupt can wake up the circuit (when the clock source is the system clock). After waking up, it can either enter the interrupt or continue executing the original program. The method refers to the port input change wake-up.



TC3 block diagram

3.7.4.1 TC3 Timer Setting Instructions

1. Assign initial values to the TC3C registers TC3CL and TC3CH;
2. Set the value of the TC3CON register (select clock source and prescale ratio), set TC3HEN=0 to select TC3 as an 8-bit counter function, set TC3HEN=1 to select TC3 as a 16-bit counter function;
3. If selecting TC3 as an 8-bit reloadable counter, set RELOAD=1 in the TC3CON register, set the TC3CH register as the reload value register, and set TC3HEN to 0.
4. After all configurations are set, finally enable the timer counter by setting TC3EN in the TC3CON register;
5. If interrupt functionality is required, set TC3IE (Bit 3) in the INTE1 register to 1 and execute the EI instruction;
6. During system execution, the interrupt service routine will automatically save the ACC, STATUS, and RSR data. After executing the RETI instruction, the data will be automatically restored. Before exiting the interrupt, the TC3 interrupt flag must be cleared;

3.7.4.2 TC3 Timing Calculation Description

The TC3 timing function works by writing values to the TC3CL and TC3CH registers. The timer starts counting from the initial value and increments until it overflows, triggering an interrupt.

TC3 timing calculation formula (8-bit counter mode):

$$\text{TC3 Timing duration} = (1/\text{Fosc}) \times (\text{TC3 Prescaler}) \times (256 - \text{TC3 initial value})$$

Example:

Fosc = 6MHz, TC3 prescaler = 8, TC3 initial value = 100;

$$\text{TC3 Timing duration} = (1/6) \times (8) \times (256 - 100) = 208\ \text{us}$$

TC3 timing calculation formula (16-bit counter mode):

$$\text{TC3 Timing duration} = (1/\text{Fosc}) \times (\text{TC3 Prescaler}) \times (65536 - \text{TC3 initial value})$$

Example:

Fosc = 6MHz, TC3 prescaler = 8, TC3 initial value = 64936;

$$\text{TC3 Timing duration} = (1/16) \times (8) \times (65536 - 64936) = 800\text{us}$$

3.7.4.3 TC3 Idle Mode Wake-up Description

TC3 can wake up the idle mode by enabling TC3WE at bit 6 of the R188/CPUCON register and selecting the system clock as the TC3 clock source. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC3 timer operates normally. When the TC3 timer overflows, the system wakes up. If TC3IE and EI are enabled, the system enters an interrupt after waking up; if DI is executed, the system executes the next instruction after waking up.

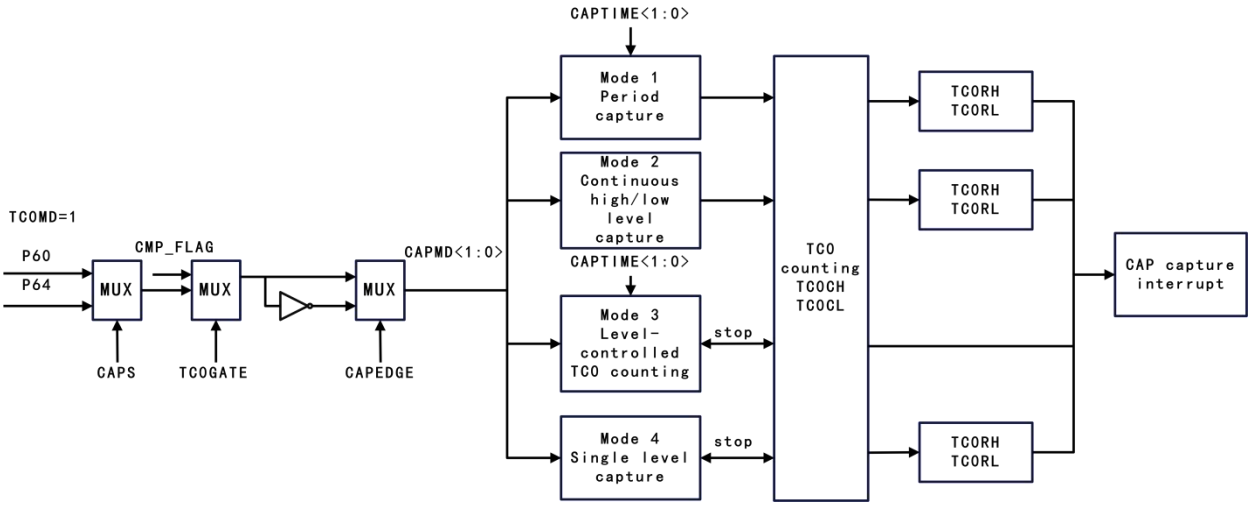
When the clock source is set to ILRC and TC3WE = 1 is enabled, executing the SLEEP instruction directly can also wake up the system.

3.8 TC0 Capture Mode

TC0 timer counter has a capture function. The captured signal source can be the external ports P60, P64, or the comparator output CMPOUT. The TC0MD mode selection bit is set to capture mode, multiplexing the TC0 reload registers TC0RL and TC0RH to store the captured count value. Each capture source group can select either the rising edge or falling edge to set the start of capture and counting. There are four capture modes to choose from, selected by CAPMMD<1:0> in the CAPCON capture control register. This involves selectable cycle count modes, and the count value is selected by CAPIME<1:0>.

Capture can generate an interrupt signal by enabling CAPIE (bit 4) in the INTE1 register.

If the signal period is long, attention should be paid to possible timer counter overflow issues by appropriately setting the timer's working mode and prescaler value to match the signal characteristics.



TC0 capture mode block diagram

3.8.1 TC0 Capture Mode Setting Description

1. Assign initial values to the TC0C registers TC0CL and TC0CR;
2. Set the value of the TC0CON register (select clock source and prescaler);
3. When used as a counter, select the TC0 signal source as an external input signal in the TC0CON register; when selecting the RTC crystal oscillator as the signal source, select RTC mode in the TC0CON register and enable RTC_EN in OPTION;
4. When using capture mode, set TC0MOD to 1 in the CAPCON register for capture mode, set the CAPEDG capture edge selection bit, set CAPS capture input source

or TCOGATET=1, select capture mode CAPMD, and choose the capture count selection bit CAPTIME according to the capture mode;

5. After all configurations are set, enable capture by setting CAPEN, and finally enable the timer counter by setting TCOEN in the TCOCON register;
6. If interrupt functionality is required, set CAPIE (bit 4) in the INTE1 register to 1 and execute the EI instruction;
7. The system automatically saves ACC, STATUS, and RSR data when executing the interrupt service routine. After executing the RETI instruction, the data is automatically restored. Before exiting the interrupt, the CAPIF interrupt flag must be cleared;

3.8.2 Description of TC0 Capture Mode

Bit<3:2>: CAPMD<1:0> - Capture Mode Selection Bits

CAPMD<1>	CAPMD<0>	Capture Mode Selection
0	0	Mode 1
0	1	Mode 2
1	0	Mode 3
1	1	Mode 4

Capture Mode	Capture Mode Description
Mode 1	Periodic capture, selectable number of periods (1, 4, 8, 16)
Mode 2	Continuous capture of high and low levels
Mode 3	Level controls TC0 counting, selectable number of levels (1, 4, 8, 16)
Mode 4	Single level capture

Bit<1:0>: CAPTIME<1:0> - Capture count selection bits

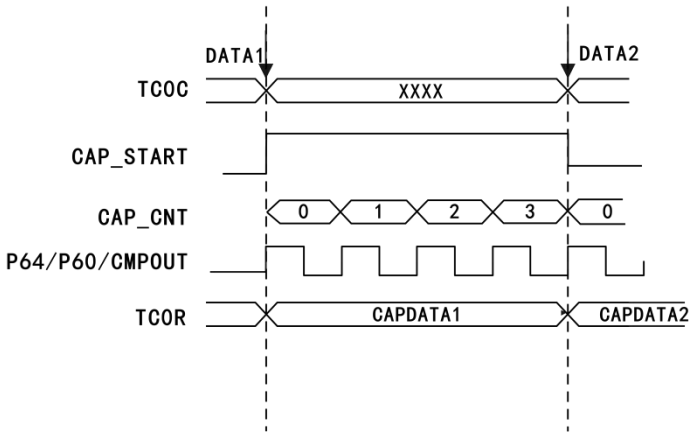
CAPTIME<1>	CAPTIME<0>	Capture count value selection
0	0	1
0	1	4
1	0	8
1	1	16

Mode 1: Period Capture

Period capture can capture the time of one or multiple periods of the input signal. As shown in the period capture mode figure, CAPCON (R1C5) = 0xD1, selecting rising edge trigger to start capture and capturing 4 periods. When the first rising edge

of the capture source arrives, the first count value DATA1 is captured, and the TC0 count value is recorded into TCORL and TCORH. When the fifth rising edge arrives, the second count value DATA2 is captured, and the TC0 count value is recorded into TCORL and TCORH. After that, the capture stops and CAPCON becomes 0. The difference between DATA1 and DATA2 can be used to accurately measure the capture source signal. The TC0 counter does not stop counting during this period.

If the capture interrupt enable is set, the interrupt routine can be entered at both capture events.



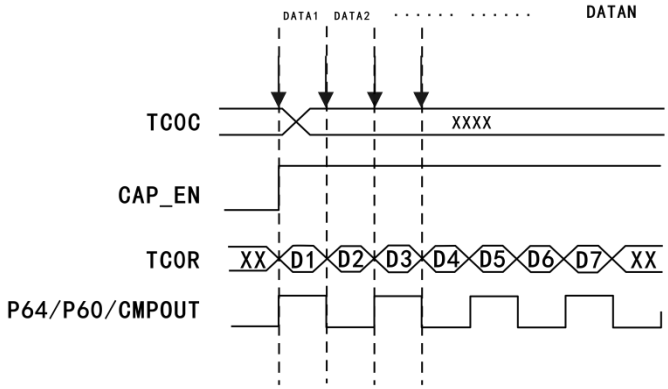
Mode 1

Mode 2: Continuous High-Low Level Capture

Continuous high-low level capture can monitor and record the moments and durations of high and low level changes of the capture source signal.

As shown in the continuous high-low level capture mode figure, CAPEDGE can be set to 1 or 0, and TC0 counts normally. Whenever the capture signal source generates a high or low level change, the current count value DATA is captured and recorded into TCORL and TCORH. The TC0 counter does not stop counting.

If the capture interrupt enable is set, the interrupt routine can be entered at each capture event.

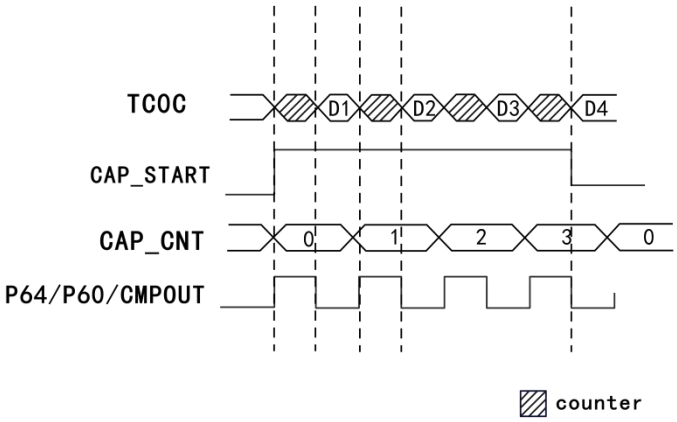


Mode 2

Mode 3: Level-Controlled TC0 Counting

Level-controlled counter counting can control TC0 counting under high level or low level conditions. CAPEDG can select high level or low level to enable counting. As shown in the figure below, CAPCON = 0xD9, counting occurs during 4 periods of high level. When the high level changes to low level, TC0 counting stops, and the counter's count value is held as DATAn. In the next high level, the TC0 counter continues counting based on DATAn. The number of enabled counting levels can be set by CAPTIME<1:0> capture count selection bits. Within the corresponding number of levels, the TC0 counter stops counting, and capture enable will automatically turn off. If a counter overflow occurs during level counting, the enabled interrupt wake-up can normally enter the interrupt or wake up the system. If the capture interrupt CAPIE is enabled, the capture interrupt routine can be entered at the end of the last level count.

If CAPEDGE is changed to 1, counting occurs during the low level period, and counting stops during the high level period.

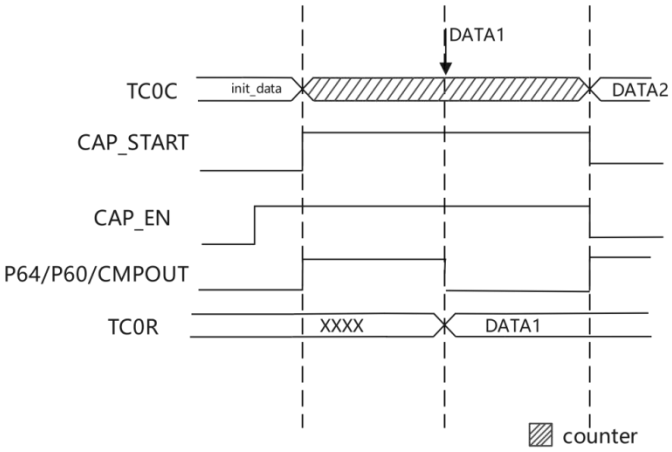


Mode 3

Mode 4: Single-Level Capture

Single-level capture can monitor the external capture source signal. In the figure below, when CAPCON=0xDC, the TC0 counter starts timing when the signal reaches and holds at the preset level (for example, high level), until the signal switches to another level (becomes low level). At this time, the count value DATA1 is saved in TC0RL and TC0RH (the TC0 counter does not stop), which is used to determine the duration of that level state. If a counter overflow occurs during counting, enabling interrupt wake-up allows normal entry into the interrupt or system wake-up. If the capture interrupt CAPIE is enabled, a capture interrupt program can be entered when a capture occurs.

In this mode, counting only occurs within one cycle of the capture source signal. After the cycle ends, the TC0 counter stops counting, and capture enable is automatically turned off. If CAPEDGE is changed to 1, capture occurs when the low level changes to high level.



Mode 4

3.9 PWM Pulse Width Modulation

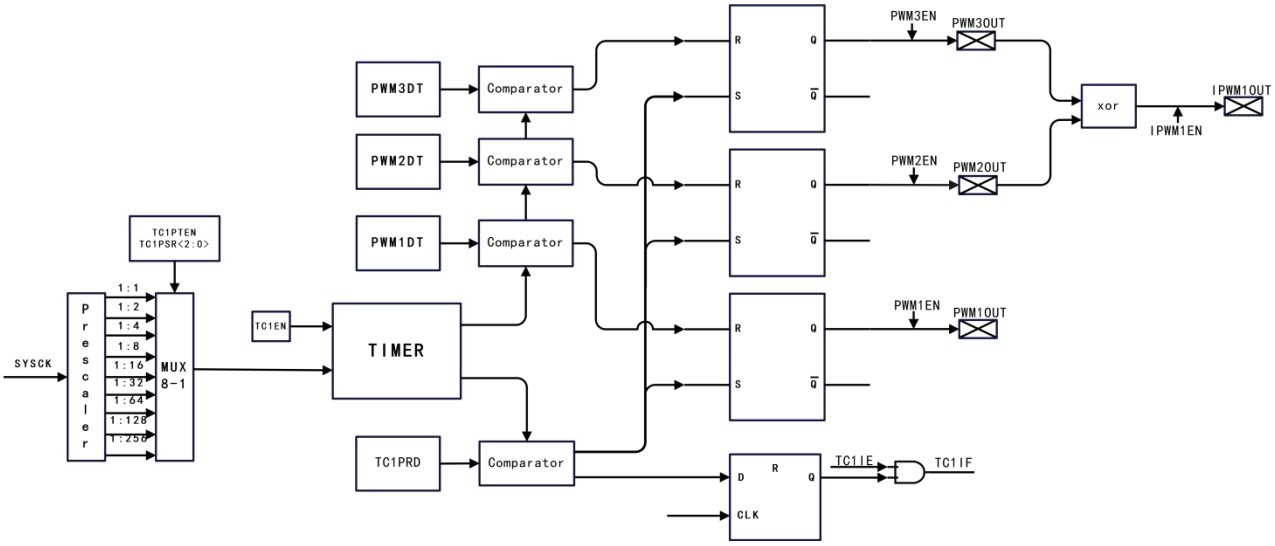
The JZ8M4601 provides 2 groups of 12-bit TC1 and TC2 counters. Each group of counters can be divided into three PWM channels to generate pulse width modulation signals. The PWM output waveform is determined by the period and duty cycle, with the transmission rate being the reciprocal of the period. The chip provides dead-zone complementary output, which after XOR operation between PWM2 and PWM3 serves as IPWM1, and together with PWM1 forms the dead-zone complementary signal. (IPWM4 is the same as IPWM1)

PWM has a period overflow interrupt, which can jump to the interrupt when enabled.

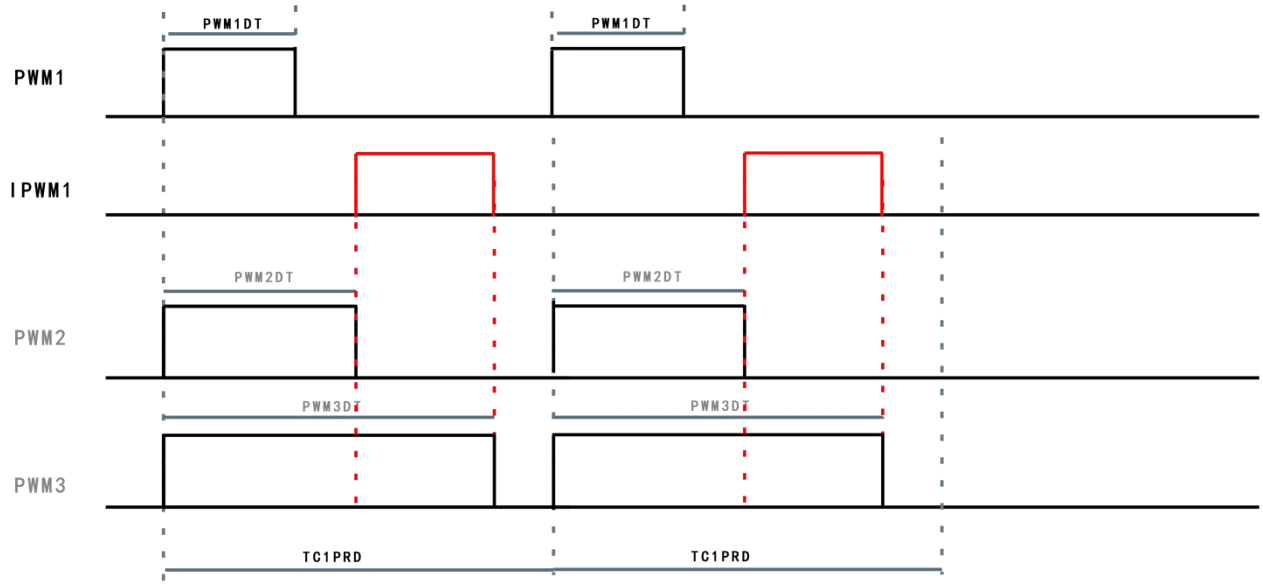
In IDLE (idle mode), TC1 and TC2 can wake up the system by selecting TC1CKS=1 and TC2CKS=1 in the TC1 and TC2 control registers and enabling TC1WE and TC2WE in the CPU mode control register.

3.9.1 PWM Internal Structure and Timing

The following internal block diagram is for reference and understanding only and does not represent the actual circuit.



PWM working structure circuit



Explanation of 3-Channel Synchronous PWM and IPWM Timing

3.9.2 PWM Period and Duty Cycle

The PWM provides a 12-bit clock counter with an 8-bit programmable prescaler, serving as the baud rate clock generator for the PWM module. The counter function can be enabled by setting TCxEN in the PWM control register. The prescaler for the counter can be configured via the control bits TCxPSR<2:0>. INVxH and INVxL control the inversion of the output pins, while PWMxE and IPWMxE enable the PWM function and the complementary PWM function, respectively.

The PWM period is set by writing values to the TCxPRDL (lower eight bits) and TCxPRDTH (upper four bits) period registers. When the counter value equals the PRD value, the following events occur at the next increment cycle:

- The counter is cleared to zero;
- The corresponding PWM output pin is set to a high level;
- A PWM period overflow interrupt is generated (if enabled);
- The PWM duty cycle is latched from the PWMxDTL/TCxPRDTH registers into the DT/TIMER compare register;

PWM period calculation formula:

$$\text{PWM period} = (\text{PRD}) \times (\text{PWM_CK}) \times (\text{PWM prescaler})$$

Example:

PWMxRD=100, Fosc=16MHz, PWMCKS=1, PWM prescaler selection = divide by 2;

$$\text{PWM period} = (100) \times (1/16) \times (2) = 12.5\ \text{us}$$

The PWM duty cycle is set by writing to the PWM duty cycle register. When the counter overflows and resets to zero, the value of PWMxDT is latched into the DT/TIMER

compare register. When the value in the DT/TIMER compare register equals the TIMER counter value, the PWM output pin is set to a low level. The value of PWMxDT can be written at any time, but the DT/TIMER compare register is only updated on period overflow:

PWM duty cycle calculation formula:

$$\text{PWM duty} = (\text{DT}) \times (\text{PWM_CK}) \times (\text{PWM prescaler})$$

Example:

PWMxDT=50, Fosc=16MHz, PWMCKS=1, PWM prescaler selection=divide by 2;

$$\text{PWM duty} = (50) \times (1/16) \times (2) = 6.25\ \text{us}$$

3.9.3 PWM Idle Mode Wake-up Description

In idle mode, CPU instructions stop executing, modules with wake-up functions and the system clock operate normally, while other functions are disabled.

PWM can wake up from idle mode by setting TC1/TC2WE wake-up enable and selecting the clock source as the system clock (SYSCK). Enable the corresponding period or duty cycle interrupt, set IDLE (R188) to 1, and use the SLEEP instruction to enter idle mode; the PWM timer operates normally.

When the corresponding interrupt condition is met, the system wakes up. If EI is enabled, it enters an interrupt after waking up; if DI is enabled, it executes the next instruction after waking up.

3.9.4 PWM Comparator Gating Description

The gating function of PWM1 is controlled by PWM1GATE in the TC1CON register. When PWM1GATE=1, PWM1 output is controlled by the comparator result, and the PWM waveform is output when CMP_FLAG=0.

The gating function of PWM4 is controlled by PWM4GATE<1:0> in the TC2CON register. When PWM4GATE<0>=1, PWM4 output is controlled by the comparator result, and the PWM waveform is output when CMP_FLAG=0. When PWM4GATE<1>=1, PWM4 output is controlled by the external interrupt EXINT (P50 or P54), and the PWM waveform is output when EXINT=1.

3.9.5 IPWM Waveform and Buzzer Setting Description

The IPWM waveform is not directly inverted; instead, IPWM1EN is enabled, and the output is generated by XORing PWM2 and PWM3. When IPWM1EN is enabled, the output can be selected from P61/P67 through the PWM2 output selection control bit; when PWM3EN is enabled, the output can be selected from P55/P65 through the PWM3 output selection

control bit. Enabling both supports simultaneous output of the IPWM1 waveform from two ports.

Similarly, enabling IPWM4EN outputs the XOR of PWM5 and PWM6. If PWM5EN is enabled, the output can be selected from P52/P63 through the PWM5 output selection control bit; if PWM6EN is enabled, the output can be selected from P50/P64 through the PWM6 output selection control bit. Enabling both supports simultaneous output of the IPWM4 waveform from two ports.

The PWM module also includes a buzzer function. Users can enable PWM output for the buzzer via the BZXEN (R1B7, R1BF) control bit. The buzzer port can be selected through PWM1S (R1B7) and PWM4S (R1BF), outputting respectively from ports P60/P66 and P51/P62. It should be noted that enabling the buzzer requires clearing PWM1EN and PWM4EN and setting the corresponding output ports as outputs.

3.9.6 PWM2DT Interrupt and ADC Trigger Description

PWM2DT provides a duty cycle triggered interrupt function. After enabling PWM2DTIE (R1D6) and executing the EI instruction, the interrupt routine can be entered based on the configured PWM2 duty cycle.

The PWM can trigger ADC conversion through the PWM2 duty cycle. By setting the ADCGATE (R1A7) bit to 1, the ADC conversion will be triggered on the falling edge of the PWM2 duty cycle.

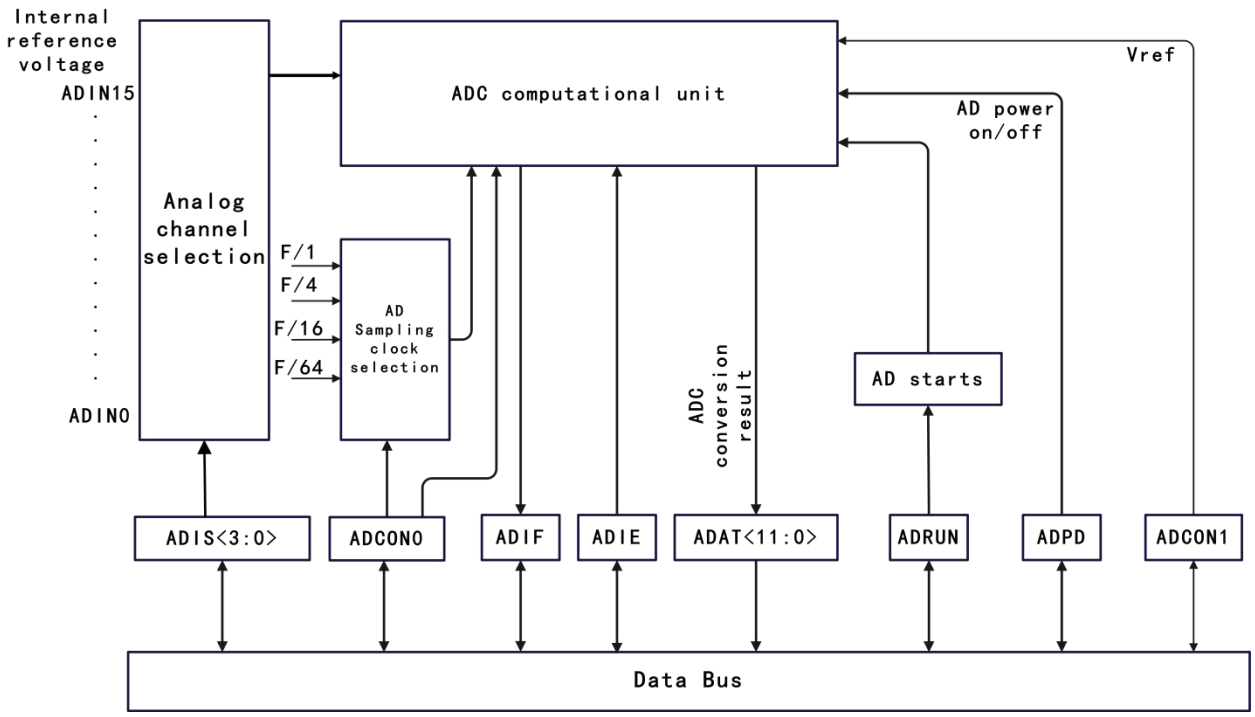
3.10 ADC Analog-to-Digital Conversion

The JZ8M4601 ADC module provides a 12-bit precision SAR AD converter with 15 analog channels.

The ADC converter uses a successive approximation analog-to-digital conversion method. The results are stored in R1A3/ADATH (high 8 bits of ADC result register), R1A4/ADATL (low 8 bits of ADC result register), and R1A5/ADCON0 (ADC control and high 4 bits register). The channel selection, zero calibration, internal/external reference voltage source, sampling clock, ADC start, and ADC power consumption are configured through the ADCON0 and ADCON1 control registers.

When AD conversion is complete, it can trigger an interrupt or be polled by checking the ADRUN bit in R1A7/ADCON1.

If the AD wake-up function is enabled, the completion of AD conversion can wake the system from sleep mode or idle mode.



AD conversion function diagram

AD sampling time calculation method:

From setting ADRUN=1, the time to complete one AD sampling = ADC sampling hold period + AD conversion time

AD conversion time:

AD conversion requires one TAD time per bit. The chip has a built-in 12-bit AD, so the conversion time is 12 TADs.

AD sampled voltage value calculation:

$$\text{ADC sampling voltage} = \frac{\text{Sample value}}{4096} * \text{Reference voltage}$$

Example: Reference voltage is internal reference 3V, sampled value is 0x800=2048

$$\text{ADC sampling voltage} = \frac{2048}{4096} * 3 = 1.5\text{V}$$

3.10.1 ADC power supply voltage detection description

By configuring the ADCCON1 (R1A6) register, channel selection bits ADIS<4:0>=10000 select 0.254*VDD as the sampling channel, VREF<2:0> selects the reference voltage, and the conversion result is obtained through ADC conversion. The voltage value of VDD can be derived as:

$$\text{Conversion result} = ((0.254 * \text{VDD})/\text{VREF}) \times 4096$$

Then

$$\text{VDD} = \text{Conversion result} * \text{VREF}/4096/0.254$$

3.10.2 ADC Analog-to-Digital Conversion Settings Description

1. Enable ADC input ports and select analog channels by setting registers R1A0/P5ADE, R1A1/P6ADE, and R1A6/ADCON1;
2. Set ADC reference voltage source, clock prescaler, and reference voltage selection by configuring registers R1A5/ADCON0 and R1A6/ADCON1;
3. If interrupt functionality is required, set ADIE=1 and execute the "EI" instruction;
4. Set "ADEN=1" to start the AD power supply voltage;
5. Call the AD accuracy calibration subroutine;
6. Select IDLE/SLEEP mode as needed, set AD wake-up function by enabling ADCWE=1;
7. Set "ADRUN=1" to start AD conversion;
8. Wait for interrupt or for ADRUN to be cleared to 0. If an AD interrupt occurs, clear ADIF when exiting the interrupt routine;
9. Save the conversion result. If multiple AD conversions are needed, return to step 7;

3.10.3 Explanation of ADC Analog-to-Digital Conversion Accuracy Calibration

1. Based on steps 1 to 4 of section 3.10.2 ADC analog-to-digital conversion settings, enable ADC compensation calibration CALI;

2. Set the ADC compensation voltage polarity SIGN, first calibrate the ADC positive voltage, then calibrate the ADC negative voltage, calibrating each time Compensation amplitude of 2LSB;
3. Continuously monitor the AD value; if the result is "0", end the AD accuracy calibration and set the ADC's "CALI" position to 0;

3.11 LCD/LED Drive

The JZ8M4601 chip has a built-in LCD/LED driver module, with LCD and LED sharing control registers and display data RAM. Mode switching can be done via the LCDMD (R1E6) bit.

The JZ8M4601 LCD module has 4 common pins and 16 segment pins. Each SEG pin has a corresponding register enable bit, controlled through the R1E7 and R1E8 registers, allowing independent control of each individual SEG pin. The COM port used for the corresponding duty cycle needs to be set as an input pin to ensure normal common drive output.

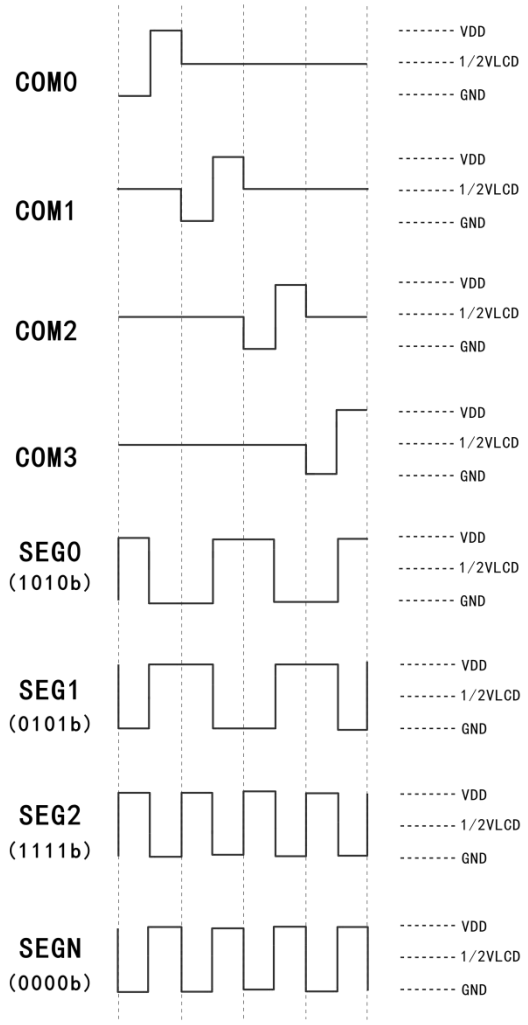
In LCD driving, the timing controller sets the timing for display access and duty cycle based on the subsystem clock to meet display requirements. R1E6 is the control register of the LCD driver, which includes controls for LCD enable/disable, LCD/LED selection, duty cycle (1/2, 1/3, 1/4), drive waveform selection, clock source, and LCD frame frequency. The lower 4 bits of the R180 register are the LCDRAM address selection bits, and R1E9 is the LCDRAM data register. After selecting the LCDRAM address, reading and writing to the R1E9 register is equivalent to operating on the LCDRAM at the same address. The common drive terminal defaults to a 1/2 VDD bias.

The following is a schematic explanation of the structure of the LCD/LED display RAM:

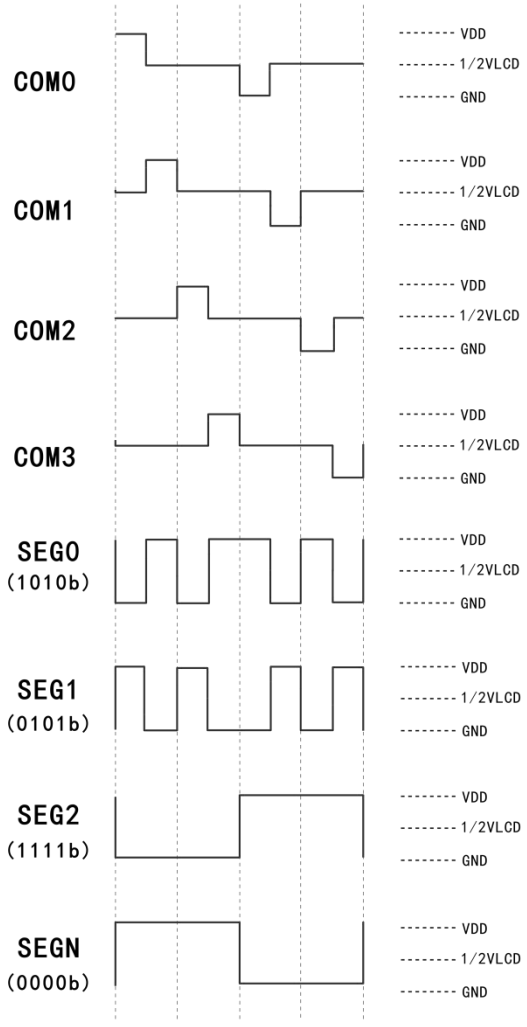
LCD/LED RAM Address	LCD Data Register					Section
	Bit7-4	Bit3	Bit2	Bit1	Bit0	
00H	X	-	-	-	-	SEG0
01H	X	-	-	-		SEG1
02H	X	-	-	-	-	SEG2
03H	X	-	-	-	-	SEG3
04H	X	-	-	-	-	SEG4
05H	X	-	-	-	-	SEG5
06H	X	-	-	-	-	SEG6
07H	X	-	-	-	-	SEG7
08H	X	-	-	-	-	SEG8
09H	X	-	-	-	-	SEG9
0AH	X	-	-	-	-	SEG10
0BH	X	-	-	-	-	SEG11
0CH	X	-	-	-	-	SEG12
0DH	X	-	-	-	-	SEG13
0EH	X	-	-	-	-	SEG14
0FH	X	-	-	-	-	SEG15

	X	COM3	COM2	COM1	COM0	COM / SEG

The following are the LCD waveforms of type A and B with 1/2 bias and 1/4 duty cycle respectively



1/4 duty cycle, 1/2 bias
Type A



1/4 duty cycle, 1/2 bias
Type B

3.12 UART Receiver/Transmitter

The Universal Asynchronous Receiver/Transmitter (UART) serial port is a serial I/O communication peripheral. The serial interface is used for low-speed data transmission and communication with low-speed peripheral devices. The JZ8M4601 supports one-byte data length, with a transmission format consisting of a start bit, 8 data bits, a parity bit, and a stop bit. The programmable baud rate supports peripherals operating at different speeds.

There are mainly three serial communication modes, selected by the two highest bits of the SCON0 (R1E3) register.

Mode 1: 8-bit asynchronous full-duplex communication mode, consisting of one start bit and 8 data bits. The transmit and receive baud rate can select the overflow signal of TC0 or TC3 as the clock source.

Mode 2: 9-bit asynchronous fixed baud rate communication mode, consisting of one start bit and 8+1 data bits. The transmit and receive baud rate can select the system clock divided by 32 or 64, chosen via the SMOD control bit in the SCON2 (R1E5) register.

Mode 3: 9-bit asynchronous variable baud rate communication mode, consisting of one start bit and 8+1 data bits. The transmit and receive baud rate can select the overflow signal of TC0 or TC3 as the clock source.

Before communication, UART must first initialize the serial port control register, select the working mode and baud rate. If it is mode 1 or mode 3, the timer TC0/TC3 must also be initialized first.

In all modes, any write operation to the UART transmit/receive data register SBUF will start transmission.

UART mode list:

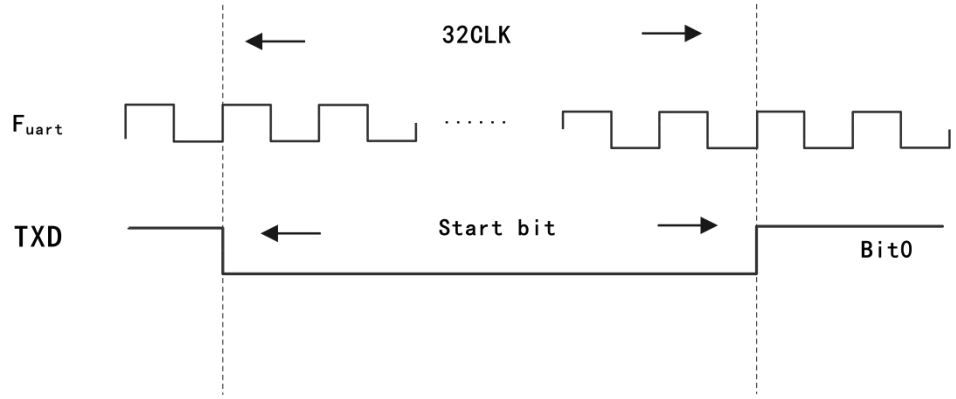
SM<0:1>	Mode	Type	Baud rate	Frame length	Start bit	Stop bit	9th bit
01	1	Asynchrono	TC0/TC3 Overflow	10 bits	1 bit	1 bit	-
10	2	Asynchrono	SYSCK 32 Division / 64 Division	11 bits	1 bit	1 bit	0/1
11	3	Asynchrono	TC0/TC3 Overflow	11 bits	1 bit	1 bit	0/1

3.12.1 UART Transmission

The main operations for UART serial data transmission are as follows:

1. Configure the UART serial control registers SCON0 (R1E3) and SCON1 (R1E5), selecting the corresponding mode, port, and baud rate.
2. Write data into the UART transmit/receive data register SBUF (R1E4).
3. UART will start transmitting.
4. Data will be sent serially from the TX pin, with the transmitted data output from LSB to MSB.
5. Stop bit: output one stop bit (“1”).

The following figure shows the UART transmit counter timing (32CLK is for reference only; the baud rate can be selected via configuration bits).

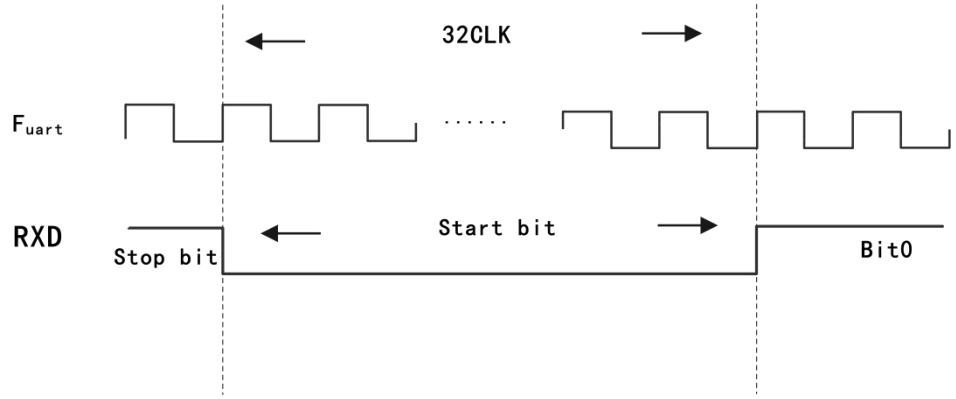


3.12.2 UART Reception

The main operations of UART serial data reception are as follows:

1. Set the REN bit of the SCON0 register high to enable the UART receive function. UART monitors the RXD pin and performs internal synchronization upon detecting the start bit.
2. Start bit: output a “0” bit.
3. The received data is shifted into the UBUF register in order from LSB to MSB.
4. The parity bit can be selected by the SCON0 register, outputting a parity bit.
5. Stop bit: output one stop bit (“1”).
6. Receive the parity bit and stop bit. After receiving the last character, the RI bit in the SCON0 register will be set to “1”.
   If the UART interrupt is enabled and EI is enabled, a UART interrupt will occur.
7. Read the received data from the SBUF register. The RI bit should be cleared by software (if the interrupt is enabled).

The following figure shows the UART receive counter timing (32CLK is for reference only; the baud rate can be selected through configuration bits).



3.13 CMP Comparator

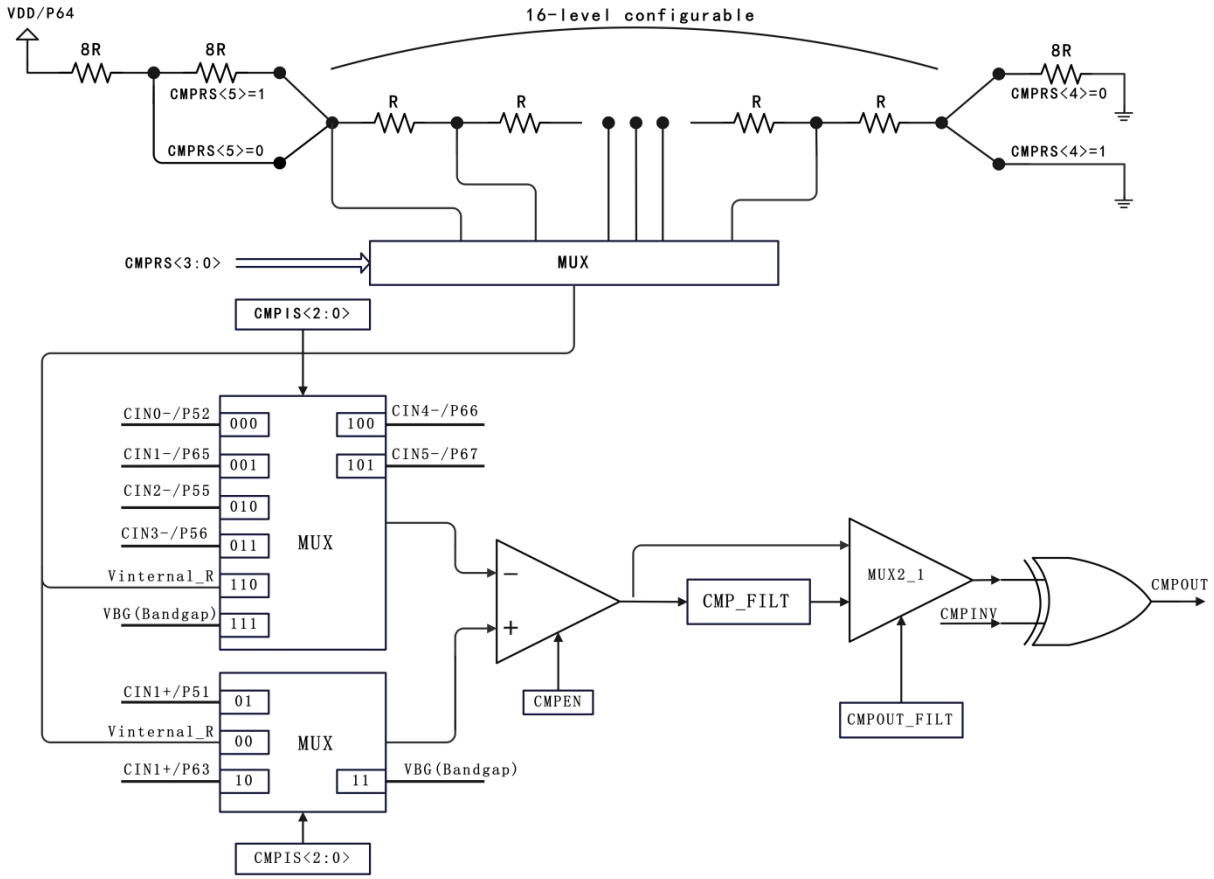
The JZ8M4601 has a built-in hardware comparator that can compare any two of the three inputs: input pins, internal reference voltage V_internal R, and the built-in Bandgap (1.29V). One is selected as the positive input and the other as the negative input. The negative input of the comparator can be P52, P55, P56, P65, P66, P67, a voltage divider resistor (selected by CMPRS<5:0>), or the built-in Bandgap (1.29V). The positive input can be P51, P63, or a voltage divider resistor (selected by CMPRS<5:0>). (The same port cannot be used simultaneously as both positive and negative inputs, and the voltage divider resistor input source cannot be used simultaneously as both positive and negative inputs.)

The voltage divider resistor input source can be configured via the CMPCON control register to select the input voltage source as either the P64 pin input or VDD.

The comparator output can be selected to output on the P61 pin, supporting output inversion. The chip supports digital filtering of the output result, which can be selected in the OPTION register.

The comparator supports triggering an interrupt on output result changes. Enabling CMPIE can generate an interrupt signal.

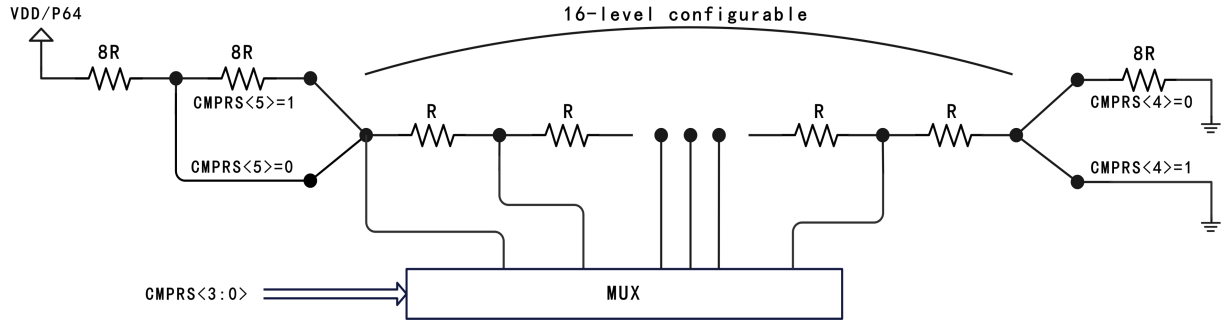
The comparator supports waking up on output result changes. Enabling CMPWE can wake the idle mode and sleep mode. In idle and sleep modes, if CMPEN is enabled, the low-speed oscillator will be enabled, causing higher sleep power consumption.



Comparator Schematic Description

3.13.1 Voltage Divider Resistor Output Voltage V_internal R

The voltage divider resistor output voltage V_internal R is composed of a series of resistors that can generate different levels of reference voltage. CMPRS<5:0> collectively determine the magnitude of V_internal R. CMPRS<5> and CMPRS<4> select the highest and lowest values of V_internal R, while CMPRS<3:0> is used to select the desired voltage level. The range between the highest and lowest values of V_internal R is divided into 16 equal parts, from which CMPRS<3:0> selects.



Comparator Adjustment Diagram

Example 1: CMPRS<5>=0, CMPRS<4>=0

Value Range: $V_{internal\ R} = (3/4) * VDD \sim (1/4) * VDD + (1/32) * VDD$

Calculation Formula: $V_{internal\ R} = (1/4) * VDD + \frac{(n+1)}{32} * VDD$

Example 2: CMPRS<5>=0, CMPRS<4>=1

Value Range: $V_{internal\ R} = (2/3) * VDD \sim (1/24) * VDD$

Calculation Formula: $V_{internal\ R} = \frac{(n+1)}{24} * VDD$

Example 3: CMPRS<5>=1, CMPRS<4>=0

Value Range: $V_{internal\ R} = (3/5) * VDD \sim (1/5) * VDD + (1/40) * VDD$

Calculation Formula: $V_{internal\ R} = (1/5) * VDD + \frac{(n+1)}{40} * VDD$

Example 4: CMPRS<5>=1, CMPRS<4>=1

Value Range: $V_{internal\ R} = (1/2) * VDD \sim (1/32) * VDD$

Calculation Formula: $V_{internal\ R} = \frac{(n+1)}{32} * VDD$

n=CMPRS<3:0>

3.13.2 Comparator Configuration

When using the comparator, CMPEN must be enabled (this will activate the LRC used to filter the output result CMPOUT, which increases power consumption). Set CMPIS<5:0> to select the positive and negative input sources, and configure the ports for the positive and negative inputs as inputs. The same port cannot be used simultaneously as both positive and negative input, and the resistive voltage divider input source cannot be used as both positive and negative input at the same time.

If a resistive voltage divider is selected as the input source, set the register CMPRS<5:0> as needed to select the desired voltage output Vinternal R of the voltage divider for comparison.

Example 1:

Select P52 as the negative input and the voltage of Vinternal R as (18/32)*VDD as the positive input. Configure Vinternal R by setting CMPRS<5>=0, CMPRS<4>=0, and CMPRS<3:0>=4b’1001 (n=9) to obtain

Vinternal R = (1/4)*VDD + [(9+1)/32]*VDD = (18/32)*VDD

After configuration is complete, enable bit 7 CMPEN of the CMPCON0 (R1EA) control register to start the comparator. The comparison result can be output through port P61 by setting bit 7 CMPOE of the CMPCON1 (R1EB) control register (P61 must be set as output). The output result can also be inverted by setting bit 6 CMPINV of the same control register.

3.13.3 Bandgap Usage Method

The built-in Bandgap reference voltage provides 1.29V and can be used to measure the external power supply voltage level. This is achieved by selecting the Bandgap reference voltage as the negative input and comparing it with the positive input Vinternal R. By setting the power supply of Vinternal R to VDD and adjusting the voltage level of Vinternal R to compare with the Bandgap reference voltage, the voltage of VDD can be determined. If n (decimal value of CMPRS[3:0]) makes Vinternal R closest to 1.29V, taking the four cases in section 3.10.1 as examples, the voltage of VDD can be calculated by the following formula:

For using Case 1: VDD = [32/(n+9)] * 1.29V;

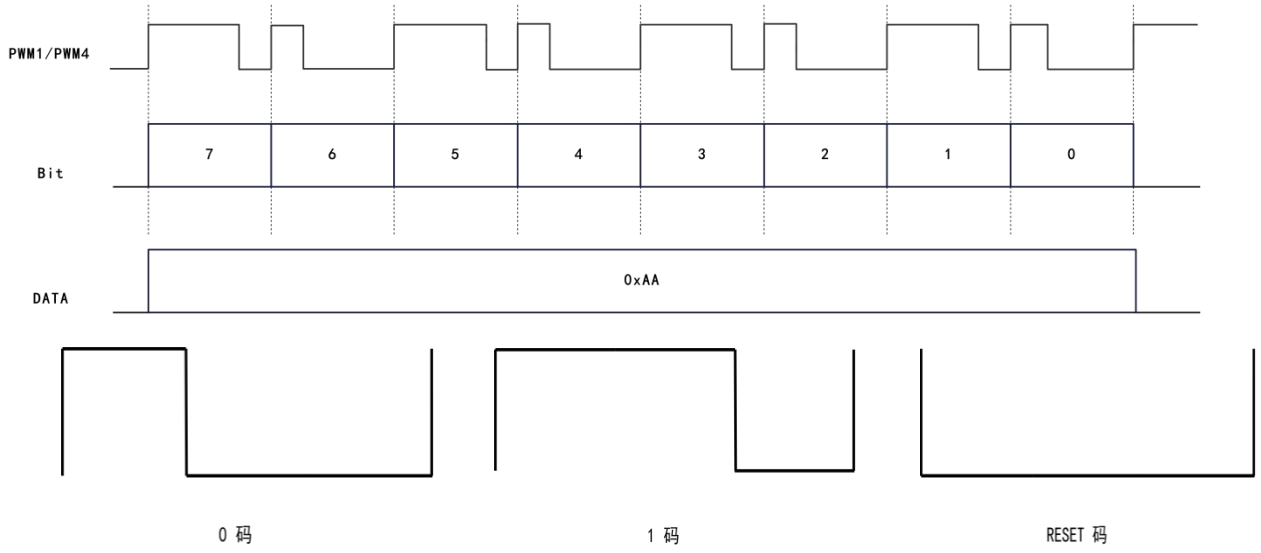
For using Case 2: VDD = [24/(n+1)] * 1.29V;

For using Case 3: VDD = [40/(n+9)] * 1.29V;

For using Case 4: VDD = [32/(n+1)] * 1.29V;

3.14 Single-wire LED Cascading

JZ8M4601 supports 2 channels of single-wire cascaded LED driving, outputting cascade control timing through PWM1 and PWM4 ports. The timing diagram for cascaded LED driving is as follows:



Single-wire Cascaded LED Timing Description

PWM1 and PWM4 are two independent single-wire cascaded LED drive controls. When using PWM1 as the LED drive control, the 0/1 code cycle is set by the TC1PRD period register; the high-level time of the 0 code is set by the PWM1 duty cycle register; the high-level time of the 1 code is set by the PWM2 duty cycle register; the data to be sent is set by the lower 8 bits of the PWM3 duty cycle register. After enabling PWM1_LEDEN (R186) + TC1EN, the 8-bit cascade data transmission begins, and the data is output from the PWM1 port. After the 8-bit cascade data transmission ends, TC1EN automatically resets to zero. Re-enabling TC1EN starts the transmission of the next 8-bit cascade data.

When using PWM4 as the LED drive control, the 0/1 code cycle is set by the TC2PRD period register; the high-level time of the 0 code is set by the PWM4 duty cycle register; the high-level time of the 1 code is set by the PWM5 duty cycle register; the data to be sent is set by the lower 8 bits of the PWM6 duty cycle register. After enabling PWM4_LEDEN (R186) + TC2EN, the 8-bit cascade data transmission begins, and the data is output from the PWM4 port. After the 8-bit cascade data transmission ends, TC2EN automatically resets to zero. Re-enabling TC2EN starts the transmission of the next 8-bit cascade data.

3.15 EEPROM and ISP Programming

3.15.1 EEPROM Read and Write Operations

The JZ8M4601 has a built-in 128 Byte 16-bit EEPROM data memory, with factory default data set to 0xFFFF. It supports real-time reading or writing of data by the user program during powered operation. When writing data, the MCU will halt instruction execution and resume after the write is complete. During simulation, the EEPROM window cannot read values, but the programmer supports direct reading of the EEPROM.

Writing EEPROM:

Before writing to an EEPROM cell, the user must first write the address into the TBRDL register to select the EEPROM address. Then, write values to the EEPROM data registers E2PDATL/E2PDATH. Finally, unlock the EEPROM write operation by opening E2PLOCK and set the E2PWR bit to 1. Once a write process starts, clearing the E2PWR bit will not affect the write cycle. When the write cycle completes, the E2PWR bit will be cleared by hardware and must be set again by the user before the next write.

Note: During EEPROM writing, the instruction clock stops, and the MCU does not execute any instructions. The high-speed oscillator and low-speed oscillator continue to run normally, and the system clock remains normal;

Reading EEPROM:

To read an EEPROM memory cell, the user must first write the address into the TBRDL register and set the E2PRD bit in the E2PCON register to 1. After enabling the read control bit, execute the TBRD instruction. The data from the EEPROM will be stored in the corresponding R register (high 8 bits) and ACC register (low 8 bits).

3.15.2 ISP Programming

The JZ8M4601 supports three different programming methods: conventional programming (off-board), on-board programming without power, and on-board programming with power. On-board programming with power requires the user to pre-configure the programming ports and programming functions.

1、 Conventional programming (off-board):

In the OPTION settings, select [P53/P54 not used as programming ports, on-board powered programming not supported] for [Programming Port Settings], and select [Conventional programming (programmer powered)] for [Programming Function Selection]. These configurations do not affect the use of ports P53/P54.

2、 On-board programming without power:

OPTION setting [Programming Port Setting] select [P53/P54 not used as programming ports, in-circuit powered programming not supported], OPTION setting [Programming Function Selection] select [Regular Programming (programmer powered programming)]. With the above configuration, P53/P54 should preferably be set as input ports to avoid external components such as transistors or MOSFETs.

3、 In-circuit powered programming:

In-circuit powered programming supports two programming methods. The MCU needs to pre-select "Regular Programming" to program the firmware. In the in-circuit powered programming mode, the programmer must connect three lines: GND, P53, and P54; VDD must not be connected. The following two programming methods are supported.

Method 1: P53/P54 used as programming ports only during reset, program can use them

OPTION setting [Programming Port Setting] select [P53/P54 used as programming ports only during reset (program can use)], OPTION setting [Programming Function Selection] select [In-circuit powered programming]. The instruction clock (Fcpu) frequency must be greater than 1M (e.g., IRC frequency = 16M, Clocks division = 4 Clocks). With the above configuration, P53/P54 can be used as normal GPIOs. The program needs to configure specific registers and enable external interrupt 0 (EXINT0) to receive clock data sent by the programmer. After correct decoding, the software unlocks the ISP function. See the ISP demo for details.

Software unlocking of ISP mainly consists of the following two steps:

1) The program writes 0110 to the high 4 bits E2PLOCK<3:0> of the E2PCON (0x1E0) register to complete the first unlock step;

2) The program writes 0xC5 to the E2PDATH (0x1E2) register and then writes 0x3A to the E2PDATL (0x1E1) register to complete the second unlock step;

After completing the two unlock steps, the MCU hardware sets P53 and P54 as input ports, waiting for external timing to control MCU reset.

Method 2: P53/P54 used only as programming ports, program not controllable

OPTION setting [Programming Port Configuration]: select [P53/P54 used only as programming ports (hardware pull-up program uncontrollable), the chip can enter programming mode at any time]. OPTION setting [Programming Function

Selection]: select [On-board powered programming]. With the above configuration, P53/P54 need to be left floating. If Type-C port upgrade is required, P53/P54 should be connected to the CC1/CC2 ports.

Note: The P53/P54 programming pins have a default hardware pull-up, which cannot be controlled by the program. External pull-down will cause leakage current.

According to the Type-C port model, select the appropriate powered programming method. Taking Type-C port powered programming as an example:

1) If P53/P54 are connected to the Type-C port's CC1/CC2 with pull-down resistors, please choose Method 1 with software control;

2) If the Type-C port's CC1/CC2 has no pull-down resistors, please choose Method 2;

3) If P53/P54 are connected to the Type-C port's D+/D-, please choose Method 2;

3.16 RFC Resistor Frequency Conversion

The JZ8M4601 has a built-in RFC resistor frequency conversion function, which uses the comparator's comparison result to control TC0 capture, achieving time counting of external voltage changes.

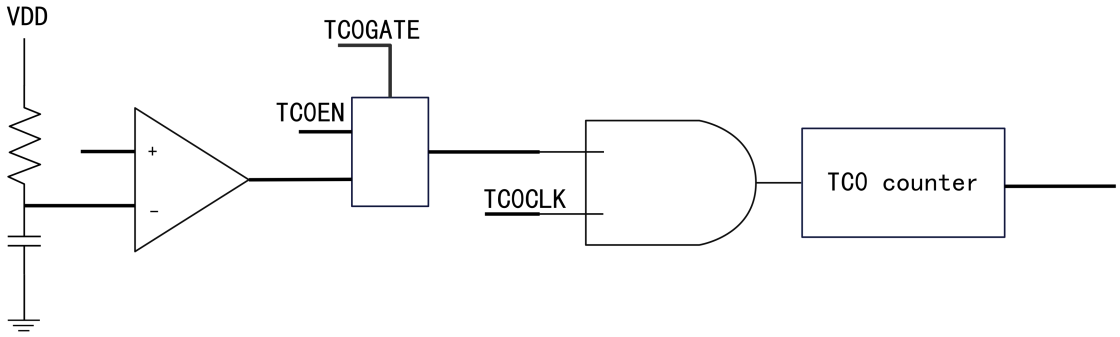
RFC Principle:

The voltage change at the RFC port affects the comparator's output. When the TC0GATE bit in the EXIN TCON register is enabled, the TC0 count is controlled by the comparator output CMPOUT. When the RFC port voltage is lower than the comparator's positive input voltage, CMPOUT=1 and TC0 starts counting; when the RFC port voltage is higher than the comparator's positive input voltage, CMPOUT=0 and TC0 stops counting. The TC0 count value records the time for the RFC port voltage to charge to the preset voltage (the comparator's positive input voltage).

Application Steps:

1. Set the P5P7AE, P6AE registers to select the analog port of the comparator;
2. Set the CMPCON0, CMPCON1 registers to configure the positive input source of the comparator as a fixed voltage and the negative input source as an external port (as shown in the diagram);
3. Set the port of the comparator's negative input source to output a low level to discharge the port capacitance;
4. Clear the initial value of the TC0 timer;

5. Set the port of the comparator's negative input source as an analog input port and start sampling the RFC port voltage;
6. Read the TC0 count value and calculate the charging time of the RFC port;



RFC structure diagram

4. OPTION configuration table

CODE OPTION	Option	Function Description
Watchdog	Enable	Watchdog WDT Enable
	Disable	Watchdog WDT Disable
Clocks Division	2 Clocks	Instruction Clock Division Selection 2 Clocks
	4 Clocks	Instruction Clock Division Selection 4 Clocks
	8 Clocks	Instruction Clock Division Selection 8 Clocks
	16 Clocks	Instruction Clock Division Selection 16 Clocks
	32 Clocks	Instruction Clock Division Selection 32 Clocks
Oscillation mode	IRC mode	Main clock selects internal IHRC oscillator
	HXT mode	Main clock selects external high-speed crystal
	LXT mode	Main clock selects external low-speed crystal
IRC Frequency	1M	IRC Frequency Selection 1M
	6M	IRC Frequency Selection 6M
	16M	IRC Frequency Selection 16M
	32M	IRC Frequency Selection 32M (2clock selection prohibited)
Low voltage reset option	Enable: LVR	Default LVR function always enabled
	Enable:	LVR enable bit can be modified by software
Low voltage reset	LVR=1.8V	Low Voltage Reset Point Selection 1.8V
	LVR=2.0V	Low Voltage Reset Point Selection 2.0V
	LVR=2.2V	Low Voltage Reset Point Selection 2.2V
	LVR=2.3V	Low Voltage Reset Point Selection 2.3V
	LVR=2.5V	Low Voltage Reset Point Selection 2.5V
	LVR=2.7V	Low Voltage Reset Point Selection 2.7V
	LVR=3.1V	Low Voltage Reset Point Selection 3.1V
P55 Port	RST	P55 port used as external reset port
	GPIO	P55 port used as general-purpose input/output port
Reset time	PWRT=WDT=4.5ms	Reset setup time = WDT overflow time = 4.5ms
	PWRT=WDT=16ms	Reset setup time = WDT overflow time = 16ms
	PWRT=WDT=64ms	Reset setup time = WDT overflow time = 64ms
	PWRT=WDT=256ms	Reset setup time = WDT overflow time = 256ms
	PWRT=350us, WDT=4.5ms	Reset setup time = 350us, WDT overflow time = 4.5ms
	PWRT=350us, WDT=16ms	Reset setup time = 350us, WDT overflow time = 16ms
	PWRT=350us, WDT=64ms	Reset setup time = 350us, WDT overflow time = 64ms
	PWRT=350us, WDT=256ms	Reset setup time = 350us, WDT overflow time = 256ms
RTC	Enable	RTC Function Enabled

	Disable	RTC Function Disabled
Internal Capacitor Selection for Crystal Oscillator Pin	Internal Capacitor for Crystal Oscillator Pin Disabled	Internal Capacitor for Crystal Oscillator Pin Not Selected
	Internal Capacitor for Crystal Oscillator Pin 14pF	Internal Capacitor Selection for Crystal Oscillator Pin 14pF
	Internal Capacitor for Crystal Oscillator Pin 18pF	Internal Capacitor Selection for Crystal Oscillator Pin 18pF
	Internal Capacitor for Crystal Oscillator Pin 25pF	Crystal oscillator pin built-in capacitor selection 25pf
P5 drive enhancement	Enable	P5 port drive enhancement function enabled
	Disable	P5 port drive enhancement function disabled
P6 drive enhancement	Enable	P6 port drive enhancement function enabled
	Disable	P6 port drive enhancement function disabled
P7 drive enhancement	Enable	P7 port drive enhancement function enabled
	Disable	P7 port drive enhancement function disabled
CMP_FILT	Enable	Comparator result digital filter enabled
	Disable	Comparator result digital filter disabled
IRC oscillator voltage source selection	IRC oscillator selects LDO voltage	IRC oscillator voltage source selects LDO voltage
	IRC oscillator selects VDD voltage	IRC oscillator voltage source selects VDD voltage
Package pins	16pin	Chip package pin selection 16 pins
	20pin	Chip package pin selection 20 pins
	24pin	Chip package pin selection 24 pins
Programming mode selection	FLASH	Programming mode selection FLASH
	EEPROM	Programming mode selection EEPROM
	FLASH+EEPROM	Programming mode selection FLASH+EEPROM

Programming Port Settings	P53/P54 not used as programming ports	P53/P54 not used as programming ports, in-circuit powered programming not supported
	P53/P54 used as programming ports only during reset Used as programming ports	P53/P54 used as programming ports only during reset Used as programming ports (available for program use)
	P53/P54 used only as programming ports	P53/P54 used only as programming ports (hardware pull-up, program uncontrollable) The chip can enter programming mode at any time
Programming Function Selection	Regular Programming	Regular Programming (Programmer Powered Programming)
	On-board	On-board Powered Programming
OS Test	Enable	OS Test Enable (All Pin Detection)
	Disable	OS Test Disable (Programming Pin Detection)
Power-up Time Selection	Fast Power-up	Capacitance Between Power and Ground ≤ 100uF
	Slow Power-Up	100uF ≤ Capacitance between power and ground ≤ 470uF

Precautions for programming option [Power-up Time Selection]:

1) If [Power-up Time Selection] is set to [Fast Power-up], then [Reset Time] can be selected arbitrarily;
2) If [Power-up Time Selection] is set to [Slow Power-up], then [Reset Time] must be one of [PWRT=16ms/64ms/256ms];
3) If during the first programming, [Power-up Time Selection] is set to [Fast Power-up] + [PWRT=350us], and for the second programming, you want to select [Slow Power-up], then you must first program once with "[Fast Power-up] + [PWRT=16ms]" (the purpose is to program the chip with a long reset time), and then select [Slow Power-up] for programming;

5. Instruction Set

Instruction	Instruction Action	Flag Impact
ADD A,R	A+R→A	Z,C,DC
ADD R,A	A+R→R	Z,C,DC
AND A,R	A&R→A	Z
AND R,A	A&R→R	Z
CLRA	0→A	Z
CLR R	0→R	Z
INVA R	/R→A	Z
INV R	/R→R	Z
DA	A register adjusted to BCD value	C
DECA R	R-1→A	Z
DEC R	R-1→R	Z
DJA R	R-1→A, skip if zero	-
DJ R	R-1→R, skip if zero	-
INCA R	R+1→A	Z
INC R	R+1→R	Z
IJA R	R+1→A, skip if zero	-
IJ R	R+1→R, skip if zero	-
MOV R,A	A→R	-
MOV A,R	R→A	Z
MOV R,R	R→R	Z
OR A,R	A∨VR→A	Z
OR R,A	A∨VR→R	Z
SUB A,R	R-A→A	Z,C,DC
SUB R,A	R-A→R	Z,C,DC
XOR A,R	A⊕R→A	Z
XOR R,A	A⊕R→R	Z
BTC R,b	0→R(b)	-
BTS R,b	1→R(b)	-
JBTC R,b	if R(b)=0, skip	-
JBTS R,b	if R(b)=1, skip	-
LCR R	R(n)→R(n+1),R(7)→C, C→R(0)	C

LCA R	R(n)→A(n+1), R(7)→C, C→A(0)	C
RCR R	R(n)→R(n-1), R(0)→C, C→R(7)	C
RCA R	R(n)→A(n-1), R(0)→C, C→A(7)	C
SWAP R	R(0-3) ↔ R(4-7)	-
SWAPA R	R(0-3)→A(4-7), R(4-7)→A(0-3)	-
ADD A,k	A+k→A	Z,C,DC
AND A,k	A&k→A	Z
MOV A,k	k→A	-
OR A,k	A∨k→A	Z
SUB A,k	k-A→A	Z,C,DC
XOR A,k	A⊕k→A	Z
CALL k	PC+1→[SP], (Page,k)→PC	-
DI	Disable Interrupt	-
EI	Enable Interrupt	-
JMP k	K (Page,k)→PC	-
NOP	No Operation	-
RET	[Top of stack] → PC	-
RETI	[Top of stack] → PC, enable interrupt	-
RETL k	k → A, [Top of stack] → PC	-
SLEEP	0 → WDT, oscillator stops oscillating (sleep mode)	T, P
CWDT	0 → WDT	T, P
TBRD R	Machine code bits 7 to 0 given to ACC Machine code bits 15 to 8 given to R (general-purpose register)	-

Note: The execution of instructions changes the value of the program counter ("MOV R182,A", "ADD R182,A", "JMP *", "CALL *") or performs arithmetic or logical operations on R182 (e.g., "SUB R182,A", "BTS(C) R182,3", "CLR R182"); otherwise, all instructions occupy only a single instruction cycle (one instruction cycle consists of 2 oscillation cycles).

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Operating Temperature ..... -40℃ to 85℃
Storage Temperature ..... -40℃ to 150℃
Input Voltage ..... Vss-0.3V to Vdd+0.5V
Output Voltage ..... Vss-0.3V to Vdd+0.5V
Operating Voltage..... 1.8V-5.5V

6.2 Electrical Characteristics

(VDD = 5V, Operating Temperature = 25℃, unless otherwise specified)
Operating Characteristics

Parameter		Minimum	Typical	Maximum	Unit	Condition
System Clock (SYSCK)		-	32	-	MHz	[Oscillation Mode] Select IRC mode, frequency value is selected through [IRC Frequency]
		-	16	-	MHz	
		-	6	-	MHz	
		-	1	-	MHz	
		-	LXT	-	Hz	Oscillation mode selects LXT mode
Instruction Clock (Fcpu)	2T/4T	-	8	-	MHz	VDD=2.0V～5.5V
	4T/8T	-	4	-	MHz	VDD=1.8V～5.5V
	8T/16T	-	2	-	MHz	VDD=1.8V～5.5V
Power-on Reset Hold Time			350		μs	PWRT Independent Time
		Reset Time = WDT Overflow			ms	PWRT = WDT
External Reset Pulse		2			μs	25℃

Low Voltage Reset (LVR)

Parameter	Minimum	Typical	Maximum	Unit	Condition
ILVR		0.7		uA	25℃, VDD=5V
LVR threshold	1.72	1.8	1.85	V	25℃
	1.91	2.0	2.05		
	2.11	2.2	2.5		
	2.25	2.3	2.35		
	2.45	2.5	2.57		
	2.61	2.7	2.78		
	2.72	2.8	2.89		
	2.95	3.1	3.18		
LVR delay	50	-	120	us	25℃, VDD = 1.8V-5V

I/O port circuit

Parameter		Minimum	Typical	Maximum	Unit	Condition
VIL		0	-	0.25*VDD	V	25℃
VIH		0.54*VDD	-	VDD	V	25℃
Source Current	L0(P5/P6/P7)	6	8	10	mA	25℃, VDD=5V, VOH=4.4V
	L1(P5/P6/P7)	33	35	37		
	L2(P60/P61/P62/P63)	56	61	66		
Sink Current	L0(P5/P6/P7)	11	13	15	mA	25℃, VDD=5V, VOH=0.6V
	L1(P5/P6/P7)	36	38	40		
	L2(P60/P61/P62/P63)	55	60	65		
Pull-up Resistor		80	90	100	KΩ	25℃, VDD=5V
Pull-down Resistor		80	90	100	KΩ	25℃, VDD=5V

Operating Current (IDD)

Parameter	SYSCK	Typical Value @ VDD			Unit
		2.0V	3.0V	5.0V	
Normal Mode (2T)	32 MHz	0.88	1.9	3.2	mA
	16 MHz	0.64	1.0	1.4	
	6 MHz	0.35	0.5	0.67	
	1 MHz	0.18	0.23	0.25	
	40 KHz	0.004	0.005	0.009	
Sleep Mode (WDT off, LVR on)	-	0.2	0.3	0.8	uA
Sleep mode (WDT on, LVR on)	-	1.4	2	4	
Sleep mode (WDT off, LVR on, ADC on)	-	400	500	900	
Sleep mode (WDT off, LVR on, CMP on)	-	50	55	65	

MTP and EEPROM

Parameter		Minimum value	Typical value	Maximum value	Unit	Condition
VDD-READ	MTP/EEPROM	1.2	-	5.5	V	25℃, FCPU ≤
VDD-WRIT	MTP	2.5	-	5.5	V	25℃
	EEPROM	2.5	-	5.5	V	25℃
Endurance	MTP/EEPROM		10000		times	25℃
Retention	MTP/EEPROM		10		Year	25℃
TWRIT Write Time	MTP/EEPROM		2.5		ms	25℃
TERASE Erase Time	MTP/EEPROM		1.5		ms	25℃
IP/E Write/Erase	MTP/EEPROM		2.5		mA	25℃, VDD=5.5V

6.3 AD Conversion Characteristics

(VDD=5V, VSS=0V, Operating Temperature=25℃)

Symbol		Parameter Description	Condition	Minimum	Typical	Maximum	Unit
VAREF		Analog Reference Voltage	VAREF - VASS ≥ 2V	1.29	-	VDD	V
VASS				VSS	-	VSS	V
VAI		Analog Input	-	VASS	-	VAREF	V
IAI1	IVDD	Analog Supply Current	VAREF=VDD=5V VASS=0V FS*1=100KHz FIN*1=1KHz (VREF from internal Vdd)	-	-	1400	μA
	IVREF			-	-	10	μA
IAI2	IVDD	Analog Supply Current	VAREF=VDD=5V VASS=0V FS*1=100KHz FIN*1=1KHz (VREF from external VREF pin)	-	-	900	μA
	IVREF			-	-	500	μA
RN		Resolution	-	-	12	-	Bit
TAD		ADC cycle clock	VDD= VAREF =5V, VASS=0V	1	-	-	μs
TSH		Sampling and hold time	VDD=3～5.5V VASS=0V, Ta=25℃	4	-	-	μs
			VDD=2.5～3V VASS=0V, Ta=25℃	16	-	-	μs
TCN		AD conversion time	VDD=2.5～5.5V, VASS=0V	14	-	24	TAD
TADD1		Delay between the first TAD starting at the high	VDD=2.5～5.5V VASS=0V	1	-	-	TAD
PSRR		Power Supply Rejection Ratio	VAREF=2.5V VASS=0V VIN*1=0V～2.5V FS*1=25KHz	-	-	2	LSB

6.4 VREF Characteristics

(VDD = 5V, VSS = 0V, Ta = -40 to 85℃)

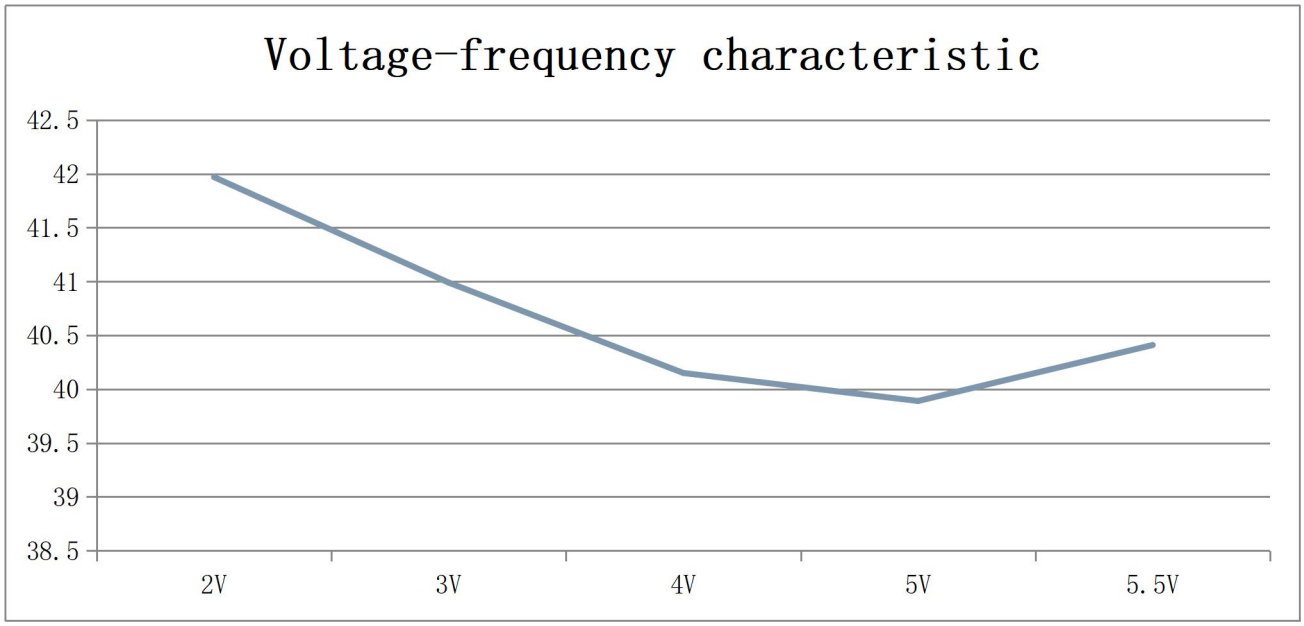
Symbol	Parameter Description	Condition	Minimum	Typical	Maximum	Unit
VDD	Supply Voltage	-	1.29	-	5.5	V
IVDD	DC Supply Current	No load	-	-	250	μA
VREF	Reference Voltage Output	VBG, 2V, 3V, 4V	-	±1	1.75	%
Warm up Time	Reference Voltage Preparation Time	VDD=VDDmin-5.5V, Cload=19.2pf Rload-15.36KΩ	-	38	50	μs
VDDmin	Minimum supply	-	-	VREF+0.2	-	V

6.5 Characteristic Curves

The curves listed in this chapter are for design reference only. Some of the data provided may exceed the specified operating range of the chip. To ensure the normal operation of the chip, please strictly follow the electrical characteristics specifications.

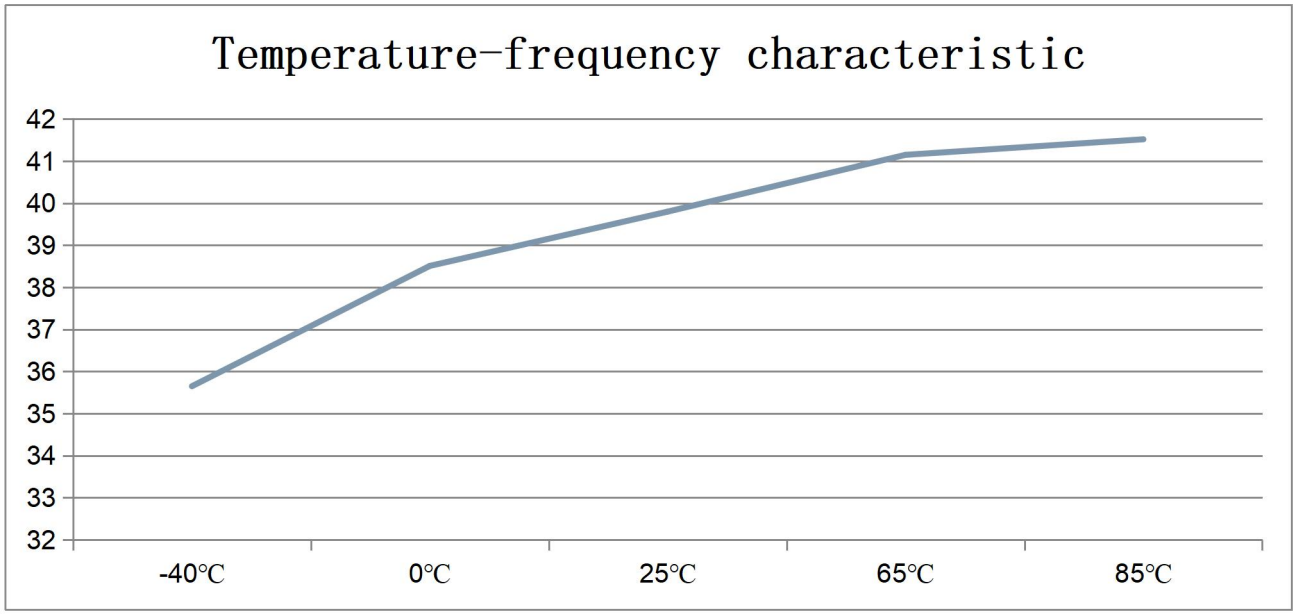
6.5.1 Internal Low-Speed Oscillator - Voltage-Frequency Characteristic Curve

Operating temperature at 25℃: (unit KHz)



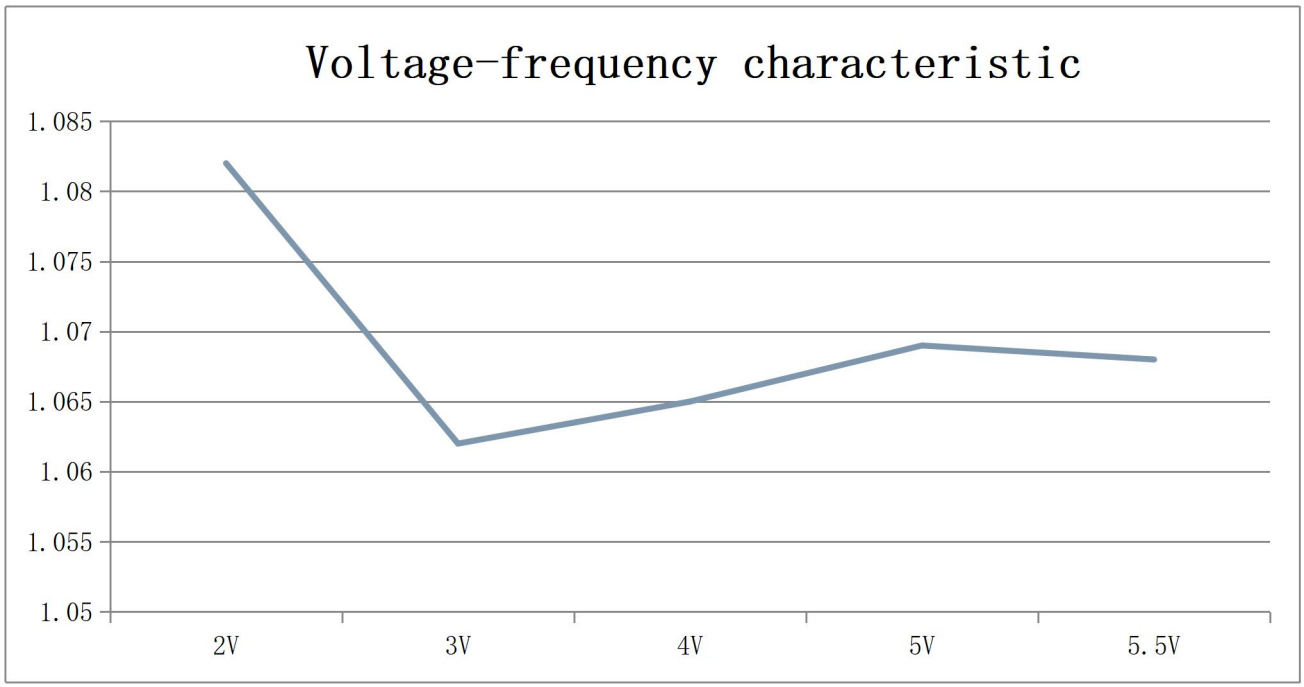
6.5.2 Internal Low-Speed Oscillator - Temperature-Frequency Characteristic Curve

Operating voltage at 5V condition: (unit Khz)



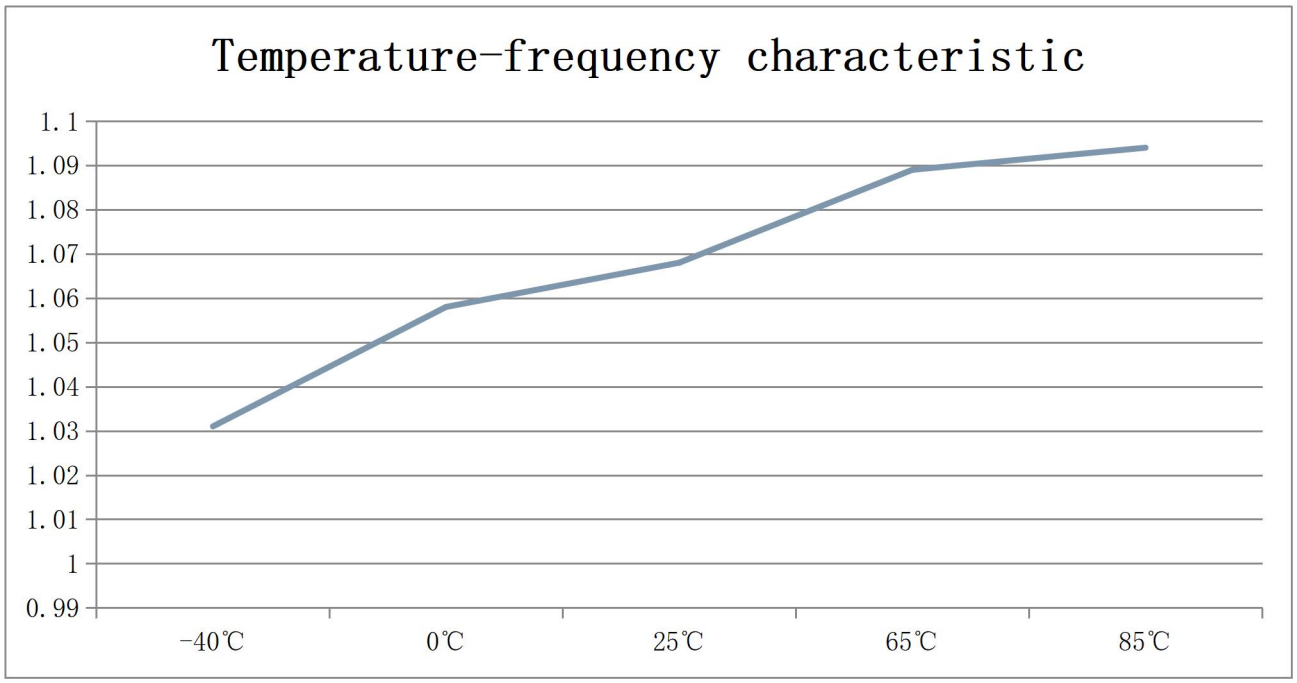
6.5.3 Internal 1MHz RC Oscillator - Voltage-Frequency Characteristic Curve

Operating temperature at 25℃ condition: (unit MHz)



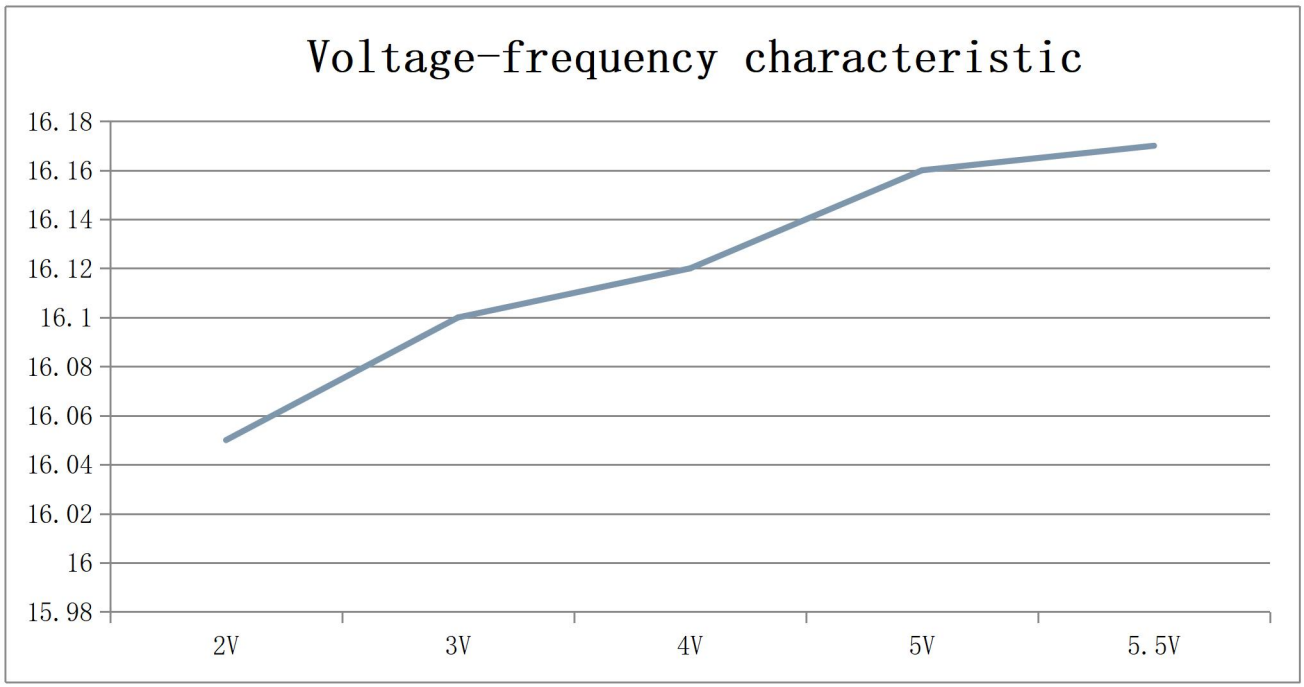
6.5.4 Internal 1MHz RC Oscillator - Temperature-Frequency Characteristic Curve

Operating voltage at 5V condition: (unit MHz)



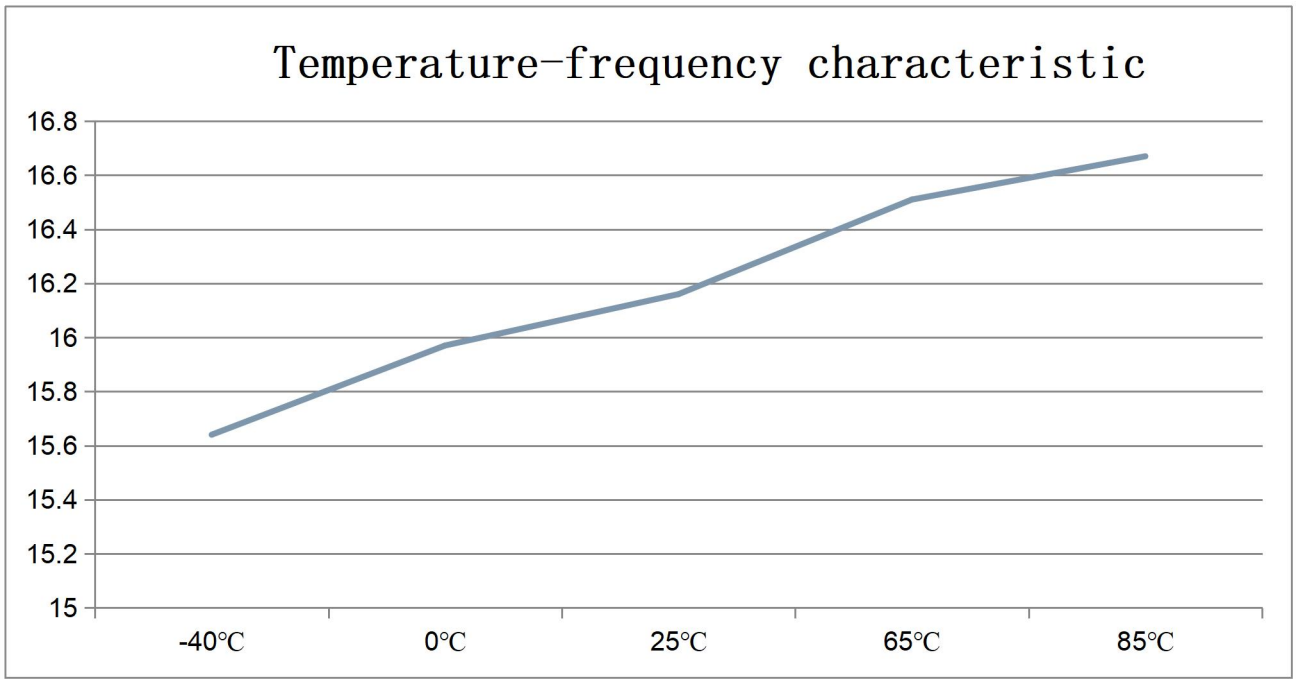
6.5.5 Internal 16MHz RC Oscillator - Voltage-Frequency Characteristic Curve

Operating temperature at 25℃ condition: (unit MHz)



6.5.6 Internal 16MHz RC Oscillator - Temperature-Frequency Characteristic Curve

Operating voltage at 5V condition: (unit MHz)



6.6 IHRC Frequency Fine-Tuning Parameter Description

The parameter description is for trend reference only; actual values may vary.

IHRCCAL Adjustment Value (Hexadecimal)	Frequency (MHz)	Tuning Deviation (IHRCCAL=0x7F)
00	7.8685	-51.27%
01	7.8989	-51.08%
02	7.9306	-50.88%
03	7.9615	-50.69%
04	7.9946	-50.48%
05	8.0244	-50.30%
06	8.0567	-50.10%
07	8.0900	-49.89%
08	8.1230	-49.69%
09	8.1554	-49.49%
0A	8.1911	-49.27%
0B	8.2221	-49.08%
0C	8.2612	-48.83%
0D	8.2928	-48.64%
0E	8.3260	-48.43%
0F	8.3594	-48.23%
10	8.3979	-47.99%
11	8.4313	-47.78%
12	8.4694	-47.54%
13	8.5057	-47.32%
14	8.5400	-47.11%
15	8.5790	-46.87%
16	8.6136	-46.65%
17	8.6503	-46.42%
18	8.6891	-46.18%
19	8.7255	-45.96%
1A	8.7629	-45.73%
1B	8.8015	-45.49%
1C	8.8443	-45.22%
1D	8.8817	-44.99%
1E	8.9246	-44.73%
1F	8.9603	-44.50%
20	9.0002	-44.26%
21	9.0346	-44.04%
22	9.0782	-43.77%
23	9.1206	-43.51%
24	9.1629	-43.25%
25	9.2062	-42.98%

26	9.2536	-42.69%
27	9.2929	-42.44%
28	9.3373	-42.17%
29	9.3862	-41.87%
2A	9.4265	-41.62%
2B	9.4737	-41.32%
2C	9.5194	-41.04%
2D	9.5634	-40.77%
2E	9.6137	-40.46%
2F	9.6657	-40.13%
30	9.7111	-39.85%
31	9.7610	-39.54%
32	9.8052	-39.27%
33	9.8555	-38.96%
34	9.9056	-38.65%
35	9.9545	-38.35%
36	10.0069	-38.02%
37	10.0607	-37.69%
38	10.1097	-37.38%
39	10.1618	-37.06%
3A	10.2126	-36.75%
3B	10.2720	-36.38%
3C	10.3227	-36.07%
3D	10.3786	-35.72%
3E	10.4337	-35.38%
3F	10.4836	-35.07%
40	10.5419	-34.71%
41	10.6021	-34.34%
42	10.6584	-33.99%
43	10.7153	-33.63%
44	10.7758	-33.26%
45	10.8314	-32.91%
46	10.8925	-32.54%
47	10.9519	-32.17%
48	11.0149	-31.78%
49	11.0798	-31.38%
4A	11.1415	-30.99%
4B	11.2065	-30.59%
4C	11.2811	-30.13%
4D	11.3397	-29.77%
4E	11.4024	-29.38%
4F	11.4741	-28.93%
50	11.5460	-28.49%
51	11.6136	-28.07%

52	11.6864	-27.62%
53	11.7510	-27.22%
54	11.8237	-26.77%
55	11.8957	-26.32%
56	11.9714	-25.85%
57	12.0446	-25.40%
58	12.1222	-24.92%
59	12.1995	-24.44%
5A	12.2718	-23.99%
5B	12.3573	-23.46%
5C	12.4258	-23.04%
5D	12.5138	-22.50%
5E	12.5884	-22.03%
5F	12.6776	-21.48%
60	12.7655	-20.94%
61	12.8476	-20.43%
62	12.9325	-19.90%
63	13.0183	-19.37%
64	13.1138	-18.78%
65	13.2061	-18.21%
66	13.2976	-17.64%
67	13.3926	-17.05%
68	13.4878	-16.46%
69	13.5799	-15.89%
6A	13.6794	-15.28%
6B	13.7778	-14.67%
6C	13.8836	-14.01%
6D	13.9823	-13.40%
6E	14.0871	-12.75%
6F	14.1931	-12.09%
70	14.3019	-11.42%
71	14.4097	-10.75%
72	14.5217	-10.06%
73	14.6339	-9.36%
74	14.7487	-8.65%
75	14.8661	-7.93%
76	14.9850	-7.19%
77	15.1078	-6.43%
78	15.2292	-5.68%
79	15.3525	-4.91%
7A	15.4803	-4.12%
7B	15.6073	-3.34%
7C	15.7431	-2.49%
7D	15.8757	-1.67%

7E	16.0069	-0.86%
7F	16.1458	0.00%
80	14.7633	-8.56%
81	14.8206	-8.21%
82	14.8799	-7.84%
83	14.9406	-7.46%
84	14.9875	-7.17%
85	15.0587	-6.73%
86	15.1219	-6.34%
87	15.1816	-5.97%
88	15.2429	-5.59%
89	15.3056	-5.20%
8A	15.3653	-4.83%
8B	15.4271	-4.45%
8C	15.4962	-4.02%
8D	15.5627	-3.61%
8E	15.6262	-3.22%
8F	15.6900	-2.82%
90	15.7579	-2.40%
91	15.8226	-2.00%
92	15.8758	-1.67%
93	15.9582	-1.16%
94	16.0252	-0.75%
95	16.0920	-0.33%
96	16.1644	0.11%
97	16.2341	0.55%
98	16.3050	0.99%
99	16.3822	1.46%
9A	16.4535	1.91%
9B	16.5289	2.37%
9C	16.6084	2.87%
9D	16.6874	3.35%
9E	16.7538	3.77%
9F	16.8327	4.25%
A0	16.9115	4.74%
A1	16.9946	5.26%
A2	17.1022	5.92%
A3	17.1442	6.18%
A4	17.2501	6.84%
A5	17.3241	7.30%
A6	17.4032	7.79%
A7	17.4754	8.23%
A8	17.5911	8.95%
A9	17.6619	9.39%

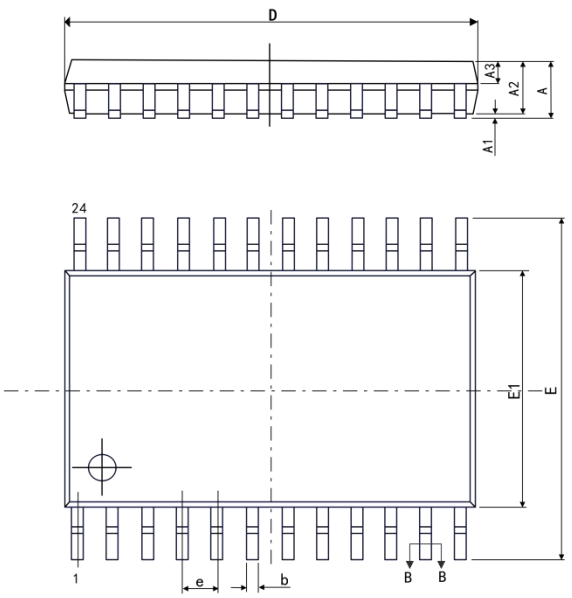
AA	17.7601	10.00%
AB	17.8608	10.62%
AC	17.9364	11.09%
AD	18.0114	11.55%
AE	18.1189	12.22%
AF	18.2237	12.87%
B0	18.3181	13.45%
B1	18.4032	13.98%
B2	18.4694	14.39%
B3	18.5649	14.98%
B4	18.6502	15.51%
B5	18.7591	16.19%
B6	18.8554	16.78%
B7	18.9598	17.43%
B8	19.0521	18.00%
B9	19.1623	18.68%
BA	19.2432	19.18%
BB	19.3453	19.82%
BC	19.4602	20.53%
BD	19.5515	21.09%
BE	19.6595	21.76%
BF	19.7762	22.49%
C0	19.8803	23.13%
C1	19.9999	23.87%
C2	20.1009	24.50%
C3	20.2071	25.15%
C4	20.3154	25.82%
C5	20.4301	26.54%
C6	20.5520	27.29%
C7	20.6728	28.04%
C8	20.8597	29.20%
C9	20.9218	29.58%
CA	21.0434	30.33%
CB	21.1664	31.10%
CC	21.2888	31.85%
CD	21.4206	32.67%
CE	21.5467	33.45%
CF	21.6666	34.19%
D0	21.7945	34.99%
D1	21.9343	35.85%
D2	22.0665	36.67%
D3	22.2033	37.52%
D4	22.3494	38.42%
D5	22.4765	39.21%

D6	22.6220	40.11%
D7	22.7328	40.80%
D8	22.9036	41.85%
D9	23.0364	42.68%
DA	23.1816	43.58%
DB	23.3294	44.49%
DC	23.4603	45.30%
DD	23.6235	46.31%
DE	23.7779	47.27%
DF	23.9420	48.29%
E0	24.1088	49.32%
E1	24.2740	50.34%
E2	24.4546	51.46%
E3	24.6332	52.57%
E4	24.7976	53.59%
E5	24.9741	54.68%
E6	25.1388	55.70%
E7	25.3200	56.82%
E8	25.4950	57.90%
E9	25.6810	59.06%
EA	25.8604	60.17%
EB	26.0300	61.22%
EC	26.2191	62.39%
ED	26.4211	63.64%
EE	26.6126	64.83%
EF	26.8000	65.99%
F0	27.0091	67.28%
F1	27.1812	68.35%
F2	27.3823	69.59%
F3	27.6009	70.95%
F4	27.7993	72.18%
F5	27.9843	73.32%
F6	28.2271	74.83%
F7	28.4457	76.18%
F8	28.6658	77.54%
F9	28.9211	79.12%
FA	29.1583	80.59%
FB	29.3971	82.07%
FC	29.5810	83.21%
FD	29.8559	84.91%
FE	30.1299	86.61%
FF	30.3641	88.06%

7. Package Dimensions

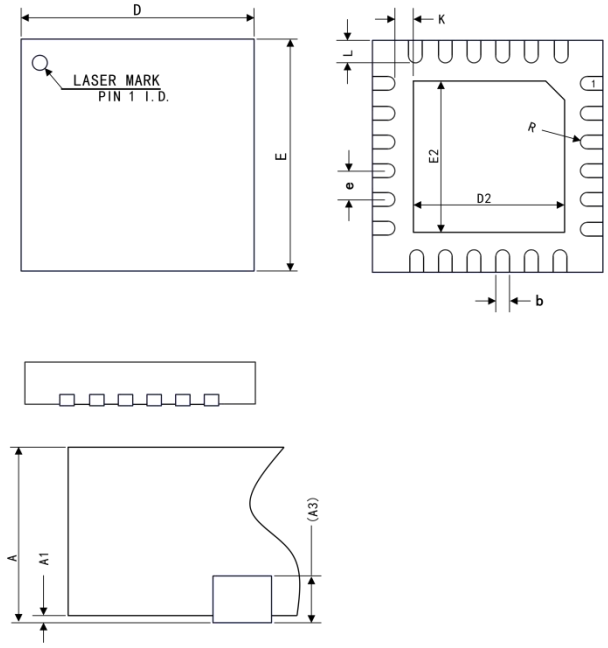
7.1 24PIN Package Dimensions

(Unit: mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.03	0.08	0.12
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

TSSOP24 Package Dimensions

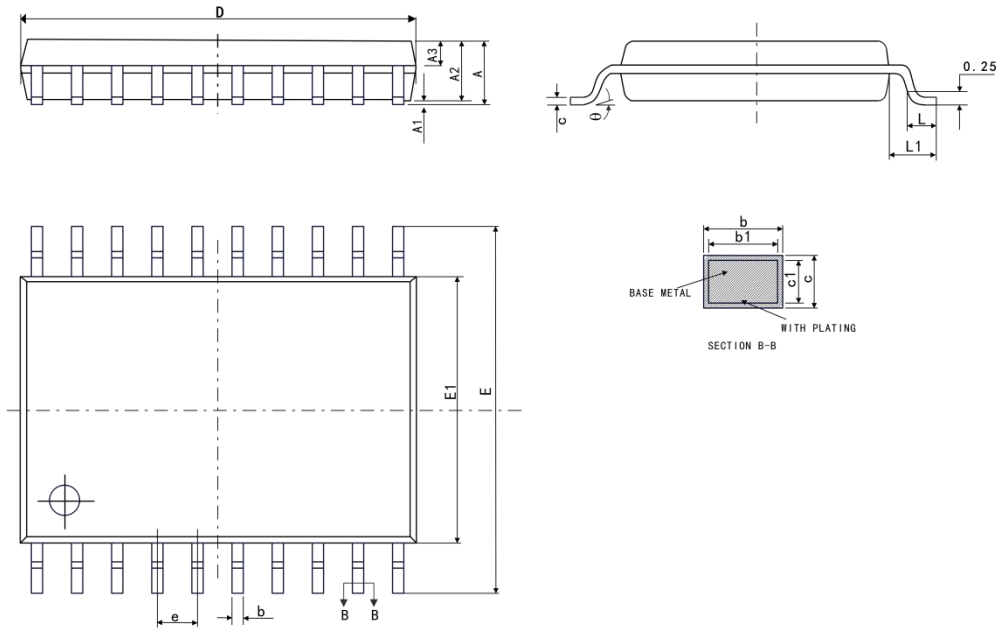


SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.40	0.50	0.60
K	0.20	—	—
L	0.35	0.40	0.45
R	0.09	—	—

QFN24 Package Dimensions

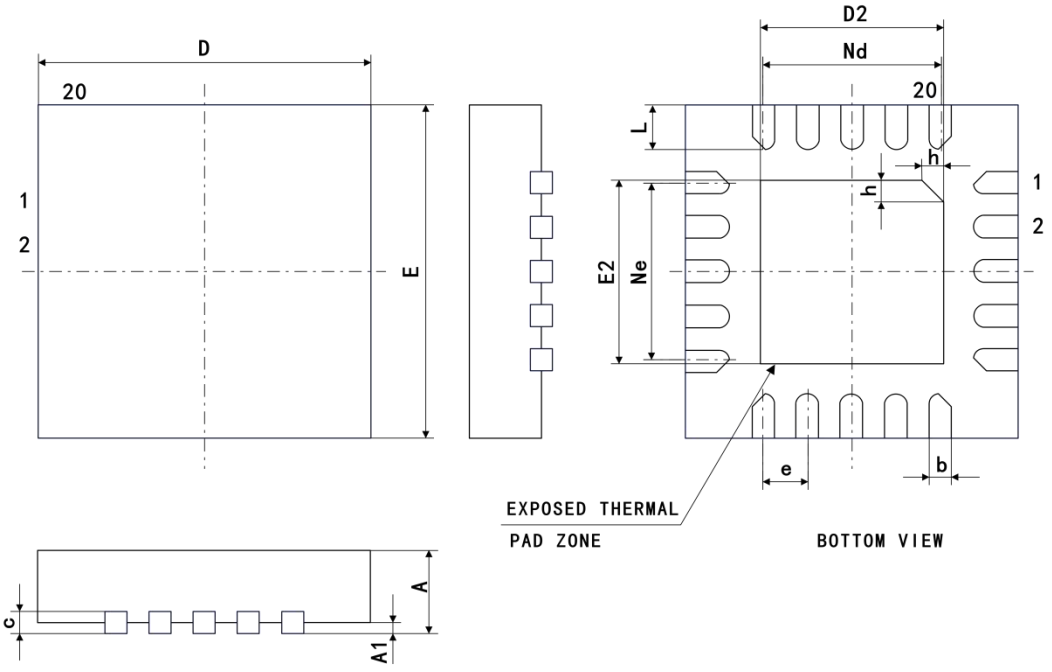
7.2 20PIN Package Dimensions

(Unit: mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	0.08	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

TSSOP20 Package Dimensions



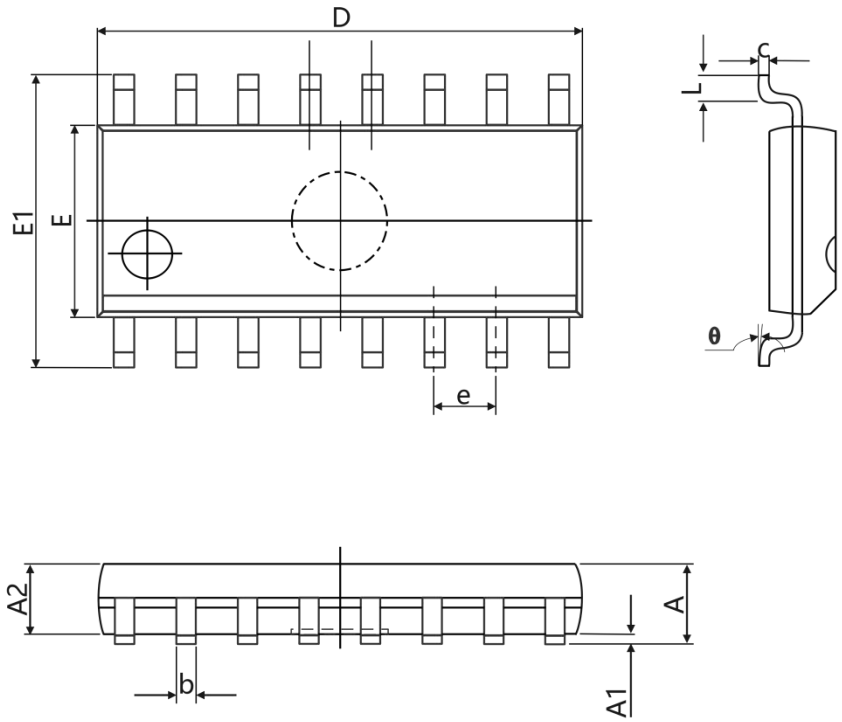
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
	75*75		

QFN20 Package Dimensions

7.3 16PIN Package Dimensions

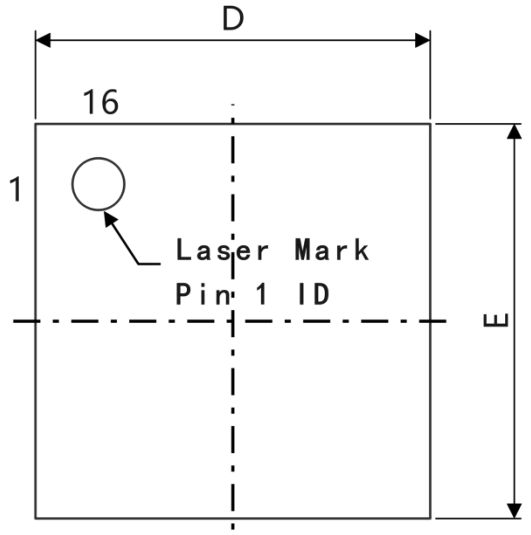
(Unit: mm)

SOP16

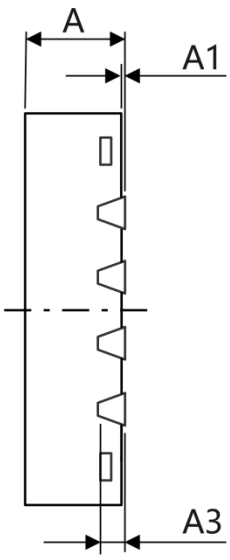


SYMBOL	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0 °	8 °	0 °	8 °

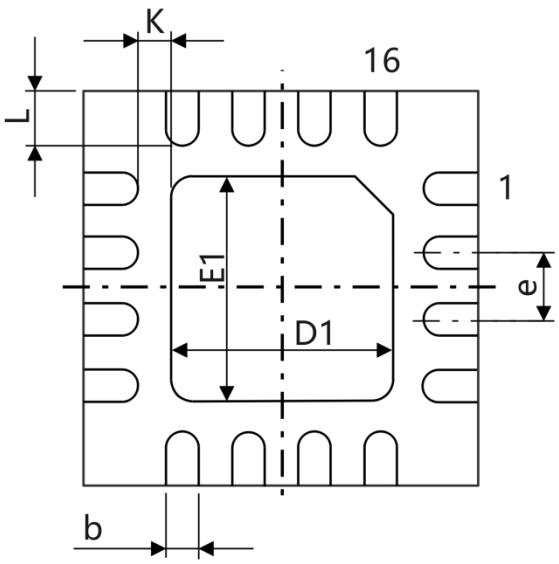
SOP16 package Dimensions



Top View



Side View

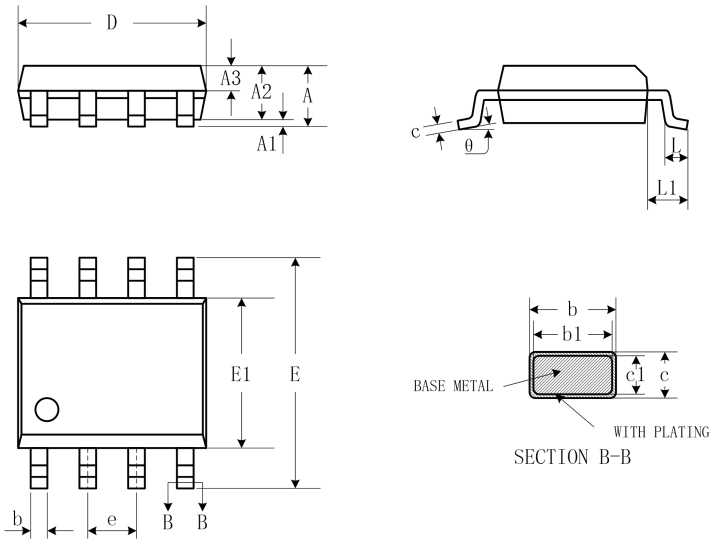


Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e	0.50TYP		
K	0.20	—	—
L	0.30	0.40	0.50

QFN16 package Dimensions

7.4 8PIN Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	-	8°

SOP8 package Dimensions