JZ8ME2602C

8-Bit Microcontroller with MTP ROM

DATASHEET

VERSION 1.0

Revision History

Version	Revision Description	Note
V1.0	Finish the first draft	

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1 General Description

1.1 Features

CPU Configuration

- 2K×16-Bit MTP ROM
- 256×8-Bit EEPROM
- 80×8-Bit SRAM
- 8-level stacks
- 4 programmable Level Voltage Detector
  4.5V, 4.0V, 3.3V, 2.2V
- 4 programmable Level Voltage Reset
  4.0V, 3.5V, 2.7V, 1.8V
- Less than 2 mA (4MHz/5V)
- Less than 30 μA (32kHz/3V)
- Less than 1 μA (Sleep Mode)

I/O Port Configuration

- 3 bidirectional I/O:P5, P6, P7
- 16 I/O pins(P71 open-drain output)
- Wake-up port:P5 口
- 14 programmable pull-high I/O pins
- 8 programmable pull-down I/O pins
- 6 programmable open-drain I/O pins
- 14 programmable high-sink current I/O pins

Operating Voltage

- Operating voltage range:
  1.8V～5.5V (0℃-70℃)
  2.3V～5.5V (-40℃-85℃)

Operating Frequency range

- Internal RC Oscillator Mode:
  16MHz, 8MHz, 4MHz, 1MHz
- External RC Oscillator Mode:
- External XT Oscillator Circuit:
  DC～16MHz (more than 4.5V)
  DC～8MHz (more than 3V)
  DC～4MHz (more than 2.5V)
- Clock Cycle Frequency Division:
  2Clock, 4Clock, 8Clock, 16Clock

Peripheral Configuration

- 8-bit real time clock/counter
- 7 channel ADC with 12 bit resolution
- One pair of comparator or OP
- Two PWM with 8-bit resolution
- Cascade 16Bit PWM

Available Interrupts

- TCC overflow interrupt
- Input port status changed interrupt
- ADC completion interrupt
- Comparator status changed interrupt
- Low voltage detect (LVD) interrupt
- PWM1 period/ duty match interrupt
- PWM2 period/ duty match interrupt

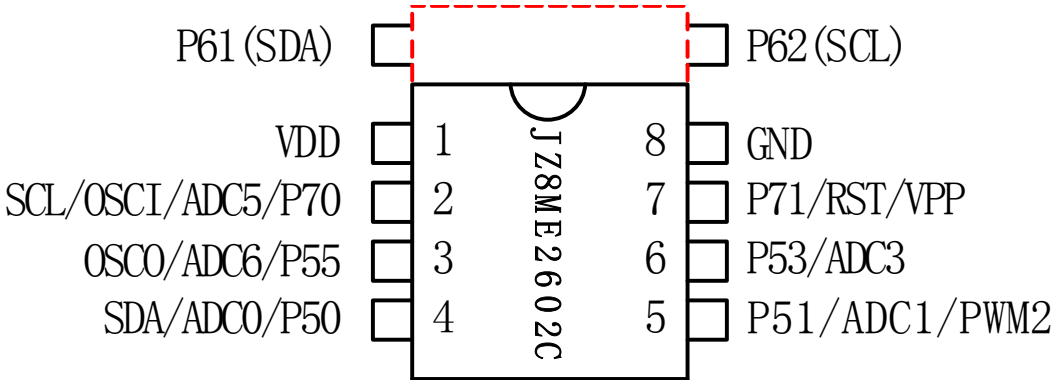
Features

- Programmable Watchdog Timer
- 4 working modes switch
- It can record 1000 times
  repeatedly

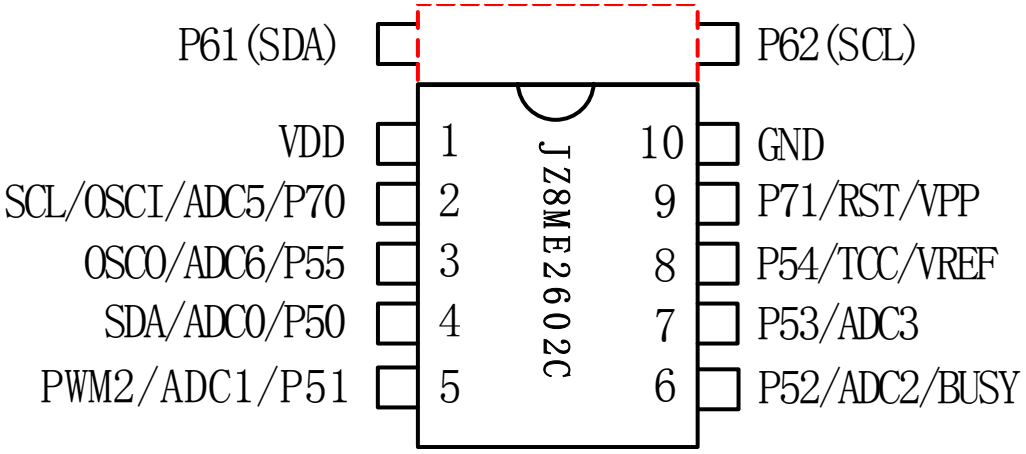
Package Type

- JZ8ME2602C-DIP16;
- JZ8ME2602C-SOP16;
- JZ8ME2602C-DIP8;
- JZ8ME2602C-SOP8;
- JZ8ME2602C-MSOP10;

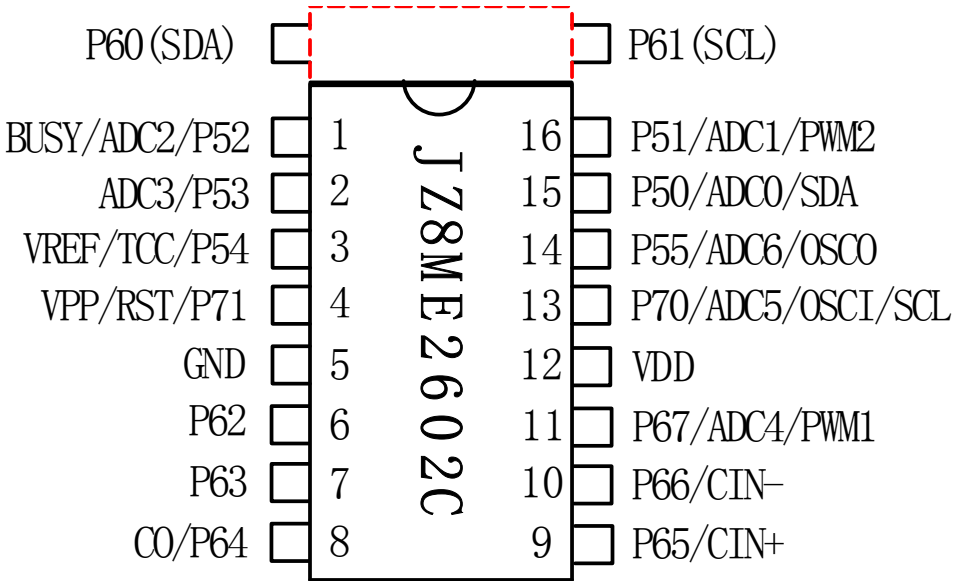
1.2 Pin Assignment



JZ8ME2602C-8PIN



JZ8ME2602C-10PIN



JZ8ME2602C-16PIN

NOTE: P60, P61 and P62 are 24C02 communication ports, which are marked according to the foot map of the specific model

1.3 Pin Description

Name	Function	I/O	Description
P50	P50	I/O (Pull up/down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up.
	ADC0	AN	ADC Input 0
	SDA	--	Burning port
P51	P51	I/O (Pull up/down)	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC1	AN	ADC Input 1
	PWM2	CMOS	PWM2 output
P52	P52	I/O (Pull up/down)	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC2	AN	ADC Input 2
	BUSY	--	Burning port
P53	P53	I/O (Pull up/down)	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	ADC3	AN	ADC Input 3
P54	P54	I/O (Pull up/down)	Bidirectional I/O pin with programmable pull-down, pull-high, high-driver, high-sink and pin change wake-up.
	TCC	SMT	Real Time Clock/Counter clock input
	VREF	AN	ADC external voltage reference
P55	P55	I/O (Pull up/down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up.
	ADC6	AN	ADC Input6
	OSCO	XTAL	Clock output of crystal oscillator
	ERCin	AN	External RC input pin
P60	P60	I/O (Pull up/down)	Bidirectional I/O pin with programmable open-drain, pull-high, high-driver and high sink.
	SDA		EEPROM communication port
P61	P61	I/O (Pull up/down)	Bidirectional I/O pin with programmable open-drain, pull-high, high-driver and high sink.
	SDA/SCL		EEPROM communication port
P62	P62	I/O (Pull up/down)	Bidirectional I/O pin with programmable open-drain, pull-high, high-driver and high sink.
	SCL		EEPROM communication port
P63	P63	I/O (Pull up/down)	Bidirectional I/O pin with programmable open-drain, pull-high, high-driver and high sink.
P64	P64	I/O (Pull up/down)	Bidirectional I/O pin with programmable open-drain, pull-high, high-driver and high sink.
	CO	O	Comparator output
P65	P65	I/O (Pull up/down)	Bidirectional I/O pin with programmable open-drain,

			pull-high, high-driver and high sink.
	CIN+	I	comparator input “+” end
P66	P66	I/O (Pull up/down)	Bidirectional I/O pin with programmable open-drain, pull-high, high-driver and high sink.
	CIN-	I	comparator input “-” end
P67	P67	I/O (Pull up)	Bidirectional I/O pin with programmable open-drain, pull-high, high-driver and high sink.
	ADC4	AN	ADC Input 4
	PWM1	CMOS	PWM1 output
P70	P70	I/O	GPIO
	ADC5	AN	ADC Input 5
	OSCI	I (XTAL)	Clock input of crystal oscillator
	RCOUT	O	Clock output of RC oscillator
	SCL		Burning port
P71	P71	I	open-drain output
	RESET	I (SMT)	System reset pin
	VPP		Burning port
	VDD	--	Power
	VSS	--	Ground

NOTE: Red marks the chip burning port, P60, P61 and P62 are 24C02 communication ports, which are marked according to the foot map of the specific model

2 Memory Structure

2.1 Data Memory

2.1.1 RPAGE and Bank Data Register

0x00	R0 Indirect Addressing Register	Reserved
0x01	R1 Timer Clock Counter	Reserved
0x02	R2 Program Counter	Reserved
0x03	R3 Status Register	Reserved
0x04	R4 FSR RAM Bank select	Reserved
0x05	R5 Port 5 I/O data	R5 TBHP: Table Point Register
0x06	R6 Port 6 I/O data	R6 TBLP: Table Point Register
0x07	R7 Port 7 I/O data	R7 PWM Control Register
0x08	R8 ADC Input Select Register	R8 Timer Control Register
0x09	R9 ADC Control Register	R9 PWM1 Time Period
0x0A	RA ADC Offset Calibration Register	RA PWM2 Time Period
0x0B	RB Converted value AD11~AD4 of ADC	RB PMW1 Duty Cycle
0x0C	RC Converted value AD11~AD8 of ADC	RC PMW2 Duty Cycle
0x0D	RD Converted value AD7~AD0 of ADC	Reserved
0x0E	RE Interrupt Status 2 and Wake-up Control Register 1	RE LVD Control and Wakeup Control Register 2
0x0F	RF Interrupt Status Register 1	RF Mode Select and IRC Switch Register
0x10 ～ 0x1F	Common Register 16*8Bit	
0x20 ～ 0x3F	Bank0	Bank1
	Common Register 32*8Bit	Common Register 32*8Bit

2.1.2 IOPAGE Data Register

Address	IOPAGE0	IOPAGE1
0x00	Reserved	Reserved
0x01	Reserved	Reserved
0x02	Reserved	Reserved
0x03	Reserved	Reserved
0x04	Reserved	Reserved
0x05	IOC50 Port 5 I/O control	IOC51 P5 High Sink Control Register
0x06	IOC60 Port 6 I/O control	IOC61 P6 High Sink Control Register
0x07	IOC70 Port 7 I/O control	IOC71 P5 High Driver Control Register
0x08	IOC80 Comparator Control Register	IOC81 P6 High Driver Control Register
0x09	IOC90 PWM1 Timer	Reserved
0x0A	IOCA0 PWM2 Timer	Reserved
0x0B	IOCB0 Pull-down Control Register	Reserved
0x0C	IOCC0 Open-drain Control Register	Reserved
0x0D	IOCD0 Pull-high Control Register	Reserved
0x0E	IOCE0 WDT Control Register and Interrupt Mask Register 2	Reserved
0x0F	IOCF0 Interrupt Enable Register 1	IOCF1 P6 Pull-high Control Register

3 Functional Description

3.1 Operational Registers

3.1.1 RPAGE0～R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4) low 6 bit RAMS<5:0>.

3.1.2 RPAGE0～R1 (Time Clock/Counter)

TCC is an 8Bit counter, clock source optional internal clock/external clock, count overflow can form interrupt, TMR can read and write.

TCC incremented by an external signal edge which is defined by the EXINT(cont.4) through the TCC pin, or by the instruction cycle clock. If the PAB bit (cont.3) is cleared, a predivider is assigned to the TCC, and when the TCC register is written to a value, the value of the predivider is cleared to 0.

3.1.3 RPAGE0～R2 (Program Counter)

The program counter (PC) is used to record each instruction cycle of CPU instruction pointer. During the CPU cycle, the PC pushes the instruction pointer into the program memory, and then the pointer adds 1 to enter the next cycle. JZ8ME2602C has a 11-bit wide program counter (PC) with low bytes from the read-write PCL.

The JZ8ME2602C stack is used to record the instruction pointer returned by the program. When a subroutine is called, the PC pushes the instruction pointer. When the return instruction is executed, the stack sends the instruction pointer back to the PC to continue the original process. JZ8ME2602C has an 8-level stack that occupies neither program nor data storage, and the stack pointer cannot be read or written.

(1) PC and STACK are 11-bit wide, for addressing 2K×16Bit ROM, program store map.

(2) The contents of R2 are all set to 0 when a reset condition occurs.

(3) “JMP” instruction allows direct loading of the lower 10 program counter bits. Thus, “JMP” allows the PC to jump to any location within a page.

(4) “RET” (“RETL k”, “RETI”) instruction loads the program counter with the contents of the top of the stack.

(5) The stack works like a circular buffer. After eight pushes, the data for the ninth push overwrites the data for the first push, the data for the 10th push overwrites the data for the second push, and so on.

3.1.4 RPAGE0～R3 (Status Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	IOCS	-	T	P	Z	DC	C

Bit<7>:RST: Bit of reset type

0: Other reset types

1: Wake-up from sleep on pin change, comparator status change, or AD conversion completed.

Bit<6>:IOCS: Select the Segment of IO control register

0: Select the IOCPAGE0 page

1: Select the IOCPAGE1 page

Bit<4>:T: Time-out bit

0: WDT time-out

1: Set to “1” by the “SLEP” and “WDTC” commands or during power on

Affect T/P event shown in the following table:

Type	RST	T	P
Power on reset	0	1	1
Press RESET under working mode	0	hold	hold
RESET wake up	0	1	0
WDT overflow in working mode	0	0	hold
WDT overflow wake	0	0	0
Port state changes wake up	1	1	0
Execute WDTC instruction	hold	1	1
Execute SLEEP instruction	hold	1	0

Bit<3>:P: Power-down bit

0: Execute SLEEP instruction

1: Power on reset or Execute WDTC instruction

Bit<2>:Z: Zero flag

0: When arithmetic or logic is not zero

1: When arithmetic or logic is 0

Bit<1>:DC: Auxiliary carry flag

0: When the addition operation is performed, the lower four bits are not carried. When performing a subtraction operation, the lower four bits borrow

1: When performing the addition operation, the lower four bits have carry; When subtracting, the lower four bits do not borrow

Bit<0>:C: Carry flag

0: When the addition operation is performed, the higher four bits are not carried. When performing a subtraction operation, the high four bits borrow

1: When the addition operation is performed, the higher four bits have carry. When performing a subtraction operation, the high four digits do not borrow

3.1.5 RPAGE0～R4 (FSR RAM Select Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBANK	BANK	FSR<5:0>					

FSR<7>:SBANK

Special Register 0x05~0x0F bank selection bit.

FSR<6>: Used to select Bank 0 or Bank 1 of the register (0x20-0x3F)

0: Bank0

1: Bank1

FSR<5:0>: Used to select a register (Address: 00~0F, 10~3F) in indirect addressing mode.

3.1.6 RPAGE0 R5～R7(Port 5 ~ Port 7)

Port input/output registers

3.1.7 RPAGE0～R8(ADC Input Select Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ADE<6>	ADE<5>	ADE<4>	ADE<3>	ADE<2>	ADE<1>	ADE<0>

Bit<7:0>:ADE<7:0>-AD converter enable bit

1: Enable

0: Disable

Channel number	Enable control	Corresponding pin
AD0	ADE<0>	P50
AD1	ADE<1>	P51
AD2	ADE<2>	P52
AD3	ADE<3>	P53
AD4	ADE<4>	P67
AD5	ADE<5>	P70
AD6	ADE<6>	P55

Registers are readable and writable

3.1.8 RPAGE0～R9(ADC Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR<1:0>		ADRUN	ADPD	ADIS<2:0>		

Bit<7>:VREFS- The input source of Vref of the ADC

1: The Vref of the ADC is connected to P54

0: The Vref of the ADC is connected to VREF (Vdd is default value)

Bit<6:5>:CKR<1:0>（**ADC Clock Rate Select**）

CPUS	CKR<1>	CKR<0>	ADC clock
1	0	0	Fosc/16
1	0	1	Fosc/4
1	1	0	Fosc/64
1	1	1	Fosc/1
0	x	x	Fosc/1

Bit<4>:ADRUN- ADC starts to RUN

1: Enable

0: Disable

Bit<3>:ADPD- ADC Power

1: Enable

0: Disable

Bit<2:0>:ADIS<2:0>- Analog Input Select

ADICS	ADIS<2>	ADIS<1>	ADIS<0>	ADC Input Select
0	0	0	0	P50
0	0	0	1	P51

0	0	1	0	P52
0	0	1	1	P53
0	1	0	0	P67
0	1	0	1	P70
0	1	1	0	P55
1	0	0	0	OPOUT
1	1	0	0	0.25*VDD

Note: Fosc represents the oscillator clock. For example, if the IRC frequency is selected as 4M, then Fosc=4M

For example:Fosc=4M, TAD set Fosc/4, then TAD=1US

3.1.9 RPAGE0～RA(ADC Offset Calibration Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF<2:0>			VREF<1:0>		ADICS

Bit<7>:CALI-Calibration enable bit for ADC offset

1: Enable

0: Disable

Bit<6>:SIGN-Polarity bit of the offset voltage

1: Positive voltage

0: Negative voltage

Bit<5:3>:VOF<2:0>-ADC Offset voltage bits

VOF<2>	VOF<1>	VOF<0>	Calibration range
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bit<2:1>:VREF<1:0>- ADC internal reference voltage source

VREF<1>	VREF<0>	
0	0	VDD
0	1	4V
1	0	3V
1	1	2V

Bit<0>:ADICS-ADC Internal Channel Select (select ADC internal 1/4 VDD or OP output pin connected to ADC input)

1: Enable

0: Disable

3.1.10 RPAGE0～RB(Converted Value of ADC AD11-AD4)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD<11>	AD<10>	AD<9>	AD<8>	AD<7>	AD<6>	AD<5>	AD<4>

When AD conversion is completed, the result is loaded into the RB. The ADRUN bit is cleared and the ADIF is set.

3.1.11 RPAGE0～RC(Converted Value of ADC AD11-AD8)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	AD<11>	AD<10>	AD<9>	AD<8>

When AD conversion is completed, the result is loaded into the RC. The ADRUN bit is cleared and the ADIF is set.

3.1.12 RPAGE0～RD(Converted Value of ADC AD7-AD0)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD<7>	AD<6>	AD<5>	AD<4>	AD<3>	AD<2>	AD<1>	AD<0>

When AD conversion is completed, the result is loaded into the RD. The ADRUN bit is cleared and the ADIF is set.

3.1.13 RPAGE0～RE(Interrupt Status Register 2 and Wake-up Control Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<7>:LVD_FG- Low voltage Detector state (Read only)
0: Low voltage is detected
1: Low voltage is not detected or LVD function is disabled
Bit<6>:LVDIF-Low Voltage Detector Interrupt flag
1: Detected interrupt
0: No interruption detected
Bit<5>:ADIF-AD Interrupt flag for analog to digital conversion
1: interrupt request
0: no interrupt occurs
Bit<4>:CMPIF-Comparator Interrupt flag
1: interrupt request
0: no interrupt occurs
Bit<3>:ADWE-ADC wake-up enable bit
1: Enable ADC wake-up
0: Disable ADC wake-up
Bit<2>:CMPWE-Comparator wake-up enable bit
1: Enable
0: Disable
Bit<1>: P5ICWE- Port 5 input change to wake-up status enable bit
1: Enable
0: Disable
Bit<0>:LVDWE- Low Voltage Detect wake-up enable bit
1: Enable
0: Disable

3.1.14 RPAGE0～RF(Interrupt Status Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	-	P5ICIF	TCIF

Bit<6>:DT2IF- PWM2 Duty Interrupt flag
Bit<5>:DT1IF-PWM1 Duty Interrupt flag
Bit<4>:PWM2IF-PWM2 Period Interrupt flag
Bit<3>:PWM1IF-PWM1 Period Interrupt flag
Bit<1>:P5ICIF- Port5 input status change interrupt flag
Bit<0>:TCIF- TCC overflow interrupt flag
1: interrupt request
0: no interrupt occurs

3.1.15 RPAGE1～R5(TBHP :Table Point Register for Instruction TBRD)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	-	-	-	-	TAD<10>	TAD<9>	TAD<8>

Bit<7>:MLB- Chooses the MSB or LSB machine code to move into the register
1: High eight
0: Low eight
Bit<6:3>: Not used. Set to “0” at all time
Bit<2:0>:TAD<10:8>- Most 3 significant bits of address for program code

3.1.16 RPAGE1～R6(TBLP: Table Point Register for Instruction TBRD)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAD<7>	TAD<6>	TAD<5>	TAD<4>	TAD<3>	TAD<2>	TAD<1>	TAD<0>

These are the least 8 significant bits of address for program code

3.1.17 RPAGE1～R7(PWM Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PWMCAS	PWM2E	PWM1E

Bit<2>:PWMCAS-PWM Cascade Mode
1: 16-bit PWM Mode
0: Two Independent 8-bit PWM functions
Bit<1>:PWM2E- PWM2 enable bit
1: Enable (P51 output)
0: Disable
Bit<0>:PWM1E- PWM1 enable bit
1: Enable (P67 output)
0: Disable

3.1.18 RPAGE1～R8(TMR Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2EN	T1EN	T2P<2:0>			T1P<2:0>		

Bit<7>:T2EN- TMR2 enable bit
1: Enable
0: Disable

Bit<6>:T1EN- TMR1 enable bit
1: Enable
0: Disable
Bit<5:3>:T2P<2:0>-TMR2 clock prescaler option bits

T2P<2>	T2P<1>	T2P<0>	Prescale
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit<2:0>:T1P<2:0>-TMR1 clock prescaler option bits

T1P<2>	T1P<1>	T1P<0>	Prescale
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.19 RPAGE1～R9(PWM1 Time Period))

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1<7>	PRD1<6>	PRD1<5>	PRD1<4>	PRD1<3>	PRD1<2>	PRD1<1>	PRD1<0>

R9 is the time period of PWM1, Read and write.

3.1.20 RPAGE1～RA(PWM2 Time Period))

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2<7>	PRD2<6>	PRD2<5>	PRD2<4>	PRD2<3>	PRD2<2>	PRD2<1>	PRD2<0>

RA is the time period of PWM2, Read and write.

3.1.21 RPAGE1～RB(PWM1 Duty Cycle)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT1<7>	DT1<6>	DT1<5>	DT1<4>	DT1<3>	DT1<2>	DT1<1>	DT1<0>

A specified value keeps the output of PWM1 to remain high until the value matches with TMR1, Read and write.

3.1.22 RPAGE1～RC(PWM2 Duty Cycle)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT2<7>	DT2<6>	DT2<5>	DT2<4>	DT2<3>	DT2<2>	DT2<1>	DT2<0>

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2, Read and write.

3.1.23 RPAGE1～RE(LVD Interrupt and Wake-up Control Register 2)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD<1:0>		-	-	-	EXWE

Bit<7>:LVDIE- Low voltage detector interrupt enable bit
1: Enable
0: Disable
Bit<6>:LVDEN- Low voltage detector enable bit
1: Enable
0: Disable
Bit<5:4>:LVD<1:0>- Low voltage detector level bits

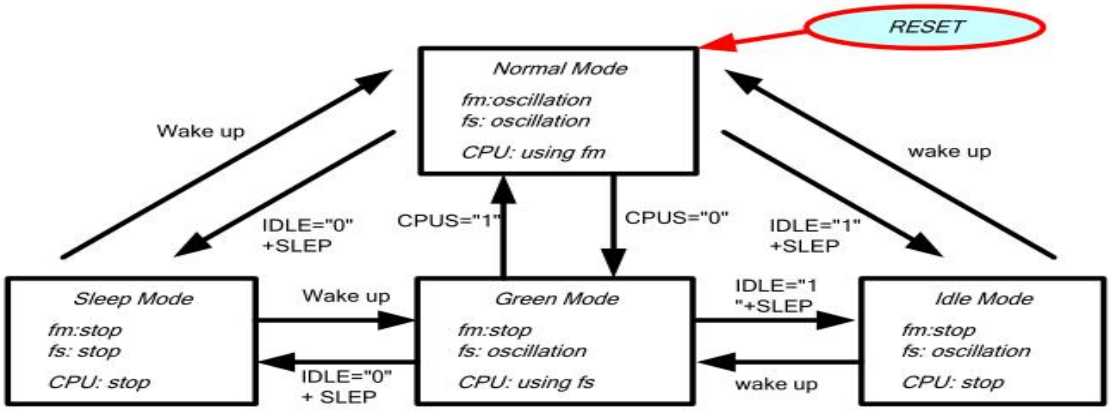
LVD<1>	LVD<0>	LVD voltage selection
0	0	4.5V
0	1	4.0V
1	0	3.3V
1	1	2.2V

Bit<0>:EXWE- External INT wake-up enable bit
1: Enable
0: Disable

3.1.24 RPAGE1～RF(System Clock and Status Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	SHS<1:0>		RCM<1:0>	

Bit<6>:TIMERSC- TCC, PWM1, PWM2 clock source select
1: Fm is used as Fcpu
0: Fs is used as Fcpu
Bit<5>:CPUS- CPU Oscillator Source Select
1: Fm is used as Fcpu
0: Fs is used as Fcpu
Bit<4>:IDLE- Idle Mode Enable Bit
1:IDLE = '1' + SLEP instruction → idle mode
0:IDLE = '0' + SLEP instruction → sleep mode(default)



Bit<3:2>:SHS<1:0>-ADC Sample and Hold Timing Select

SHS<1>	SHS<0>	Sample and Hold Timing(TAD)
0	0	2TAD
0	1	4TAD
1	0	8TAD
1	1	12TAD

Note: the accuracy, linearity, and speed of successive approximation analog-to-digital conversion are determined by the characteristics of the ADC and comparator. The sampling resistance directly affects the time required to keep the capacitor charged. The process controls the sampling time to meet the need for specific accuracy.

In general, the sampling time should increase by at least 2 us for every 1K of impedance increase in the sampling resistance. The maximum impedance of the sampling resistance is recommended to be 10K.

Bit<1:0>:RCM<1:0>: IRC mode select bits

RCM<1>	RCM<0>	Frequency (MHz)
0	0	1M
0	1	8M
1	0	16M
1	1	4M

3.2 Special Purpose Registers

3.2.1 CONT (Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit<6>:INT: Interrupt Enable flag
0: Disabled by DISI or hardware interrupt
1: Enabled by the ENI/RETI instructions
Bit<5>:TS: TCC signal source
1: Transition on the TCC pin
0: Internal instruction cycle clock. If P54 is used as I/O pin
Bit<4>:TE: TCC signal edge
1: Increment if the transition from high to low takes place on the TCC pin
0: Increment if the transition from low to high takes place on the TCC pin
Bit<3>:PSTE: Prescaler enable bit for TCC
1: Prescaler enable bit
0: Prescaler disable bit
Bit<2:0> PST2～PST0: TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Note: CONT register can read and write, and BIT6 is a read-only bit.

3.2.2 IOPAGE0～IOC50～IOC70(I/O Port Control Register)

1:input
0:output

3.2.3 IOPAGE0～IOC80(Comparator/OP AMP Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CMPOUT	COS<1:0>		-	-	-

Bit<7:6>: Not used. Set to “0” all the time
Bit<5>:CMPOUT- Result of the comparator output
1: The in-phase input voltage is greater than the reverse input voltage
0: The in-phase input voltage is less than the reverse input voltage
Bit<4:3>:COS<1:0>

COS<1>	COS<0>	Function select
0	0	Comparator and OP are not used. P64, P65, and P66 are normal I/O pin

0	1	P65 and P66 are Comparator input pins and P64 is normal I/O pin
1	0	P65 and P66 are Comparator input pins and P64 is Comparator output pin
1	1	Used as OP and P64 is OP output pin

Bit<2:0>: Not used. Set to "0" all the time

Note: the IOC80 register BIT<4:0> is read-write, and BIT5 is read-only

3.2.4 IOPAGE0～IOC90(PWM1 Timer)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR1<7:0>							

TMR1, read-only

3.2.5 IOPAGE0～IOCA0(PWM2 Timer)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR2<7:0>							

TMR2, read-only

3.2.6 IOPAGE0～IOCB0(P5 Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P5PD<5>	P5PD<4>	P5PD<3>	P5PD<2>	P5PD<1>	P5PD<0>

Port5 : Control bit used to enable internal pull-down

1: Disable (default)

0: Enable

3.2.7 IOPAGE0～IOCC0(Open-drain Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6OD<7>	P6OD<6>	P6OD<5>	P6OD<4>	P6OD<3>	P6OD<2>	P6OD<1>	P6OD<0>

Port6: Control bit used to enable open-drain output

1: Enable

0: Disable (default)

3.2.8 IOPAGE0～IOCD0(P5 Pull-high Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P5PH<5>	P5PH<4>	P5PH<3>	P5PH<2>	P5PH<1>	P5PH<0>

Port5: Control bit used to enable internal pull-high

1: Disable (default)

0: Enable

3.2.9 IOPAGE0～IOCE0(WDT Control Register and Interrupt Enable Register 2)

Bit 7	Bit6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<7>:WDTE- Control bit used to enable Watchdog Timer

1: Enable

0: Disable

Bit<6>:EIS- Control bit used to define the function of the P60 (INT) pin

1: external interrupt pin
0: P60, bidirectional I/O pin

Bit<5>:ADIE-interrupt enable bit
Bit<4>:CMPIE-interrupt enable bit
Bit<3>:PSWE- Prescaler enable bit for WDT
1: Enable
0: Disable
Bit<2:0>:PSW<2:0>- WDT prescaler bits

PSW<2>	PSW<1>	PSW<0>	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.2.10 IOPAGE0～IOCF0(Interrupt Enable Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	-	P5ICIE	TCIE

Bit<6>: PWM2 duty interrupt enable bit
Bit<5>:PWM1 duty interrupt enable bit
Bit<4>: PWM2 period interrupt enable bit
Bit<3>:PWM1 period interrupt enable bit
Bit<1>:P5ICIE interrupt enable bit
Bit<0>:TCC over flow interrupt enable bit
1: Enable
0: Disable

3.2.11 IOPAGE1～IOC51(P5 High Sink Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	P5HS<4>	P5HS<3>	P5HS<2>	P5HS<1>	-

Port5：Output High Sink current Select
1: Augmentation
0: Normal

P5HS<X>	VDD=5v Sink current
0	20mA (0.6V)
1	45mA (0.6V)

3.2.12 IOPAGE1～IOC61(P6 High Sink Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HS<7>	P6HS<6>	P6HS<5>	P6HS<4>	P6HS<3>	P6HS<2>	P6HS<1>	P6HS<0>

Port6: Output High Sink current Select

1: Augmentation
0: Normal

P6HS<X>	VDD=5v Sink current
0	20mA (0.6V)
1	45mA (0.6V)

3.2.13 IOPAGE1～IOC71(P5 High Driver Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	P5HD<4>	P5HD<3>	P5HD<2>	P5HD<1>	-

Port5: Output High Driver current Select
1: Augmentation
0: Normal

P5HD<X>	VDD=5v Driver current
0	5mA (4.4V)
1	12mA (4.4V)

3.2.14 IOPAGE1～IOC81(P6 High Driver Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HD<7>	P6HD<6>	P6HD<5>	P6HD<4>	P6HD<3>	P6HD<2>	P6HD<1>	P6HD<0>

Port6: Output High Driver current Select
1: Augmentation
0: Normal

P6HD<X>	VDD=5v Driver current
0	5mA (4.4V)
1	12mA (4.4V)

3.2.15 IOPAGE1～IOCF1(P6 Pull-high Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PH<7>	P6PH<6>	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>

Port6: Control bit used to enable pull-high
1: Disable
0: Enable

3.3 GPIO Function Module

JZ8ME2602C has three sets of bidirectional I/O ports, 16 inputs and 16 outputs (P71 open-drain output), most of which can be reused for other functions.

14 programmable pull up I/O pins:P5.0～P5.5, P6.0～P6.7;

6 programmable pull down I/O pins:P5.0～P5.5;

12 programmable driver enhanced I/O pins:P5.1～P5.4, P6.0～P6.7;

8 programmable drain open I/O pins:P6.0～P6.7;

3.3.1 GPIO Register Specification

RPAGE0～R5 (PORT5 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P55	P54	P53	P52	P51	P50

Port input/output registers, P5 ports are 8-bit

P5 is a readable and writable register.

RPAGE0～R6 (PORT6 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

Port input/output registers, P6 ports are 8-bit

P6 is a readable and writable register.

RPAGE0～R7 (PORT7 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	P71	P70

Port input/output registers, P7 ports are 2-bit

P7 is a readable and writable register.

IOPAGE0～IOC50(P5 Port Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P5CR<5>	P5CR<4>	P5CR<3>	P5CR<2>	P5CR<1>	P5CR<0>

Port5 Port Control Register

1: input (default)

0: output

IOPAGE0～IOC60(P6 Port Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6CR<7>	P6CR<6>	P6CR<5>	P6CR<4>	P6CR<3>	P6CR<2>	P6CR<1>	P6CR<0>

Port6 Port Control Register

1: input (default)

0: output

IOPAGE0～IOC70(P7 Port Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	P7CR<1>	P7CR<0>

Bit<1:0>:Port7 Port Control Register

1: input (default)

0: output

IOPAGE0～IOCB0(P5 Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P5PD<5>	P5PD<4>	P5PD<3>	P5PD<2>	P5PD<1>	P5PD<0>

Port5 Control bit used to enable internal pull-down

1: Disable (default)

0: Enable

IOPAGE0～IOCC0(P6 Open-drain Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6OD<7>	P6OD<6>	P6OD<5>	P6OD<4>	P6OD<3>	P6OD<2>	P6OD<1>	P6OD<0>

Port6 Control bit used to enable open-drain output

1: Enable

0: Disable (default)

IOPAGE0～IOCD0(P5 Pull-high Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P5PH<5>	P5PH<4>	P5PH<3>	P5PH<2>	P5PH<1>	P5PH<0>

Port5 Control bit used to enable internal pull-high

1: Disable (default)

0: Enable

IOPAGE1～IOC51(P5 High Sink Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	P5HS<4>	P5HS<3>	P5HS<2>	P5HS<1>	-

Port5 Output High Sink current Select

1: Augmentation

0: Normal

P5HS<X>	VDD=5v Sink current
0	20mA (0.6V)
1	45mA (0.6V)

IOPAGE1～IOC61(P6 High Sink Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HS<7>	P6HS<6>	P6HS<5>	P6HS<4>	P6HS<3>	P6HS<2>	P6HS<1>	P6HS<0>

Port6 Output High Sink current Select

1: Augmentation

0: Normal

P6HS<X>	VDD=5v Sink current
0	20mA (0.6V)
1	45mA (0.6V)

IOPAGE1～IOC71(P5 High Driver Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	P5HD<4>	P5HD<3>	P5HD<2>	P5HD<1>	-

Port5 Output High Driver current Select

1: Augmentation

0: Normal

P5HD<X>	VDD=5v Driver current
0	5mA (4.4V)
1	12mA (4.4V)

IOPAGE1～IOC81(P6 High Driver Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HD<7>	P6HD<6>	P6HD<5>	P6HD<4>	P6HD<3>	P6HD<2>	P6HD<1>	P6HD<0>

Port6 Output High Driver current Select

1: Augmentation

0: Normal

P6HD<X>	VDD=5v Driver current
0	5mA (4.4V)
1	12mA (4.4V)

IOPAGE1～IOCF1(P6 Pull-high Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PH<7>	P6PH<6>	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>

Port6 Control bit used to enable pull-high

1: Disable (default)

0: Enable

3.4 TCC Function Module

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST2~PST0 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PSW2~PSW0 bits of the IOCE0 register are used to determine the prescaler of WDT. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-3 depicts the block diagram of TCC/WDT.

In IDLE mode, a TCC interrupt can wake up the chip.

3.4.1 TCC Register Specification

RPAGE0~R1 (Time Clock/Counter)

TCC (R1) is an 8-bit timer/counter. The TCC clock source can be internal clock (Fm/Fs) or external signal input (edge selectable from the TCC pin).

If TCC signal source is from the internal clock, TCC will be incremented by 1 at every instruction cycle (without prescaler). If TCC signal source is from an external clock, the TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept at High or Low level) must be greater than Fm clock or Fs clock, determine by Bank 1 RF CPUS bit.

RPAGE0~RF(Interrupt Status Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	-	P5ICIF	TCIF

Bit<0>:TCIF- TCC overflow interrupt flag
1: interrupt request
0: no interrupt occurs

CONT (Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit<6>:INT: Interrupt Enable flag
0: Disabled by DISI or hardware interrupt
1: Enabled by the ENI/RETI instructions
Bit<5>:TS: TCC signal source
1: Transition on the TCC pin
0: Internal instruction cycle clock. If P54 is used as I/O pin
Bit<4>:TE: TCC signal edge
1: Increment if the transition from high to low takes place on the TCC pin
0: Increment if the transition from low to high takes place on the TCC pin
Bit<3>:PSTE: Prescaler enable bit for TCC
1: Prescaler enable bit
0: Prescaler disable bit
Bit<2:0> PST2~PST0: TCC prescaler bits

PST2	PST1	PST0	TCC 分频系数
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

IOPAGE0～IOCF0(Interrupt Enable Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	P5ICIE	TCIE

Bit<0>:TCIE-TCC over flow interrupt enable bit

1: Enable

0: Disable

RPAGE1～RF(System Clock and Status Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	SHS<1:0>		RCM<1:0>	

Bit<6>:TIMERSC- TCC, PWM1, PWM2 clock source select

1: Fm is used as Fcpu

0: Fs is used as Fcpu

3.4.2 TCC Setting Instructions

1. Assign initial value to TCC register;
2. Set the value of CONT register;
3. As a counter, it is necessary to select the TCC input signal in the CONT register to add 1 to the rising edge or the falling edge;
4. If the interrupt function needs to be performed, set the TCIE (Bit0) in the IOCF0 register to 1 and execute the ENI instruction.
5. The interrupt program will automatically save ACC, STATUS and R4 in the stack, and then take them out from the stack after executing RETI instruction. The TCC interrupt marker should be clear before exiting the interrupt.

3.5 WDT Function Module

WDT is a 12-bit counter with two enabling signal controls (ENWDT in OPTION and WDTE control bits in IOCE register). The counting clock is provided by a separate oscillator, so WDT can still run (if enabled) after the system goes into sleep mode, and the overflow of WDT can reset the system in either normal mode or sleep mode. The reset time is selected by the control bit WDTPS implementation in OPTION at 4.5ms or 18ms.

System to provide a 8-bit counter as WDT divider, through IOCE0 register Settings.

3.5.1 WDT Register Specification

IOPAGE0～IOCE0(WDT Control Register and Interrupt Enable Register 2)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<7>:WDTE- Control bit used to enable Watchdog Timer

1: Enable

0: Disable

Bit<3>:PSWE- Prescaler enable bit for WDT

1: Enable

0: Disable

Bit<2:0>:PSW<2:0>- WDT prescaler bits

PSW<2>	PSW<1>	PSW<0>	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.5.2 WDT Setting Instructions

1. Set Bit7(WDTE) in register IOCE0;
2. Set the predivider coefficient;
3. If WDT is enabled, other WDT awakenings are prohibited.

3.6 IO Change Wake-up/Interrupt Function Module

After executing the SLEEP command, the system goes into SLEEP mode (IDLE=0), the system clock stops, and all modules stop working except WDT (if enabled). If SLEEP is performed during AD conversion, the system clock, TCC, TMR1, TMR2, TMR3, and WDT (if enabled) continue to run.

3.6.1 Description of Wake Up Mode

- RESET pin input low level;
- WDT reset;
- Port input state changed;
- Comparator state changes;
- AD conversion completed;
- LVD low voltage detection;
- External interrupt pin wake up;

The first and second awakenings reset the system, thus terminating all procedures performed before sleep.

Other wake up modes can continue the program by programmatically choosing to continue the original process (DISI before SLEEP) or to perform the corresponding jump (ENI before SLEEP), and turn on the corresponding enable control to jump to the interrupt vector.

3.6.2 Port Status Changes Wake Up Register Description

RPAGE0～RE(Interrupt Status Register 2 and Wake-up Control Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<1>: P5ICWE- Port 5 input change to wake-up status enable bit

1: Enable

0: Disable

RPAGE0～RF(Interrupt Status Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	-	P5ICIF	TCIF

Bit<1>:P5ICIF-Port5 input status change interrupt flag

1: interrupt request

0: no interrupt occurs

IOPAGE0～IOCF0(Interrupt Enable Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	-	P5ICIE	TCIE

Bit<1>:P5ICIE interrupt enable bit

1: Enable

0: Disable

3.6.3 P5 Port State Changes Query Mode Wake-up Settings

1. Set the wake-up port as input;
2. Set the pull up or pull down of IO port;
3. Enable ICIE and wake up control;
4. Set the P5ICWE of register RPAGE0-RE as 1 enabling wake up function;
5. Execute DISI instruction and do not enter the interrupt address port;
6. Read PORT ports (such as MOV 0X05,0X05);
7. Execute the "SLEP" instruction and enter the sleep (IDLE=0)/ IDLE (IDLE=1) mode;
8. After awakening, execute the next instruction of the SLEP.

3.6.4 P5 Port State Changes Interrupt Mode Wake-up Settings

1. Set the wake-up port as input;
2. Set the pull up or pull down of IO port;
3、The setting of WDT predivider must be greater than 1:1, WDT is forbidden;
4、Enable ICIE and wake up control;
5、Set the P5ICWE of register RPAGE0-RE as 1 enabling wake up function;
6、Enable the state of the PORT to change and interrupt;
7、Execute "ENI" instruction and wait to enter the interrupt address port;
8、Read PORT ports (such as MOV 0X05,0X05);
9、Execute the "SLEP" instruction and enter the sleep (IDLE=0)/ IDLE (IDLE=1) mode;
10、After awakening, it will enter the interrupt address port. After exiting the interrupt, it will execute the next instruction of SLEP.

3.7 LVD Function Module

JZ8ME2602C has the function of low voltage detection (LVD). Four voltage values can be selected programmatically. If Vdd drops below the low voltage detector level, LVD (Bit 7 of RE) is cleared to "0" to show a low voltage signal when LVD is enabled. This signal can be used for low voltage detection.

3.7.1 LVD Register Specification

RPAGE0~RE(Interrupt Status Register 2 and Wake-up Control Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<7>:LVD_FG- Low voltage Detector state (Read only)
0: Low voltage is detected
1: Low voltage is not detected or LVD function is disabled
Bit<6>:LVDIF- Low Voltage Detector Interrupt flag
1: Detected interrupt
0: No interruption detected
Bit<0>:LVDWE- Low Voltage Detect wake-up enable bit
1: Enable
0: Disable

RPAGE1~RE(LVD Interrupt and Wake-up Control Register 2)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD<1:0>		-	-	-	EXWE

Bit<7>:LVDIE- Low voltage detector interrupt enable bit
1: Enable
0: Disable
Bit<6>:LVDEN- Low voltage detector enable bit
1: Enable
0: Disable
Bit<5:4>:LVD<1:0>- Low voltage detector level bits

LVD<1>	LVD<0>	LVD voltage selection
0	0	4.5V
0	1	4.0V
1	0	3.3V
1	1	2.2V

3.7.2 LVD Setting Instructions

1. Set the voltage value of LVD (LVD1 and LVD0 bits of RPAGE1 RE register);
2. Enable LVD function (RPAGE1 RE register LVDEN bit);
3. Enable LVD interrupt (LVDIE bit of RPAGE1 RE register), execute "ENI" instruction (if LVD interrupt is required);
4. After the interrupt subroutine or main program judges that LVDIF bit is 1, then judge the LVD_FG bit of RPAGE0 RE register and execute the corresponding action.

3.8 ADC Function Module

JZ8ME2602C has an 7-channel input channel, 12-bit ADC. Three control registers (AISR/R8, ADCON/R9, & ADOC/RA), three data registers (ADDATA/RB, ADDATA1H/RC, and ADDATA1L/RD) and an ADC with 12-bit resolution . The analog reference voltage (Vref) and the analog ground are connected via separate input pins. Connecting to an external VREF is more accurate than connecting to an internal VDD.

AD Sampling time calculation:

From setting ADRUN=1, AD Sampling time = **ADC sampling retention period + AD conversion time**

3.8.1 ADC Register Specification

RPAGE0～R8(ADC Input Select Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ADE<6>	ADE<5>	ADE<4>	ADE<3>	ADE<2>	ADE<1>	ADE<0>

Bit<7:0>:ADE<7:0>-AD converter enable bit

1: Enable

0: Disable

Channel number	Enable control	Corresponding pin
AD0	ADE<0>	P50
AD1	ADE<1>	P51
AD2	ADE<2>	P52
AD3	ADE<3>	P53
AD4	ADE<4>	P67
AD5	ADE<5>	P70
AD6	ADE<6>	P55

Registers are readable and writable

RPAGE0～R9(ADC Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR<1:0>		ADRUN	ADPD	ADIS<2:0>		

Bit<7>:VREFS- The input source of Vref of the ADC

1: The Vref of the ADC is connected to P54

0: The Vref of the ADC is connected to VREF (Vdd is default value)

Bit<6:5>:CKR<1:0>（**ADC Clock Rate Select**）

CPUS	CKR<1>	CKR<0>	ADCclock
1	0	0	Fosc/16
1	0	1	Fosc/4
1	1	0	Fosc/64
1	1	1	Fosc/1
0	x	x	Fosc/1

Bit<4>:ADRUN- ADC starts to RUN

1: Enable

0: Disable

Bit<3>:ADPD- ADC Power
1: Enable
0: Disable
Bit<2:0>:ADIS<2:0>- Analog Input Select

ADICS	ADIS<2>	ADIS<1>	ADIS<0>	ADC Input Select
0	0	0	0	P50
0	0	0	1	P51
0	0	1	0	P52
0	0	1	1	P53
0	1	0	0	P67
0	1	0	1	P70
0	1	1	0	P55
1	0	0	0	OPOUT
1	1	0	0	0.25*VDD

Note: Fosc represents the oscillator clock. For example, if the IRC frequency is selected as 4M, then Fosc=4M
For example:Fosc=4M, TAD set Fosc/4, then TAD=1US

RPAGE0～RA(ADC Offset Calibration Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF<2:0>			VREF<1:0>		ADICS

Bit<7>:CALI- Calibration enable bit for ADC offset
1: Enable
0: Disable
Bit<6>:SIGN- Polarity bit of the offset voltage
1: Positive voltage
0: Negative voltage
Bit<5:3>:VOF<2:0>-ADC Offset voltage bits

VOF<2>	VOF<1>	VOF<0>	Calibration range
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bit<2:1>:VREF<1:0>- ADC internal reference voltage source

VREF<1>	VREF<0>	
0	0	VDD
0	1	4V
1	0	3V

1	1	2V

Bit<0>:ADICS- ADC Internal Channel Select (select ADC internal 1/4 VDD or OP output pin connected to ADC input)

1: Enable

0: Disable

RPAGE0～RB(Converted Value of ADC AD11-AD4)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD<11>	AD<10>	AD<9>	AD<8>	AD<7>	AD<6>	AD<5>	AD<4>

When AD conversion is completed, the result is loaded into the RB. The ADRUN bit is cleared and the ADIF is set.

RPAGE0～RC(Converted Value of ADC AD11-AD8)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	AD<11>	AD<10>	AD<9>	AD<8>

When AD conversion is completed, the result is loaded into the RC. The ADRUN bit is cleared and the ADIF is set.

RPAGE0～RD(Converted Value of ADC AD7-AD0)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD<7>	AD<6>	AD<5>	AD<4>	AD<3>	AD<2>	AD<1>	AD<0>

When AD conversion is completed, the result is loaded into the RC. The ADRUN bit is cleared and the ADIF is set.

RPAGE0～RE(Interrupt Status Register 2 and Wake-up Control Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<5>:ADIF-AD Interrupt flag for analog to digital conversion

1: interrupt request

0: no interrupt occurs

Bit<3>:ADWE- ADC wake-up enable bit

1: Enable ADC wake-up

0: Disable ADC wake-up

RPAGE1～RF(System Clock and Status Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	SHS<1:0>		RCM<1:0>	

Bit<3:2>:SHS<1:0>-ADC Sample and Hold Timing Select

SHS<1>	SHS<0>	Sample and Hold Timing(TAD)
0	0	2TAD
0	1	4TAD
1	0	8TAD
1	1	12TAD

Note: the accuracy, linearity, and speed of successive approximation analog-to-digital conversion are determined by the characteristics of the ADC and comparator. The sampling resistance directly affects the time required to keep the

capacitor charged. The process controls the sampling time to meet the need for specific accuracy.

In general, the sampling time should increase by at least 2 us for every 1K of impedance increase in the sampling resistance. The maximum impedance of the sampling resistance is recommended to be 10K.

IOPAGE0～IOCE0(WDT Control Register and Interrupt Enable Register 2)

Bit 7	Bit6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<5>:ADIE- ADIF interrupt enable bit

1: Enable

0: Disable

3.8.2 ADC Setting Instructions

1. Set registers RPAGE0-R8 to enable analog input channels;
2. Set ADIS2: ADIS0 of registers RPAGE0-R9 to select the AD input channel; set CKR1-CKR0 of registers RPAGE0-R9 to select the clock prescaler of the ADC; select the reference voltage of the ADC; set “ADPD = 1” to start the AD power supply Voltage;
3. Call the AD accuracy correction subroutine;
4. If you need to use the interrupt function, set ADIE = 1 and execute the "ENI" instruction;
5. You can enable the AD wake-up function according to your needs and set ADWE = 1;
6. Set "ADRUN = 1" to start AD conversion;
7. Select IDLE / SLEEP mode as required;
8. Wait for the interrupt or ADRUN to be cleared to 0; if an AD interrupt occurs, you need to clear ADIF to "0" when leaving the interrupt routine
9. Save the result of the conversion. If multiple AD conversions are required, skip to step 5.

3.8.3 ADC Conversion Accuracy Adjustment Instructions

1. Set registers RPAGE0-R8 to enable analog input channels;
2. Set ADIS2: ADIS0 of registers RPAGE0-R9 to select the AD input channel; set CKR1-CKR0 of registers RPAGE0-R9 to select the clock prescaler of the ADC; select the reference voltage of the ADC; set “ADPD = 1” to turn on the ADC power ;
3. Set ADOC to 0XF8, enable ADC correction bit function, set “ADRUN = 1” to start AD conversion;
4. Correct the ADC positive voltage first, then correct the ADC negative voltage, and correct the voltage of 2LSB each time;
5. When the AD value is detected as “0”, the AD accuracy correction is ended, that is, the “CALI” bit value of the ADC is “0”.

3.9 PWM Function Module

JZ8ME2602C has two built-in counters with prescaler, which are used to generate pulse width modulation signals. Among them, PWM1 and PWM2 are 8Bit (configurable combination is 16Bit).

3.9.1 PWM Register Specification

RPAGE0～RF(Interrupt Status Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	-	P5ICIF	TCIF

Bit<6>:DT2IF- PWM2 Duty Interrupt flag
Bit<5>:DT1IF-PWM1 Duty Interrupt flag
Bit<4>:PWM2IF-PWM2 Period Interrupt flag
Bit<3>:PWM1IF-PWM1 Period Interrupt flag
1: interrupt request
0: no interrupt occurs

RPAGE1～R7(PWM Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PWMCAS	PWM2E	PWM1E

Bit<2>:PWMCAS- PWM Cascade Mode
1: 16-bit PWM Mode
0: Two Independent 8-bit PWM functions
Bit<1>:PWM2E- PWM2 enable bit
1: Enable (P51 output)
0: Disable
Bit<0>:PWM1E- PWM1 enable bit
1: Enable (P67 output)
0: Disable

RPAGE1～R8(TMR Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2EN	T1EN	T2P<2:0>			T1P<2:0>		

Bit<7>:T2EN- TMR2 enable bit
1: Enable
0: Disable
Bit<6>:T1EN- TMR1 enable bit
1: Enable
0: Disable
Bit<5:3>:T2P<2:0>-TMR2 clock prescaler option bits

T2P<2>	T2P<1>	T2P<0>	Prescale
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8

1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit<2:0>:T1P<2:0>-TMR1 clock prescaler option bits

T1P<2>	T1P<1>	T1P<0>	Prescale
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

RPAGE1～R9(PWM1 Time Period)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1<7>	PRD1<6>	PRD1<5>	PRD1<4>	PRD1<3>	PRD1<2>	PRD1<1>	PRD1<0>

R9 is the time period of PWM1, Read and write.

RPAGE1～RA(PWM2 Time Period)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2<7>	PRD2<6>	PRD2<5>	PRD2<4>	PRD2<3>	PRD2<2>	PRD2<1>	PRD2<0>

RA is the time period of PWM2, Read and write.

RPAGE1～RB(PWM1 Duty Cycle)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT1<7>	DT1<6>	DT1<5>	DT1<4>	DT1<3>	DT1<2>	DT1<1>	DT1<0>

A specified value keeps the output of PWM1 to remain high until the value matches with TMR1, Read and write.

RPAGE1～RC(PWM2 Duty Cycle)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT2<7>	DT2<6>	DT2<5>	DT2<4>	DT2<3>	DT2<2>	DT2<1>	DT2<0>

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2, Read and write.

RPAGE1～RF(System Clock and Status Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	SHS<1:0>		RCM<1:0>	

Bit<6>:TIMERSC- TCC, PWM1, PWM2 clock source select

1: Fm is used as Fcpu

0: Fs is used as Fcpu

IOPAGE0～IOC90(TMR1 Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR1<7:0>							

TMR1, read-only

IOPAGE0～IOCA0(TMR2 Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR2<7:0>							

TMR2, read-only

IOPAGE0～IOCF0(Interrupt Enable Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	-	P5ICIE	TCIE

Bit<6>:DT2IE- PWM2 duty interrupt enable bit
Bit<5>:DT1IE- PWM1 duty interrupt enable bit
Bit<4>:PWM2IE- PWM2 period interrupt enable bit
Bit<3>:PWM1IE-PWM1 period interrupt enable bit
1: Enable
0: Disable

3.9.2 PWM Setting Instructions

1. Set the RPAGE1-R7 and RPAGE1-R8 registers, and select the corresponding timers as PWM mode, timer divide ratio, timer interrupt type (if PWM interrupt is enabled), timer clock source ;
2. Write the values of the RPAGE1-R9 and RPAGE1-RA registers to determine the period of the PWM channel;
3. Write the RPAGE1-RB and RPAGE1-RC registers to determine the Duty of the PWM channel.
4. Enable the corresponding timer;
5. Enable or disable the timer interrupt corresponding to PWM, and enable “ENI” or “DISI” instruction (if needed).

3.10 CMP/OP Function Module

The JZ8ME2602C has one comparator which has two analog inputs and one output. The comparator can be employed to wake up the system from sleep/idle mode. The comparator can be used as an operation amplifier if a feedback resistor is externally connected from the input to the output.

3.10.1 CMP/OP Function Module

IOPAGE0～IOC80(Comparator/OP AMP Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	CMPOUT	COS<1:0>		0	0	0

Bit<7:6>: Not used. Set to "0" all the time

Bit<5>:CMPOUT- Result of the comparator output

1: The in-phase input voltage is greater than the reverse input voltage

0: The in-phase input voltage is less than the reverse input voltage

Bit<4:3>:COS<1:0>

COS<1>	COS<0>	Function select
0	0	Comparator and OP are not used. P64, P65, and P66 are normal I/O pin
0	1	P65 and P66 are Comparator input pins and P64 is normal I/O pin
1	0	P65 and P66 are Comparator input pins and P64 is Comparator output pin
1	1	Used as OP and P64 is OP output pin

Bit<2:0>: Not used. Set to "0" all the time

IOPAGE0～IOCE0(WDT Control Register and Interrupt Enable Register 2)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<4>:CMPIE-interrupt enable bit

1: Enable

0: Disable

RPAGE0～RE(Interrupt Status Register 2 and Wake-up Control Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<4>:CMPIF- Comparator Interrupt flag

1: interrupt request

0: no interrupt occurs

Bit<2>:CMPWE- Comparator wake-up enable bit

1: Enable

0: Disable

3.10.2 CMP Setting Instructions

1. Set CIN + and CIN- as input ports and CO as output port;
2. Set COS1 / COS0 = 0/1 or 1/0 of the IOC80 register as a comparator;
3. According to the needs, the comparator interrupt function can be enabled and the "ENI" instruction is executed to enter the interrupt address port;
4. You can enable the wake-up function as required.

note:

1. The comparator wake-up and interrupt are both enabled. If the comparator output status changes, the program wakes up from sleep mode, executes the interrupt program, and then runs the next statement of "SLEP";
2. The offset voltage of the comparator is 10mV.

3.10.3 OP Setting Instructions

1. Set CIN + and CIN- as input ports and CO as output port;
2. Set COS1 / COS0 = 1/1 of the IOC80 register as an operational amplifier.

3.11 Interrupt Function Module

JZ8ME2602C has 9 interrupt sources. No matter which one is used, the total interrupt must be enabled, that is, the "ENI" instruction is issued. The following are the characteristics, interrupt addresses and priority levels of each interrupt:

	Interrupt source	Enabling conditions	Interrupt flag	Interrupt vector	priority
External	Port 5 pin change	ENI + ICIE=1	ICIF	006H	2
Internal	TCC overflow interrupt	ENI + TCIE=1	TCIF	009H	3
Internal	AD conversion complete interrupt	ENI + ADIE=1	ADIF	00CH	4
Internal	Comparator interrupt	ENI + CMPIE=1	CMPIF	00FH	5
Internal	PWM1 period match interrupt	ENI + HPWTIE =1	HPWTIF	012H	6
Internal	PWM2 period match interrupt	ENI + LPWTIE =1	LPWTIF	015H	7
Internal	PWM1 duty match interrupt	ENI+TCCAIE=1	TCCAIF	018H	8
Internal	PWM2 duty match interrupt	ENI+TCCBIE=1	TCCBIF	01BH	9
Internal	Low Voltage Detector interrupt	ENI+LVDIE=1	LVDIF	021H	1

RF and RE are the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF0 and IOCE0 are Interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

Before an interrupt subroutine is executed, the contents of ACC and the R3 and R4 registers are saved first by the hardware. If another interrupt occurs, the ACC, R3, and R4 will be replaced by the new interrupt. After an interrupt service routine is completed, the ACC, R3, and R4 registers are restored.

3.11.1 Interrupt Register Specification

RPAGE0～RE(Interrupt Status Register 2 and Wake-up Control Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<6>:LVDIF- Low Voltage Detector Interrupt flag
1: Detected interrupt
0: No interruption detected
Bit<5>:ADIF-AD Interrupt flag for analog to digital conversion
1: interrupt request
0: no interrupt occurs
Bit<4>:CMPIF- Comparator Interrupt flag
1: interrupt request
0: no interrupt occurs

RPAGE0～RF(Interrupt Status Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	-	P5ICIF	TCIF

Bit<6>:DT2IF- PWM2 Duty Interrupt flag
Bit<5>:DT1IF-PWM1 Duty Interrupt flag
Bit<4>:PWM2IF-PWM2 Period Interrupt flag
Bit<3>:PWM1IF-PWM1 Period Interrupt flag
Bit<1>:P5ICIF- Port 5 input status change interrupt flag
Bit<0>:TCIF- TCC overflow interrupt flag
1: interrupt request
0: no interrupt occurs

RPAGE1～RE(LVD Interrupt and Wake-up Control Register 2)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD<1:0>		-	-	-	EXWE

Bit<7>:LVDIE- Low voltage detector interrupt enable bit
1: Enable
0: Disable

IOPAGE0～IOCE0(WDT Control Register and Interrupt Enable Register 2))

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<6>:EIS- Control bit used to define the function of the P60 (INT) pin
1: external interrupt pin
0: P60, bidirectional I/O pin
Bit<5>:ADIE- ADIF interrupt enable bit
Bit<4>:CMPIE- CMPIF interrupt enable bit

IOPAGE0～IOCF0(Interrupt Enable Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	P5ICIE	TCIE

Bit<6>:DT2IE- PWM2 duty interrupt enable bit
Bit<5>:DT1IE- PWM1 duty interrupt enable bit
Bit<4>:PWM2IE- PWM2 period interrupt enable bit
Bit<3>:PWM1IE-PWM1 period interrupt enable bit
Bit<2>:EXIE- EXIF interrupt enable bit
Bit<1>:P5ICIE- ICIF interrupt enable bit
Bit<0>:TCIE- TCC over flow interrupt
1: Enable
0: Disable

3.12 Reset Function Module

3.12.1 Reset Register Specification

JZ8ME2602C provides 4 reset methods

1、Power-on reset

2、RESET pin input “low”

3、WDT time-out (if enabled)

4、LVR low voltage reset

The first reset time is determined by the SUT selection in OPTION, as shown in the following table:

SUT	Reset setup time
1	18ms
0	4.5ms

Once a reset occurs, the following functions are performed (the initial Address is 0000h).

3.12.2 Power On Reset

Any microcontroller is not warranted to start operating properly before the power supply stabilizes in steady state.

Under customer application, when power is switched OFF, Vdd must remain at OFF state for 10us before power can be switched ON again. Subsequently, the JZ8ME2602C will reset and work normally.

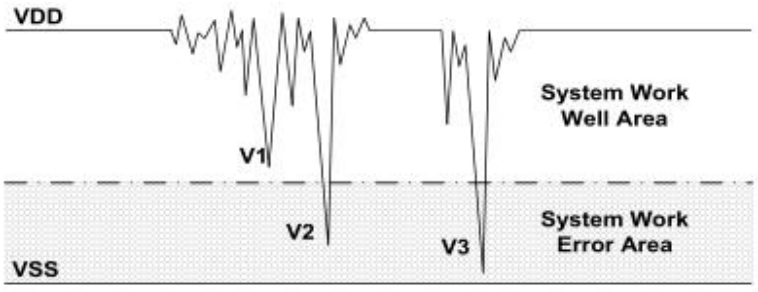
3.12.3 WDT Reset

Watchdog reset is a protection setting of the system. Under normal conditions, the watchdog timer is cleared by the program. If an error occurs, the system is in an unknown state, the watchdog timer overflows, and the system resets. After the watchdog resets, the system restarts into the normal state.

3.12.4 Low Voltage Reset

The Low Voltage Reset (LVR) is designed for unstable power situation, such as external power noise interference.

When LVR is enabled, the system supply voltage (Vdd) drops below Vdd reset level (VRESET) and remains at 10us, a system reset will occur and the system will remain in reset status. The system will remain at reset status until Vdd voltage rises above Vdd release level.



Brown Out Reset Diagram

The power dropping might through the voltage range that’s the system dead-band. The dead-band means the power range can’t offer the system minimum operation power

requirement. The above diagram is a typical brown out reset diagram. There is a serious noise under the VDD, and VDD voltage drops very deep. There is a dotted line to separate the system working area. The above area is the system work well area. The below area is the system work error area called dead-band. V1 doesn't touch the below area and not effect the system operation. But the V2 and V3 is under the below area and may induce the system error occurrence. Let system under dead-band includes some conditions.

3.12.5 Relationship Between Frequency and LVR

To avoid voltage dead zone occurs, to select the appropriate reset voltage LVR point (Fcpu = oscillator frequency / clocks dividing; e.g. IRC frequency = 4M, clocks divider = 2 Clocks, then Fcpu = 2M;).

Fcpu	LVR
Fcpu<=2M	No less than 1.8V
2M<Fcpu<=4M	No less than 2.7V
4M<Fcpu<=6M	No less than 3.5V
Fcpu>6M	Must 4.0V

3.13 System Clock Function Module

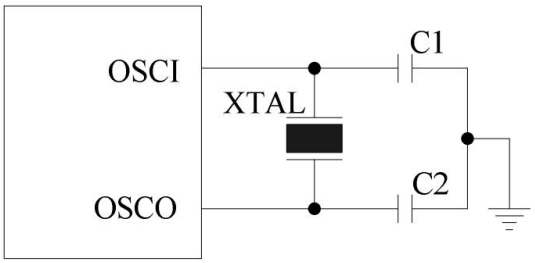
The JZ8ME2602C can be operated in six different oscillator modes, such as Crystal Oscillator Mode (XT), High Crystal Oscillator Mode 1 (HXT1), High Crystal Oscillator Mode 2 (HXT2), Low Crystal Oscillator Mode 1 (LXT1), Low Crystal Oscillator Mode 2 (LXT2), External RC Oscillator Mode (ERC), and RC Oscillator Mode with Internal RC Oscillator Mode (IRC). User can select one of the six modes by programming the OSC3, OSC2, OCS1, and OSC0 in the Code Option register.

Oscillator Modes	Description
ERC（External RC oscillator mode）	P55:ERCIN; P70:GPIO
ERC（External RC oscillator mode）	P55:ERCIN; P50:RCOUT
IRC（Internal RC oscillator mode）	RCM select 1M/2M/4M/8M P55:GPIO; P70:GPIO
IRC（Internal RC oscillator mode）	RCM select 1M/2M/4M/8M P55:GPIO; P70:RCOUT
LXT1	100K～1M
HXT1	12M～16M
LXT2	32.768KHz
HXT2	6M～12M
XT	1M～6M

Note: The system frequency transition point between HXT and LXT is around 400kHz.

3.13.1 System Clock Function Module (XT)

In most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation.



Crystal/Resonator Circuit

Capacitor selection guide for crystal oscillator or ceramic resonators:

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	LXT1 (100K～1M)	100 KHz	60	60
		200 KHz	60	60
		455 KHz	40	40
		1 MHz	30	30
	XT (1M～6M)	1 MHz	30	30
		2 MHz	30	30
		4 MHz	20	20
	LXT2 (32.768K)	32.768 KHz	40	40

Crystal Oscillator	LXT1 (100K～1M)	100 KHz	60	60
		200 KHz	60	60
		455 KHz	40	40
		1 MHz	30	30
	XT (1M～6M)	1 MHz	30	30
		2 MHz	30	30
		4 MHz	20	20
		6 MHz	30	30
	HXT2 (6M～12M)	6 MHz	30	30
		8 MHz	20	20
		12 MHz	30	30
	HXT1 (12M～16M)	12 MHz	30	30
		16 MHz	20	20

Note: The above data is for reference only, all are subject to physical testing.

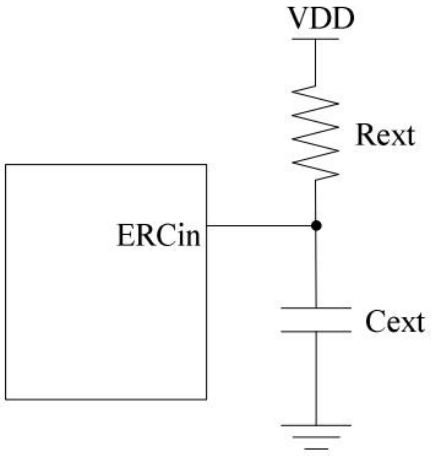
3.13.2 External RC Oscillator Mode (ERC)

For some applications that do not require precise timing calculation, the RC oscillator could offer an effective cost savings.

Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to the manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should be not lesser than 20 pF, and the value of Rext should not be greater than 1 M . If the frequency cannot be kept within this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 K , the oscillator will become unstable because the NMOS cannot correctly discharge the capacitance current.



External RC Oscillator Mode Circuit

The RC Oscillator frequencies, for reference only:

Rext	Cext	Frequency
5.1K	100p	427.2KHz
	200p	254.4KHz
	300p	189.4KHz

3.13.3 Internal RC Oscillator Mode (IRC)

The JZ8ME2602C offers a versatile internal RC mode with default frequency value of 4MHz.

Internal RC oscillator mode has other frequencies (16 MHz, 8 MHz, and 1 MHz) that can be set by Code Option, RCM1, and RCM0:

Firc	IRC Frequency
4 M	IRC 4MHz
16 M	IRC 16MHz
8 M	IRC 8MHz
1 M	IRC 1MHz

3.13.4 Frequency and Power Consumption

Fcpu	Power selection	Note: (Fcpu = Oscillator frequency / clocks frequency division)
Fcpu>=2M	High speed and high power consumption	When Fcpu>= 2M, high speed and high power consumption must be selected
Fcpu<2M	High speed and high power consumption	When Fcpu < 2M, choose high speed and high power consumption, the strongest anti-interference, relatively high power consumption, suitable for AC power supply
Fcpu<2M	normal	When Fcpu < 2M, choose normal, the power consumption is relatively low

Note: The power consumption mentioned above refers to the normal working current, not the sleep current. Full sleep power is not affected by this.

4 CODE OPTION Register

CODE OPTION	Option	Function description
WDT	Enable	WDT Enable
	Disable	WDT Disable
P71 Port	RESET	P71 as external RESET
	GPIO	P71 as GPIO
External interrupt filtering (NR)	Disable	External interrupt filtering disable
	8Fosc	Filter time 8Fosc
	32Fosc	Filter time 32Fosc
LVR	1.8V	LVR select 1.8V
	2.7V	LVR select 2.7V
	3.5V	LVR select 3.5V
	4V	LVR select 4V
System clock warm up	8 Fosc	System clock warm-up time selection 8Fosc
	32 Fosc	System clock warm-up time selection 32Fosc
Reset time	4.5ms	System setup time select 4.5ms
	18ms	System setup time select 18ms
Package pin	20PIN	Package select 20PIN
	16PIN/18PIN	Package select 16/18PIN(Unused pins must be set to output low)
	14PIN	Package select 14PIN
	10PIN	Package select 10PIN
	8PIN	Package select 8PIN
Oscillation mode	IRC mode	Oscillation mode select internal RC oscillation
	ERC mode	Oscillation mode select external RC oscillation
	LXT1 mode	External crystal frequency select 100K～1M
	LXT2 mode	External crystal frequency select 32.768K
	HXT1 mode	External crystal frequency select 12M～16M
	HXT2 mode	External crystal frequency select 6M～12M
	XT mode	External crystal frequency select 1M～6M
P70 Port	GPIO	P70 as GPIO
	RCOUT	P70 as the instruction cycle output, open drain output forbidding
	RCOUT_OD	P70 as the instruction cycle output, open drain output enable
IRC frequency	1M	RC select 1M
	4M	RC select 4M
	8M	RC select 8M
	16M	RC select 16M

Clocks division	2Clocks	Instruction cycle select 2Clocks
	4Clocks	Instruction cycle select 4Clocks
	8Clocks	Instruction cycle select 8Clocks
	16Clocks	Instruction cycle select 16Clocks
Fs clock selection	128KHz	Fs select 128KHz
	16KHz	Fs select 16KHz
P71 Port pull up	Disable	Disable P71 port pull up
	Enable	Enable P71 port pull up
Power selection	High speed and high power consumption	Fcpu>=2M selecting (Fcpu = oscillator frequency / clocks division)
	Normal	Fcpu< 2M selecting (Fcpu = oscillator frequency / clocks division)
The ADC sampling value is forcibly raised by 14 least significant bits	ban	The 14 least significant bits cannot be increased
	Can make	Enable to raise the 14 least significant bits (Applicable only when the AD port sampling is less than 5mV).
System clock filtering	Disable	Prohibited (must be prohibited when the oscillator clock frequency is 8M or 16M)
	Enable	The system clock filtering function is enabled
OS Testing	Disable	OS test forbidden (only for board burning)
	Enable	OS test enable (chip is placed on burner to burn)

5 Electrical Characteristics

5.1 IC Limiting Characteristics

Temperature under bias (℃):	(√) E:-40-85;
Storage temperature (℃):	(√) -65～+150
Limit voltage (V)	(√) -0.3～6
Input voltage (V)	(√) GND-0.3～VDD+0.5;
Output voltage (V)	(√) GND-0.3～VDD+0.5;

5.2 DC Electrical Characteristics

(T=25℃, VDD=5V,GND=0V)

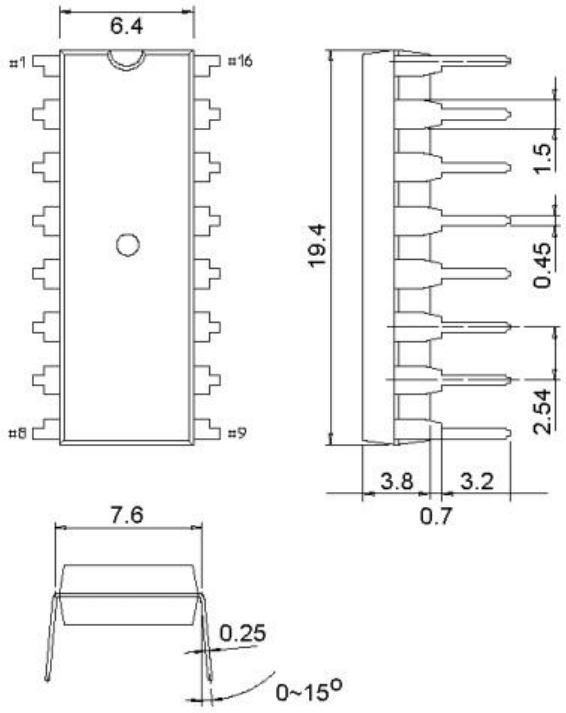
Symbol	Parameter	Condition	Min	Typ	Max	Unit
ERC	ERC: VDD to 5V	R:5.1KΩ, C:100pf	0.76	0.95	1.14	MHz
IRC1	Built-in RC oscillator 1	Firc0:Firc1=1:1		4		MHz
IRC2	Built-in RC oscillator 2	Firc0:Firc1=1:0		16		MHz
IRC3	Built-in RC oscillator 3	Firc0:Firc1=0:1		8		MHz
IRC4	Built-in RC oscillator 4	Firc0:Firc1=0:0		1		MHz
VIH1	Input high	P5, P6, P70	0.6*VDD		VDD	V
VIL1	Input low	P5, P5, P70	-0.3V		0.4*VDD	V
IOH1	Output high drive (Except P71)	IOH=VDD-0.6V	3.5	4.5	5	mA
IOH2	Output high drive enhancement (P71)	IOH=VDD-0.6V	8	10	12	mA
IOL1	IO output low level drive	IOL=GND+0.6V	16	20	23	mA
IOL2	IO output low-level drive enhancement	IOL= GND+0.6V	40	45	47	mA
RPH1	Pull-up resistor (@3v)		125	135	145	KΩ
RPH2	Pull-up resistor (@5v)		55	65	75	KΩ
RPL1	Pull-down resistor (@3v)		210	220	230	KΩ
RPL2	Pull-down resistor (@5v)		110	120	135	KΩ
Isb1	Sleep current 1	All inputs are connected to VDD, the output is floating, WDT and LVD are disabled	0.5	1	2	μA
Isb2	Sleep current 2	All inputs are connected to VDD, the output is floating, WDT and LVD are disabled		10	12	μA

Isb3	Sleep current 3	All inputs are connected to VDD, the output is floating, WDT and LVD are disabled		5	6	μA
Iop1	Working current 1	4MHz，2clks，WDT、LVD、PWM、AD are disabled	0.8	1	1.2	mA
Iop2	Working current 2	4MHz，4clks，WDT、LVD、PWM、AD are disabled		0.8	1	mA
LVR	Low voltage reset voltage	Select Vlvr reset point	Vlvr-0.2	Vlvr	Vlvr+0.2	V
LVD	Low voltage detection voltage	Select detection point as Vlvd	Vlvd-0.2	Vlvd	Vlvd+0.2	V

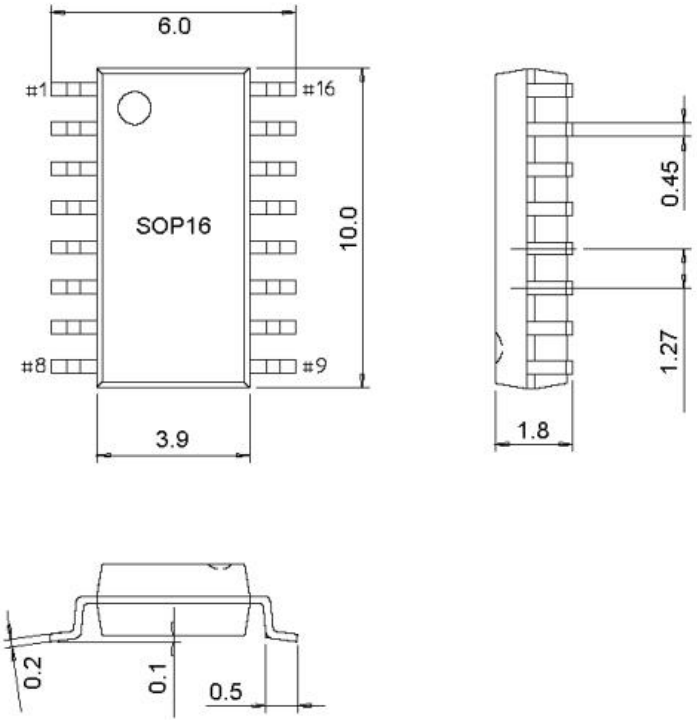
6 Packaging Configuration

6.1 16PIN Packaging

（Unit：mm）



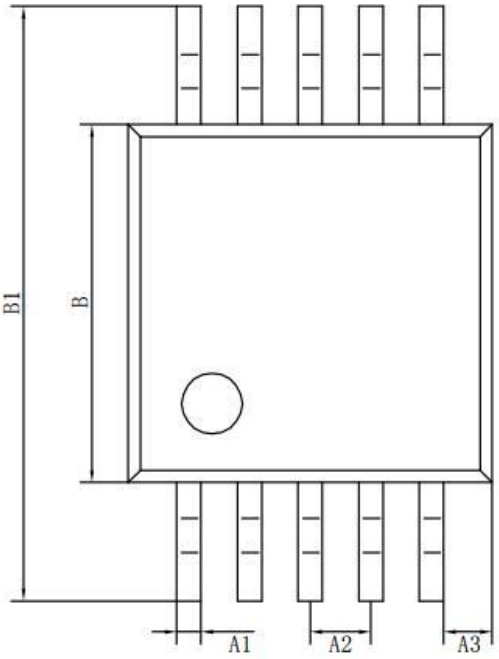
DIP16 Package size

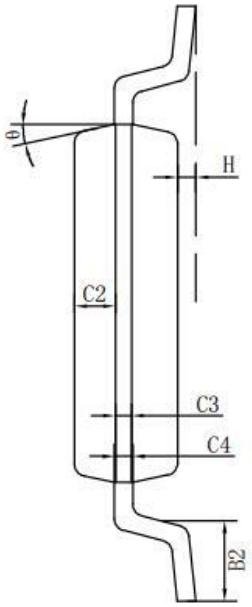


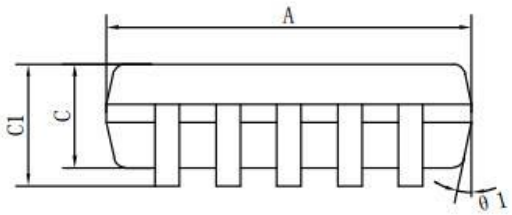
SOP16 Package size

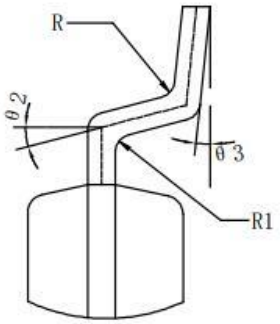
6.2 10PIN Packaging

（Unit：mm）



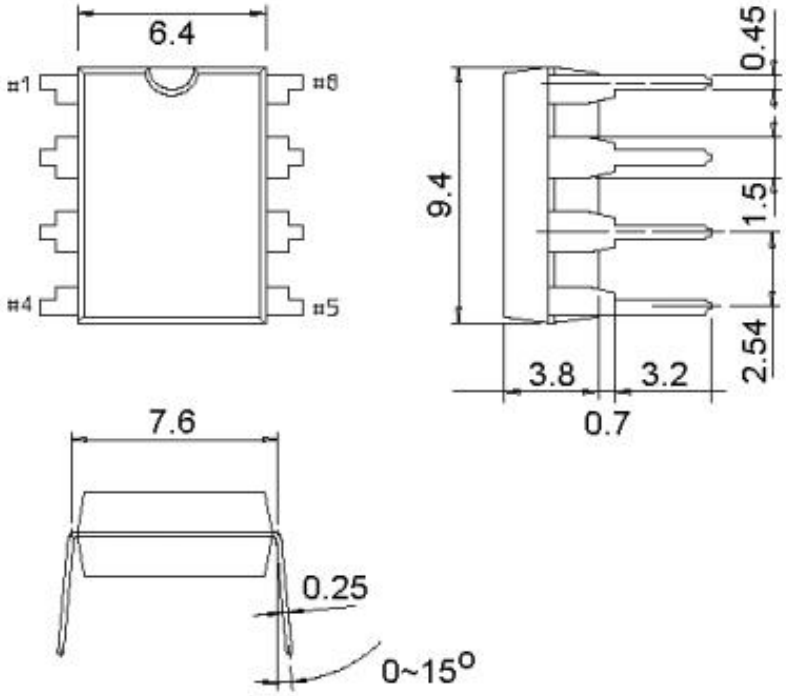




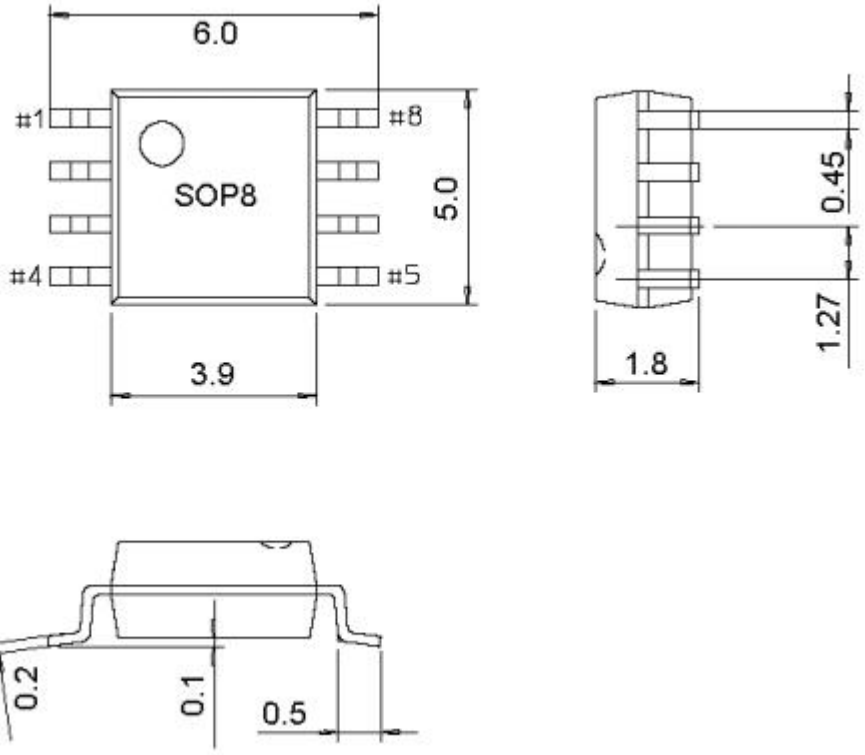


6.3 8PIN Packaging

（Unit：mm）



DIP8 Package size



SOP8 Package size

7 ESD performance description

Test Categor	Test Condition	Remarks
ESD(HBM)	>|±3KV| (TA=25℃)	IO TO IO (+) IO TO IO (-) All other pins to VCC (-) All other pins to VCC (+) All other pins to VSS (-) All other pins to VSS (+)
ESD(MM)	>|±500V| (TA=25℃)	
ESD(CDM)	>|±500V| (TA=25℃)	

*The test is based on ANSI-ESDA-JEDEC-JS-002-2018