JZ8P1530

8-BIT Microcontroller with OTP ROM

Product Specification

Version 1.0

Specification Revision History

Version	Revision Description	Remarks
V1.0	First draft version	

Notes:

1, When the TC0CON register bit.3 (PAB) predivision Bit and bit.2 ~ 0(TC0PSR2 ~ PSR0) division Bit are in the switching state。 you need to turn off the watchdog enable first, and then turn on the watchdog enable after the switching is completed, otherwise it is easy to cause reset.

2. When【IRC frequency 8M, system clock frequency doubling enabled】is forbidden, the instruction cycle selects 2Clocks to avoid chip operation errors.

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1 General Description

1.1 Functional Features

CPU configuration

- 1K×14-Bit OTP ROM
- 48×8-Bit SRAM
- 5 levels of stack space
- 8-level programmable Voltage Reset (LVR)
  1.2V, 1.6V, 1.8V, 2.6V
  2.8V, 3.6V, 4.0V, 4.3V
- Operating current less than 1.2mA (4MHz/5V)
- Operating current less than 10μ A (16KHz/5V)
- Sleep current less than 1 μA (sleep mode)

I/O configuration

- 1 set of bidirectional IO ports: P60 to P65
- Wake-up ports: P60 to P65
- Six programmable pull-up I/O pins
- 6 programmable pull-down I/O pins
- P63(reset pin) configurable pull-down and output
- External interrupt: P60

Working conditions

- Operating voltage range:
  $V_{LVR2.8\ V\sim5.5\ V}$ | Fcpu = 0 ~ 8 MHZ
  $V_{LVR2.6\ V\sim5.5\ V}$ | Fcpu = 0 ~ 4 MHZ
  $V_{LVR1.8\ V\sim5.5\ V}$ | Fcpu = 0 ~ 2 MHZ
- Operating temperature
  40 ℃ -- 85 ℃

Operating frequency range

- Built-in IHRC oscillation circuit:
  8MHz/1MHz/910KHz
- Built-in ILRC oscillation circuit:
  16 KHz (5V) / 15.5 KHz (3V)
- Instruction clock frequency division selection:2T, 4T, 8T, 16T, 32T

Peripheral modules

- P60 port level capture
- 8Bit real-time clock/counter
- 12Bit pulse width modulator PWM

Interrupt source

- TC0 overflow interrupt
- INT external interrupt
- Input change interrupt on port P6
- TC1/PWM cycle overflow interrupt
- CMP comparator result change interrupt

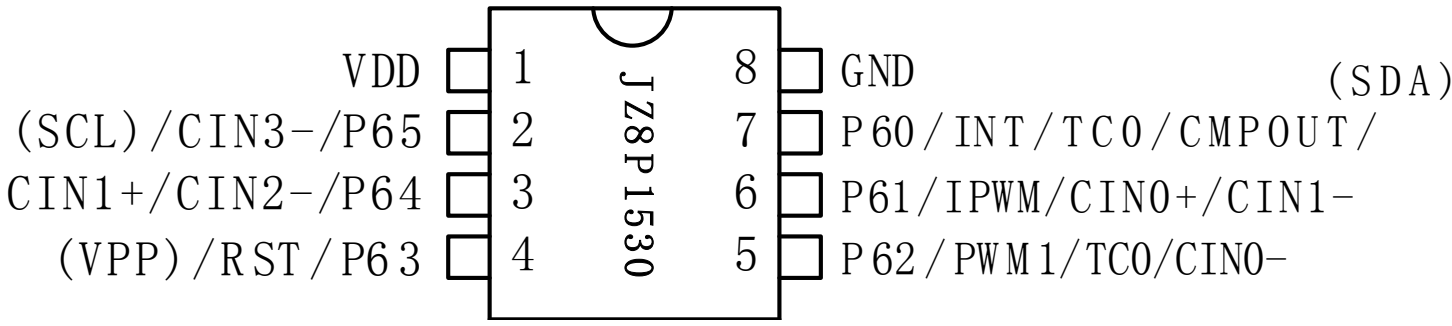
Features

- Programmable WDT timer
  4.5ms, 18ms, 72ms, 288ms
- Built-in BG is optional for the comparator

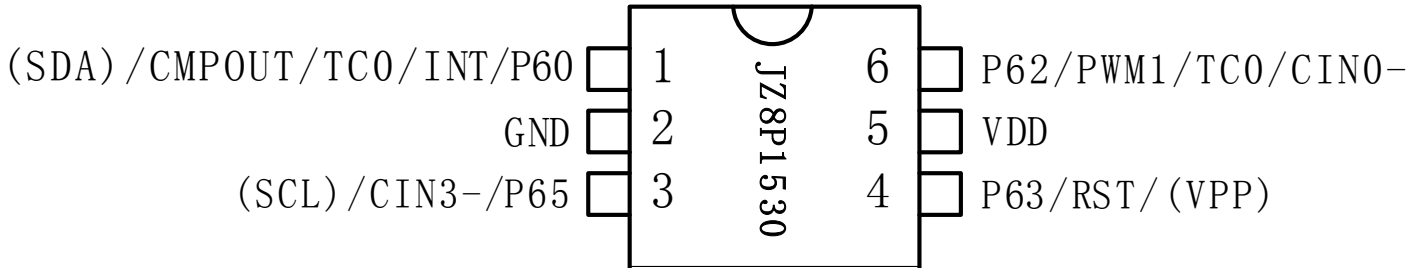
Package

- JZ8P1530-DIP8/SOP8
- JZ8P1530-SOT23-6

1.2 Pin assignment



JZ8P1530-8PIN MAP

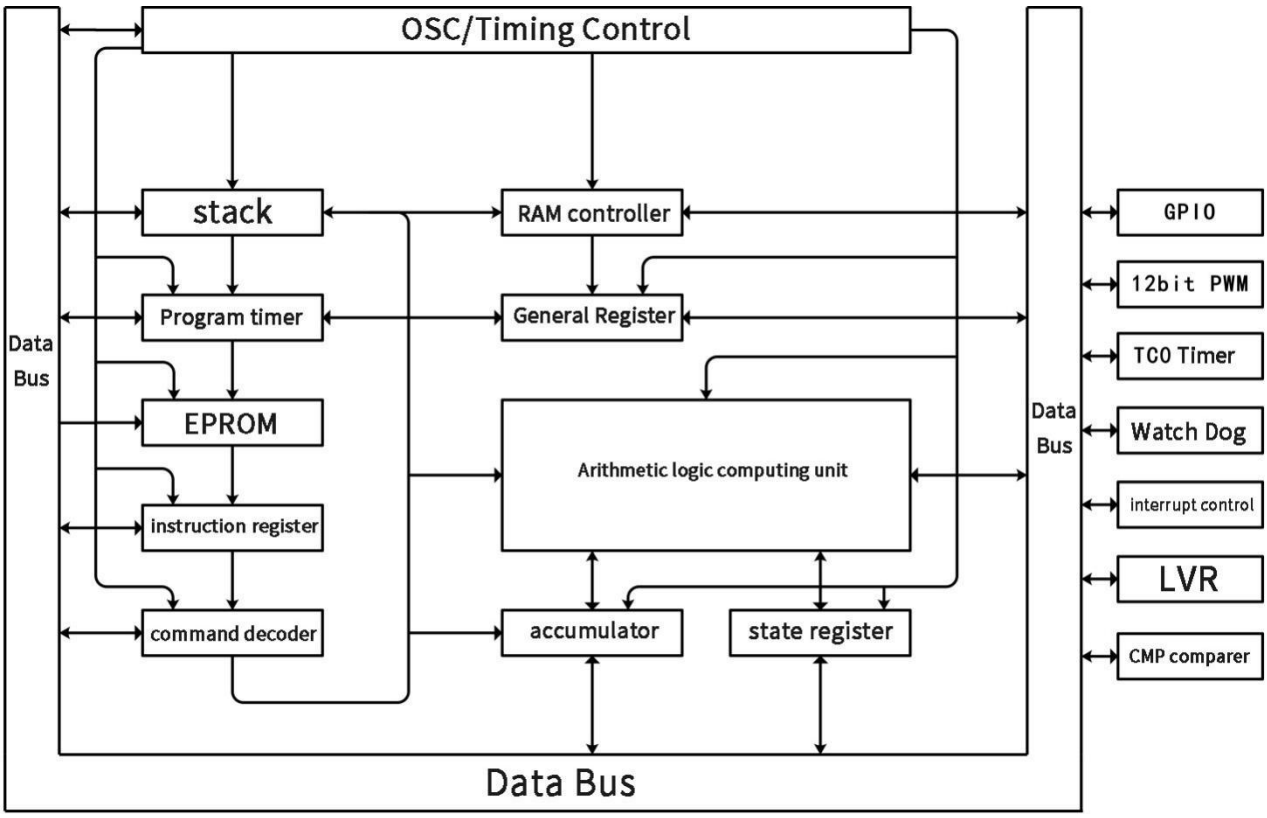


JZ8P1530-6PIN MAP

1.3 Pin description

NUM	NAME	I/O	Description
P60	P60	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	INT	I (SMT)	External interrupt input port
	TC0	I	TC0 external signal source input foot
	CMPOUT	O	Comparator result output port
	SDA	I (SMT)	Burn data port
P61	P61	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	IPWM	0	PWM complementary (negated) outlet
	CIN0+	I	Comparator positive input port
	CIN1-	I	Comparator negative input port
P62	P62	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	TC0	I	External TC0 signal source input foot
	PWM	0	PWM outlet
	CIN0-	I	Comparator negative input port
P63	P63	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	RST	I (SMT)	Reset pin
	VPP	I	Burn the high pressure port
P64	P64	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	CIN1+	I	Comparator positive input port
	CIN2-	I	Comparator negative input port
P65	P65	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	CIN3-	I	Comparator negative input port
	SCL	I (SMT)	Burn the clock port
	VDD	--	Power supply
	VSS	--	to

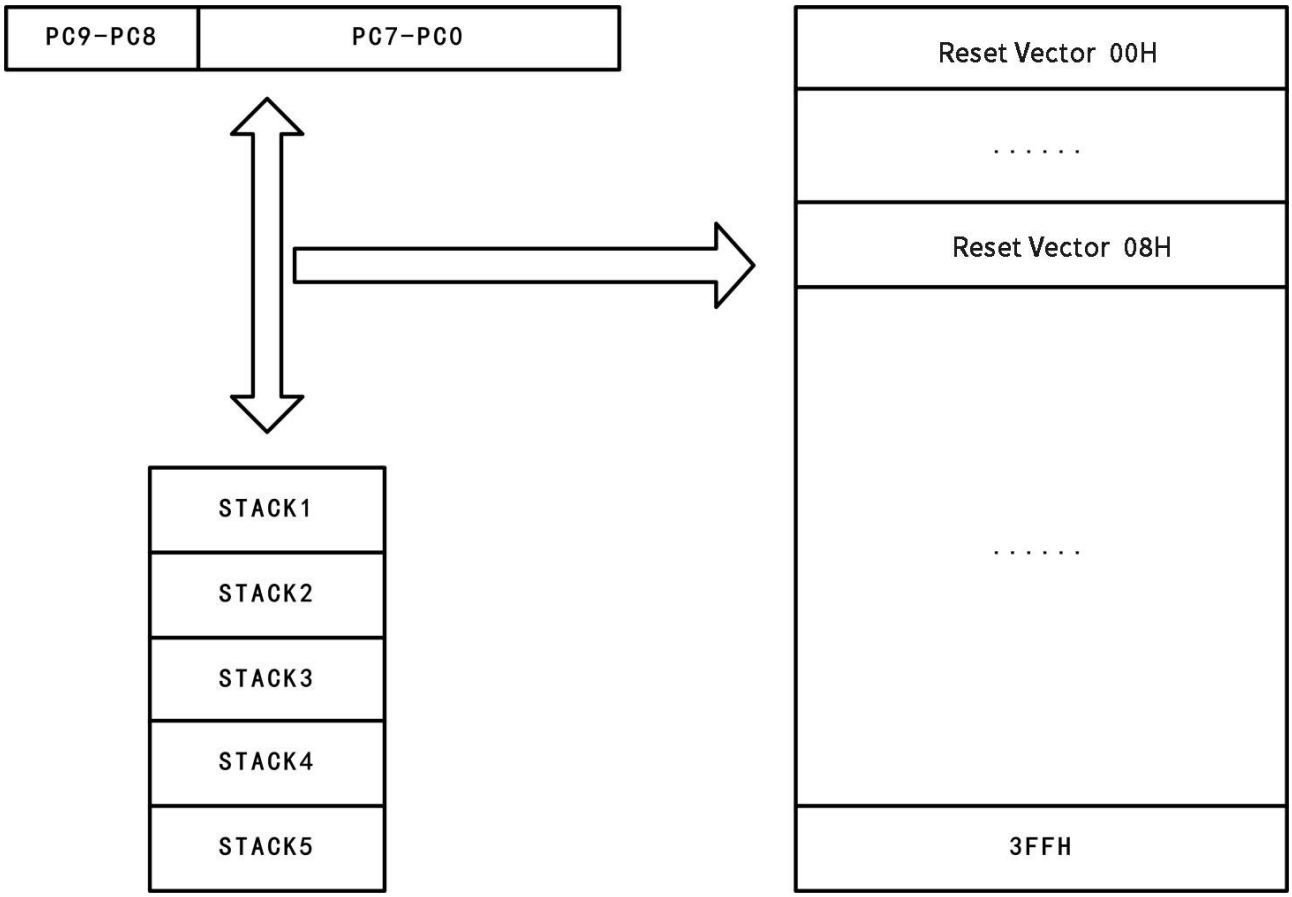
1.4 System block diagram



System circuit block diagram

2. Memory structure

2.1 Program storage area



Program store structure diagram

2.2 The data store

R page \IOC page register area (IOC pages are special pages and can only be read and written using IR/IW instructions)

Address	R page register	IOC page register
0x00	R0/IAR(Indirect addressing register)	Hold on
0x01	R1/TC0C(TC0 count register)	Keep
0x02	R2/PCL(program count low 8-bit register)	IOC2/TC0CON (TC0 control register)
0x03	R3/STATUS(status flag register)	Retain
0x04	R4/RSR(RAM select register)	Reserve
0x05	Reserved	Keep
0x06	R6/P6(P6 data register)	IOC6/P6CON(P6 control register)
0x07	R7/CMPCON0(CMP control register 0)	Keep
0x08	R8/TC1CON(TC1/PWM control register)	Keep
0x09	R9/TC1PRDL(TC1/PWM cycle low 8-bit register)	IOC9/TPRE (TC0/WDT predivider)
0x0A	RA/PWMDTL(PWM low duty cycle 8-bit register)	IOCA/CMPCON1 (CMP control register 1)
0x0B	RB/TC1PRDTH(TC1/PWM cycle high 4 bit and PWM duty cycle high 4 bit register)	IOCB/P6PD (P6 pull-down control register)
0x0C	RC/P6AE(P6 analog port control register)	Keep
0x0D	RD/P6IWE(Input state change interrupt enabled)	IOCD/P6PH (P6 pull-up control register)
0x0E	RE/CPUCON(CPU mode control register)	IOCE/WDTCON (WDT, external interrupt, TC0 capture control register)
0x0F	RF/INTF(interrupt flag register)	IOCF/INTE (Interrupt enable register)
0x10 ... 0x3F	General purpose register	Keep

3 Feature description

3.1 Operate registers

3.1.1 RPAGE ~ R0/IAR (Indirect addressing Register)

00H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAR	IAR<7:0>							
Read/write	R							
Reset values	X							

The indirection addressing register is not an actual register, its main function is to act as a pointer to indirection addressing. Any instruction that has R0 as a pointer actually corresponds to the address pointed to by RSR<5:0>, the lower 6 bits of R4 (RAM select register).

3.1.2 RPAGE ~ R1/TC0C(TC0 count register)

01H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0C(R)	TC0C<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

TC0 is an 8Bit uplink counter, clock source optional internal clock/external clock, count overflow can form interrupts, TC0C can be read and written.

If the PAB bit is cleared (TC0CON.3), there will be a predivider assigned to the TC0C, and when a value is written to the TC0C register, the value of the predivider will be cleared to zero.

If an external clock is selected, TC0 can trigger the edge by the TE bit (TC0CON.4) selection signal, which generates an increment operation when the clock edge arrives.

3.1.3 RPAGE ~ R2/PCL(Program Count Low 8-bit register)

02H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCL	PC<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

The program counter (PC) is a pointer used to record the instructions to be processed by the CPU in each instruction cycle. During the CPU run cycle, the PC pushes the instruction pointer into

the program memory, and the pointer is incremented by 1 to enter the next cycle. The JZ8P1530 has a 10-bit wide program counter (PC) whose low bytes come from the read-write PCL and high bytes (PC<9:8>) are unreadable.

The stack is the instruction pointer used to record the returns of the program. When a subprogram is called, the PC pushes the instruction pointer onto the stack. When the return instruction is to be executed, the stack sends the instruction pointer back to the PC to continue the original process. The JZ8P1530 has an 8-level stack, which occupies neither program storage nor data storage space, and the stack pointer cannot be read or written.

(1) The register PC and the built-in 8-level stack are 10 bits wide, used for 1K×14Bit ROM addressing, JZ8P1530 program memory area mapping.

(2) In general, the PC is incremented by one; When reset, all bits of PC are reset.

(3) Instruction "JMP" allows direct loading of the low 10 bit address, therefore, JMP instruction can achieve the current page (within the range of 1K) any position jump. Instruction "JMP" directly loads the low 10 bit address, and pushes PC +1 onto the stack, so that the subroutine entry address can be accurately located as long as it is in the same page.

(4) When executing "RET" instruction, the top data of the stack is sent to the PC.

(5) When setting the table lookup ability of PC to 1/4K (setting the table lookup range from 0 to 256 in the OPTION option), any instruction that directly modifies the content of PC will cause the 9th and 10th bit of PC to be reset. Therefore, the jump generated is limited to the first 256 addresses of the same page, and the instruction to change the content of the PC needs 2 instruction cycles.

When the lookup ability of PC is set to 1K, any instruction that rewrites the value of PC will affect the top two bits of PC accordingly. Therefore, the generated jumps can be expanded to the 1K range.When an interrupt occurs, the value of the program counter changes, and PC is assigned the value 0x08.

7. The stack works like a loop buffer, that is, after eight stack pushes, the data in the ninth push overwrites the data in the first push, the data in the tenth push overwrites the data in the second push, and so on.

3.1.4 RPAGE ~ R3/STATUS(status flag register)

03H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	RST	GIE	LVREN	T	P	Z	DC	C
Reading/Writing	R	R	R/W	R	R	R/W	R/W	R/W
Reset value	0	0	0	1	1	X	X	X

Bit<7> : Rst-reset type flag bit

0: Other reset type

1: If the sleep mode is awakened by changing the pin state

Bit<6> : GIe-Interrupt enable flag bit

0: Masked by DIT instruction or hardware interrupt

1: Interrupt enabled by EIT/RTI instruction

Bit<5> : LVREN-LVR software enabled

0: LVR enabled

1: LVR disabled (option only works when LVR disabled is selected)

Bit<4> : T- time overflow bit

0: WDT overflow

1: Perform "SLEEP" and "CWDT" commands or low voltage reset

Bit<3> : P- power down flag bit

0: Execute the "SLEEP" command

1: Power on reset or execute "CWDT" command

The events that affect T/P are listed in the table below:

Type	RST	T	P
Power-on reset	0	1	1
Press RESET in work mode	0	Keep	Keep
RESET Wake up	0	1	0
WDT overflows in working mode	0	0	Keep
WDT overflow wake up	0	0	0
Port state change wake up	1	1	0
Execute the CWDT command	Keep	1	1
Execute the SLEEP command	Keep	1	0

Bit<2> : z-zero flag bit set to "1" if the result of an arithmetic or logical operation is zero

0: When the result of an arithmetic or logical operation is not 0

1: When the result of an arithmetic or logical operation is 0

Bit<1> : DC- Auxiliary carry flag

0: When performing the addition, no carry is generated for the lower four bits; / when performing a subtraction operation, the lower four bits produce a borrow

1: When performing the addition operation, the lower four bits have carry generation; / When performing subtraction, no borrow is generated for the lower four bits

Bit<0> : C- Carry flag

0: When performing the addition, no carry is generated for the upper four bits; / when performing subtraction, the high four bits produce a borrow

1: When performing the addition operation, the higher four bits have carry generation; / When performing subtraction, no borrows are generated

3.1.5 RPAGE ~ R4/RSR(RAM select register)

04H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSR	-	-	RSR<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	X	X	X	X	X	X

RSR<5:0> Used to select RAM register address in indirect addressing mode (addressing range: 0X00 to 0X3F)

RSR is used to cooperate with IAR to realize indirect addressing operation. Users can put the address corresponding to a register into the RSR, and then read and write the general register data at the corresponding address of the RSR by accessing the indirect addressing register IAR.

3.1.6 RPAGE ~ R6/P6(P6 data register)

06H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6	-	-	P65	P64	P63	P62	P61	P60
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Port input/output register, P6 port is 6 bits

3.1.7 RPAGE ~ R7/CMPCON0(CMP control register 0)

07H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON0	CMPEN	CMPOUT	CMPRS<5:0>					
Read/write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : CMPEN -CMP enables the control bit

1: Enable

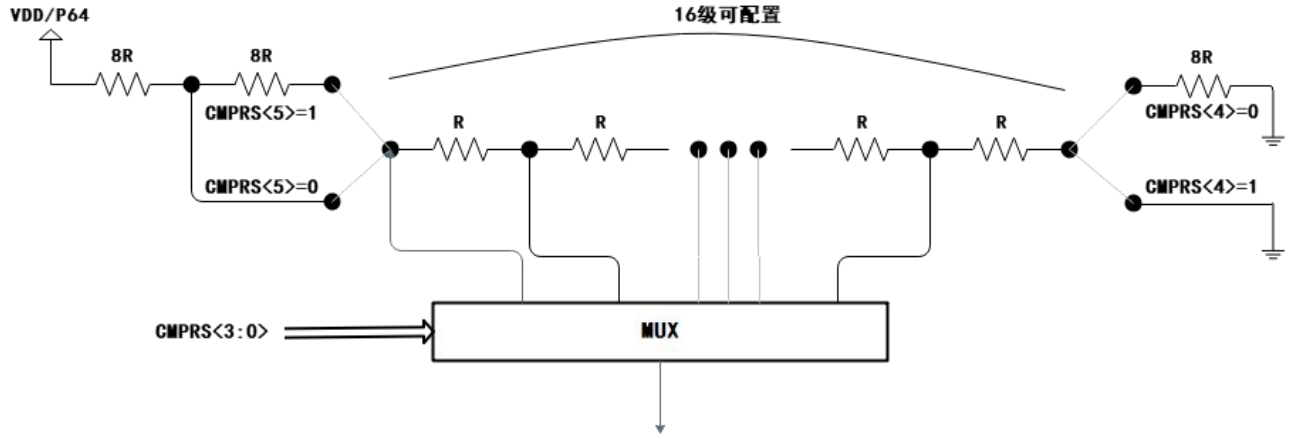
0: Forbid

Bit<6> : CMPOUT-CMP result output bit

1: The comparator positive voltage is greater than the negative voltage

0: The comparator positive voltage is less than the negative voltage

Bit<5:0> : CMPRS<5:0>- Comparator resistor voltage divider selection bit



When CMPCON1 register =0x85, comparator positive select resistance voltage divider, comparator negative select VBG, different resistance voltage division gear CMPRS<5:0> corresponding to different detection voltage, the specific table is as follows:

CMPRS	Detecting voltage	CMPRS	Detecting voltage	CMPRS	Detection voltage	CMPRS	Detecting voltage
00H	4.48 V	10H	30.24 V	20H	5.60 V	30H	40.32 V
01H	4.03 V	11H	15.12 V	21H	5.04 V	31H	20.16 V
02H	3.67 V	12H	10.08 V	22H	4.58 V	32H	13.44 V
03H	3.36 V	13H	7.56 V	23H	4.20 V	33H	10.08 V
04H	3.10 V	14H	6.05 V	24H	3.88 V	34H	8.06 V
05H	2.88 V	15H	5.04 V	25H	3.60 V	35H	6.72 V
06H	2.69 V	16H	4.32 V	26H	3.36 V	36H	5.76 V
07H	2.52 V	17H	3.78 V	27H	3.15 V	37H	5.04 V
08H	2.37 V	18H	3.36 V	28H	2.96 V	38H	4.48 V
09H	2.24 V	19H	3.02 V	29H	2.80 V	39H	4.03 V
0AH	2.12 V	1AH	2.75 V	2AH	2.65 V	3AH	3.67 V
0BH	2.02 V	1BH	2.52 V	2BH	2.52 V	3BH	3.36 V
0CH	1.92 V	1CH	2.33 V	2CH	2.40 V	3CH	3.10 V
0DH	1.83 V	1DH	2.16 V	2DH	2.29 V	3DH	2.88 V
0EH	1.75 V	1EH	2.02 V	2EH	2.19 V	3EH	2.69 V
0FH	1.68 V	1FH	1.89 V	2FH	2.10 V	3FH	2.52 V

Note: The gray part of the detection voltage is prohibited.

3.1.8 RPAGE ~ R8/TC1CON(TC1/PWM control register)

08H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	BZEN	IPWME	PWME	TC1PTEN	TC1PSR<2:0>		
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : TC1EN-TC1 /PWM counter enable control

1: Enable

0: Forbid

Bit<6> : BZEN-BUZZER output enable control bit

1: Enable BUZZER output function, TC1 overflow BUZZER flip (PWME=0)

0: Disable

Bit<5> : IPWME-IPWM enables the control bit

1: Enable PWM complementary output (PWM negation)

0: Disable

Bit<4> : PWME-PWM enable control bit

1: Enable PWM output (BZEN=0)

0: Disable

Bit<3:0> : TC1PTEN, TC1PSR2 ~ TC1PSR1 frequency division coefficient selection bit:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	Frequency division ratio
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.9 RPAGE ~ R9/TC1PRDL(TC1/PWM cycle low 8-bit registers)

09H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : TC1PRD<7:0>-TC1/PWM cycle low octet data

3.1.10 RPAGE ~ RA/PWMDTL(PWM duty cycle lower 8-bit register)

0AH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMDTL	PWMDT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWMDT <7:0>-PWM duty cycle lower eight bit data

3.1.11 RPAGE ~ RB/TC1PRDTH(TC1/PWM cycle high 4 bit and PWM duty cycle high 4 bit registers)

0BH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<11:8>				PWMDT<11:8>			
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:4> : TC1PRD<11:8>-TC1/PWM cycle high four bits of data

Bit<3:0> : PWMDT<11:8>- PWM duty cycle four data higher

3.1.12 RPAGE ~ RC/P6AE(P6 analog port enable register)

0CH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6AE	-	-	P6AE<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<5:0> : P6AE<5:0>-P6 analog port input enable control bit

1: P6x is set to analog input port

0: P6x is set to GPIO

3.1.13 RPAGE ~ RD/P6IWE(P6 input change interrupt, wake up enable register)

0DH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6IWE	-	-	P6IWE<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<5:0> : P6IWE<5:0>- P6 Input change interrupt, wake up enable control bit

1: Enable

0: Forbid

3.1.14 RPAGE ~ RE/CPUCON(CPU mode Control register)

0EH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	IPWM	TC1CKS	TC0CKS	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : IPWM-PWM, IPWM output data take the reverse selection bit

1: the output data of PWM(P62) and IPWM(P61) are inverted

0: PWM(P62) and IPWM(P61) output is normal

Bit<6> : TC1CKS-TC1/PWM clock source selection bit

1: TC1/PWM selects the system clock

0: TC1/PWM selects the instruction cycle clock

Bit<5> : TC0CKS-TC0 clock source selection bit

1: Select system clock/low speed clock (determined by TS)

0: Select instruction cycle clock/external input clock (determined by TS)

Bit<4> : TC1WE-TC1 wakeup enable bit

1: TC1/PWM wakeup enable to wake up idle mode

0: TC1/PWM wakeup disabled

Bit<3> : TC0WE-TC0 wakeup enable bit

1: Enable TC0 wakeup to wake up idle mode

0: Disable TC0 wakeup

Bit<2>：STPHX-High speed clock control bit

1: Stop the high-speed clock

0: The high-speed clock is working properly

Bit<1>：CLKMD-System clock selection bit

1: System clock using low speed RC oscillator clock

0: System clock using high speed IRC

When the system enters low speed mode from high speed mode, set CLKMD=1 first, then set STPHX=1;

When the system enters the high speed mode from low speed mode, set STPHX=0 first, and then set CLKMD=0.

Bit<0>：IDLE-Idle mode select bit

1: The system enters idle mode when it executes the SLEEP command, and the system clock works normally

TC0 and TC1 can continue to work in idle mode if the system clock is selected, and the system can be woked up.

0: The system enters SLEEP mode when the sleep command is executed

3.1.15 RPAGE ~ RF/INTF(Interrupt flag register)

0FH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF	-	-	-	CMPIF	TC1IF	INTIF	ICIF	TC0IF
Read/write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:5> : Unused

Bit<4> : CMPIF-CMPOUT status change interrupt flag

Bit<3> : TC1IF-TC1/PWM cycle interrupt flag

Bit<2> : INTIF- External port interrupt flag bit

Bit<1> : ICIF-P6 port input change interrupt flag bit

Bit<0> : TC0IF-TC0 interrupt flag bit

1: There is an interrupt, software clear 0

0: no interruption

INTF can be reset 0, but can not be reset 1.

Note: When clearing the interrupt flag bit, you must use MOV RF,A operation, not BTC AND AND RF,A instruction operation.

3.2 Control registers

3.2.1 IOPAGE ~ IOC2/TC0CON(TC0 control register)

02H(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CON	TC0EN	LRCEN	TS	TE	PAB	TC0PSR<2:0>		
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	1	1	1	1	1

Bit<7> : TC0EN-TC0 timer enable bit (clock source is system clock)

0: TC0 counter disabled

1: TC0 counter enabled

Bit<6> : LRCEN- LRCEN=1, enabling watchdog, and the system selecting low speed mode will enable ILRC

0: The internal low-speed RC oscillator is forbidden

1: Internal low speed RC oscillator enabled

Bit<5> : TS-TC0 signal source selection bit

0: Internal instruction cycle clock (TC0CKS=0)/system clock (TC0CKS=1)

1: External input clock (TC0CKS=0)/low speed oscillator clock (TC0CKS=1)

Bit<4> : TE-TC0 signal edge selection bit

0: TC0 pin signal changes from low to high plus 1

1: TC0 pin signal change from high to low add 1

Bit<3>： PAB-Pre-divider allocates bits

0: predivider is assigned to TC0

1: predivider is assigned to WDT

Bit<2:0> : TC0PSR<2:0>-TC0/WDT pre-divider selection control bit:

TC0PSR<2>	TC0PSR<1>	TC0PSR<0>	TC0 frequency division coefficient	WDT frequency division coefficient
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Note: When switching between PAB and TC0PSR<2:0>, the watchdog must be disabled first, and the watchdog can be enabled after the switch is completed.

3.2.2 IOPAGE ~ IOC6/P6CON(P6 control register)

06H(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6CON	-	-	P6CON<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P6 direction control bit

1: Define the corresponding I/O pin as the high resistance input state

0: Define the corresponding I/O as the output state

3.2.3 IOPAGE ~ IOC9/TPRE(TC0/WDT predivision read value register)

09H(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TPRE	TPRE<7:0>							
Read/write	R	R	R	R	R	R	R	R
Reset values	0	0	0	0	0	0	0	0

The TC0/WDT predivider does capture the low 8-bit counter when reading the count value

3.2.4 IOPAGE ~ IOCA/CMPCON1(CMP control register 1)

0AH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON1	CMPOE	CMPINV	CMPIS<5:0>					
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : CMPOE-comparator result output enable control bit

1: Enable, comparator result output from P60

0: Disabled, P60 as GPIO

Bit<6> : CMPINV- comparator result takes the reverse control bit

1: Take the inverse

0: No negation

Bit<5> : CMPIS<5>- divider resistor input voltage source select bit

1: P64 port input

0: VDD voltage

Bit<4:3> : CMPIS<4:3>- Comparator positive input source selection

CMPIS<4>	CMPIS<3>	Positive input source
0	0	Resistance partial pressure
0	1	CIN0+/P61
1	0	CIN1+/P64

Bit<2:0> : CMPIS<2:0>- Comparator negative input source selection

CMPIS<2>	CMPIS<1>	CMPIS<0>	Negative input source
0	0	0	CIN0-/P62
0	0	1	CIN1-/P61
0	1	0	CIN2-/P64
0	1	1	CIN3-/P65
1	0	0	Resistance partial pressure
1	0	1	VBG (Bandgap voltage 1.26V)

3.2.5 IOPAGE ~ IOCB/P6PD(P6 pull-down control register)

0BH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PD	-	-	P6PD<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit<7:6> : Undefined, fixed to 1

Bit<5:0> : P65 ~ P60 pull-down enable control

0: Enable

1: Forbid

3.2.6 IOPAGE ~ IOCD/P6PH(P6 pull-up control register)

0DH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PH	-	-	P6PH<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit<7:6> : Undefined, fixed to 1

Bit<5:0> : P65 to P60 pull-up enable control

0: Enable

1: Forbid

3.2.7 IOPAGE ~ IOCE/WDTCON(WDT, external interrupt, TC0 capture control register)

0EH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	CMPWE	INTWE	TC0GATE<2:0>			INTEDG<1:0>	
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	0	0	0	0	0

Bit<7>：WDTE-WDTEnable control

1: Enable

0: Forbid

Note: Watchdog enable requires WDTEN enable and OPTION option [Watchdog] select [Enable].

Bit<6>：CMPWE-Comparator state change Wake up enable control bit

1: CMP state change wakeup enable

0: CMP state change wakeup disabled

Bit<5>：INTWE-External interrupt wake up enable control bit（Need to set INTEDG0=1 or INTEDG1=1）

1: External interrupt wakeup enable

0: External interrupt wakeup disabled

Bit<4>：TC0GATE<2>-TC0Count gating Enable control2

1: TC0 count is controlled by CMPOUT, which counts TC0 when CMPOUT=1

0: CMP gating is forbidden

Bit<3>：TC0GATE<1>-TC0 计 Count gating Enable control1

1: The TC0 count is controlled by P60, which is low when INTEDG1=1 and high when INTEDG0=1

0: P60 gating is forbidden

Bit<2>：TC0GATE<0>-TC0Count gating Enable control0

1: TC0 external count enable (P62 as external count port)

0: TC0 external count is disabled

Bit<1>：INTEDG<1>-External interrupt rising edge triggered(TC0Low level capture count by TC0GATE<1>enable signal)

1: External interrupt rising edge trigger enabled

0: External interrupt rising edge trigger disable

Bit<0>: INTEDG<0>- External interrupt falling edge trigger (TC0 high level capture count is enabled by TC0GATE<1>)

1: External interrupt falling edge trigger enable

0: External interrupt falling edge trigger Disable

3.2.8 IOPAGF ~ IOCF/INTE(interrupt enable register)

0FH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE	-	-	-	CMPIE	TC1IE	INTIE	ICIE	TC0IE
Read/write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:5> : Unused

Bit<4>：CMPIE-Comparator state change interrupts enable control bit

1: Enable

0: Forbid

Bit<3> : TC1IE-TC1/PWM cycle interrupt enable control bit

1: Enable

0: Forbid

Bit<2>：INTIE-External interrupt enable control bit

1: Enable

0: Forbidden

Bit<1>：ICIE-Port status change Interrupt enable control bit

1: Enable

0: Forbid

Bit<0> : TC0IE-TC0 overflow interrupt enables control bits

1: Enable

0: Forbid

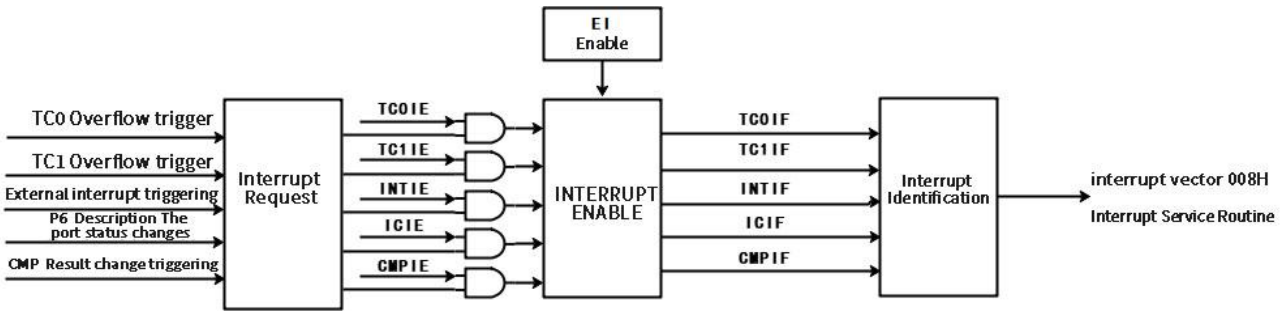
Note: It is no longer necessary to set ICIE=1 for external port wakeup

3.3 Interrupts

The JZ8P1530 has five interrupt sources, whichever interrupt is used, the total interrupt must be enabled, that is, the "EI" instruction. The interrupt vector is the fixed default address 008H. The following are the characteristics of each interrupt:

Interrupt Type	Interrupt source	Enabling condition	Interrupt flag
Exterior	External interruption	EI + INTIE=1	INTIF
Outside	Port input change interrupt	EI + ICIE=1	ICIF
Inside	TC0 overflow interrupt	EI + TC0IE=1	TC0IF
Inside	TC1 cycle overflow interruption	EI + TC1IE=1	TC1IF
Inside	CMP result change interrupted	EI + CMPIE=1	CMPIF

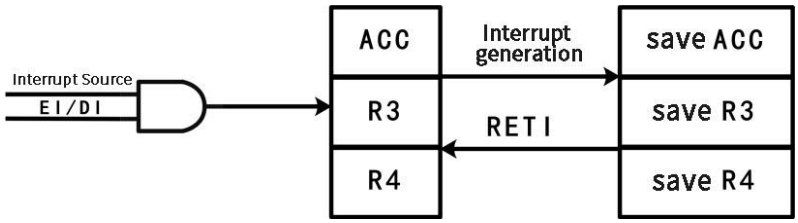
The RF of RPAGE is the interrupt status flag register, which records the interrupt flag bit after an interrupt request is generated. IOCF is the interrupt enable register. The allow and disable interrupt are set in these two registers. The total interrupt is allowed by the "EI" instruction, on the contrary, the total interrupt is forbidden by the "DI" instruction. When an interrupt is generated, the execution of its next instruction will be performed from the interrupt vector address 008H. The corresponding interrupt flag must be reset before leaving the interrupt service routine, so that the wrong action of the interrupt can be avoided.



Schematic diagram of interrupt principle

3.3.1 Interrupt site protection

In the process of responding to interrupts, it is strongly recommended to use interrupt protection in the program. The contents of ACC, R3, and R4 are saved until the interrupt subroutine is left, and the saved values are reloaded into ACC, R3, and R4. This is to avoid instructions to change the values of ACC, R3, and R4 when executing the interrupt subroutine. Cause an error when returning to the main program. As shown in the following image:



Schematic diagram of software interrupt site protection

3.4 Reset

3.4.1 Overview of reset function

The JZ8P1530 system provides four reset methods:

- POR Power on reset
- RESET foot input low reset
- WDT Watchdog overflow reset
- LVR low voltage reset

When any of the above reset occurs, all system registers are initialized to the reset value, the program stops running, and the program counter PC is reset. After the reset, the system starts running again from the vector 0000H.

Any reset situation requires a certain response time, and the system reset mechanism can ensure a reliable reset of the MCU. Different types of oscillators require different time to complete reset. Therefore, the rising rate of VDD and the starting time of different oscillators are not fixed. The RC oscillator has the shortest onset time, while the crystal oscillator has a longer onset time. In the process of using the user terminal, attention should be paid to the requirements of the application scene for power on and reset time.

3.4.2 WDT watchdog reset

The watchdog reset is a protective setting for the system. In the normal state, the watchdog timer is reset by the program. If an error occurs, the system is in an unknown state, the watchdog timer overflows, and the system is reset. After the watchdog is reset, the system is restarted into a normal state.

- Watchdog timer state: The system detects whether the watchdog timer is overflowing, if it is overflowing, the system is reset;
- System initialization: all system registers are set to their initial default values;
- Oscillator starts to work: the oscillator starts to provide the system clock;
- Execute the program: the power on ends, and the program starts to run;

Watch dog timer application notes:

- Check the state of the I/O port and the contents of the RAM before the watchdog is reset to enhance the reliability of the program;
- Do not reset the watchdog in an interrupt, otherwise the main program running cannot be detected;
- The program should only clear the watchdog once in the main program. This structure can maximize the protection function of the watchdog.

3.4.3 POR Power-on reset

Power on reset is closely related to LVR operation. The power-on process of the system is in the form of a gradually rising curve, and it takes a certain time to reach the normal level value.

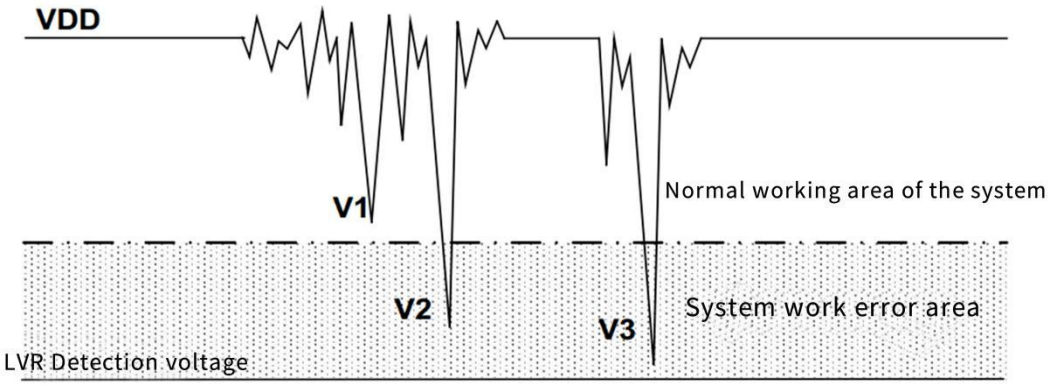
- Power on: the system detects the rise of the power supply voltage and waits for it to stabilize;
- External reset (limited to external reset pin enabled state) : The system detects the external reset pin state. If it is not high, the system remains reset until the external reset pin is released;
- System initialization: all system registers are set to their initial values;
- Oscillator starts working: the oscillator starts to supply the system clock;
- Execute the program: the power on ends, and the program starts to run;

The power-on reset time is determined by the [Reset Time] selection in the OPTION, as shown in the following table:

PWRT vs WDT	Reset setup time
PWRT=WDT	4.5ms(follow watchdog reset time)
PWRT=WDT	18ms(follow watchdog reset time)
PWRT=WDT	72ms(follow watchdog reset time)
PWRT=WDT	288ms(follow watchdog reset time)
PWRT≠WDT	140us(independent fixed reset time)

3.4.4 LVR low voltage reset

Power down reset is aimed at the system voltage sag caused by external factors (e.g., interference or external load changes). Power down may cause abnormal system working status or program execution errors.



The voltage sag may enter the system dead zone. System dead zone means that the power supply does not meet the minimum operating voltage requirements of the system. The figure above is a schematic of a typical power-down reset. In this picture, the VDD is severely disturbed and the voltage drop is very low. Above the dotted line, the system works normally. Below the dotted line, the system enters an unknown operating state. This region is called the dead zone. When VDD drops to V1, the system is still in a normal state; When VDD falls to V2 and V3, the system enters the dead zone, which is prone to errors. The system may enter the dead zone if:

DC in use:

Battery power supply is generally used in DC application. When the battery voltage is too low or the microcontroller drives the load, the system voltage may drop and enter the dead zone. At this time, the power supply will not further drop to the LVR detection voltage, so the system remains in the dead zone.

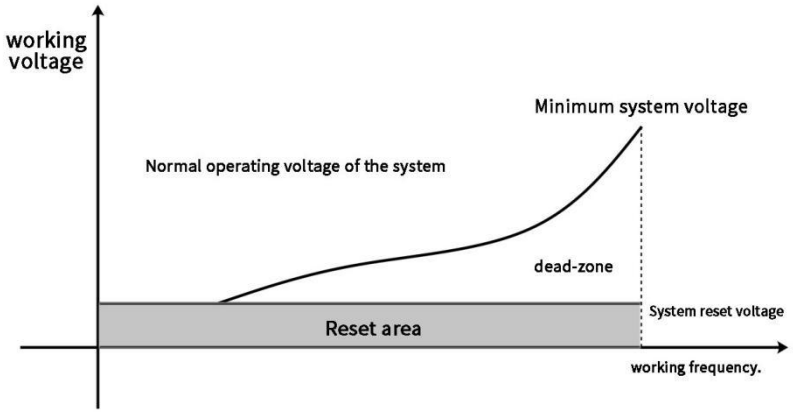
In AC operation:

When the system uses AC power supply, the DC voltage value is affected by the noise in the AC power supply. When the external load is too high, such as when driving the motor, the interference caused by the load action also affects the DC power supply. If the VDD falls below the

minimum operating voltage due to interference, the system will likely enter an unstable working state. In the AC application, the system power on and power off time are long. Among them, the power on timing protection makes the system power on normally, but the power down process is similar to the situation in the DC application. After the AC power is turned off, the VDD voltage is easy to enter the dead zone in the process of slow decline.

3.4.5 Relationship between working frequency and LVR low voltage detection

In order to improve the performance of the system power down reset, first of all, the minimum operating voltage value of the system must be clarified. The minimum operating voltage of the system is related to the execution speed of the system, and the minimum operating voltage value is different under different execution speed.



As shown in the figure above, the system normal operating voltage region is generally higher than the system reset voltage, and the reset voltage is determined by the low voltage detection (LVR) level. When the system execution speed increases, the minimum operating voltage of the system also increases accordingly. However, since the system reset voltage is fixed, there will be a voltage region between the minimum operating voltage of the system and the system reset voltage. The system will not work properly and will not reset, and this region is called dead zone.

To avoid voltage dead zone, in choosing a working frequency, to select the corresponding points as reset voltage. The following table:

IRC Frequency	Frequency doubling of the system clock	Clocks frequency division	LVR reset voltage point
IRC-8MHz	Frequency doubling	2 Clocks	As = 2.7 V
IRC-8MHz	Not octave	2 Clocks	As = 2.4 V

IRC-1MHz	Frequency doubling	2 Clocks	As = 1.8 V
IRC-1MHz	Not octave	2 Clocks	As = 1.8 V

Note: 1, working frequency = instruction cycle frequency =IRC frequency + Clocks frequency; 2, this working frequency and the corresponding value of the LVR reset voltage point, only recommended value, the user in the use of the process, according to the specific application can be adjusted reset voltage point.

3.5 Working mode

The JZ8P1530 can operate at different clock frequencies in four operating modes, which can control the operation of the oscillator, the execution of the program, and the functional loss of the analog circuit.

- High speed mode: the system clock selects high speed IRC clock;
- Low speed mode: system clock select internal low speed clock;
- Idle mode: the system clock works normally, and other parts go to sleep (TC0 and TC1 select the system clock to continue to work and wake up the system, and the port state changes to wake up the system);
- Sleep mode: all functions stop working, the system goes to sleep, port state change wake-up, WDT overflow wake-up, external reset pin input wake-up;

Function module	High speed mode	Low Speed mode	Idle mode	Sleep mode
IHRC	Run	STPHX control	STPHX controls	Stop
ILRC	Run	Run	Run	Stop
CPU instructions	Execution	Execution	Stop	Stop
TC0	Working	Workable	Workable	Stop
TC1	Workable	Workable	Workable	Stop
Internal interruption	All valid	All valid	TC0,TC1 valid	Invalid
External interruption	Valid	Effective	Effective	Effective
Wakeup function	-	-	P6IWE,TC0,TC1 INTWE,CMPWE	P6IWE,INTWE,CMPWE TC0(choose external clock)
A watchdog timer	WDT option controls	WDT Option control	WDT Option control	WDT Option control

3.5.1 High Speed mode

High-speed mode is the system high-speed clock operation mode, and the system clock source is provided by the high-speed RC oscillator. The program is executed. After a power-on reset or either reset is triggered, the system goes into high speed mode to execute the program. When the

system is awakened from sleep mode, it enters high speed mode. In high speed mode, the high speed oscillator works normally and consumes the most power.

- The program is executed and all functions can be controlled;
- The system rate is high;
- Both the high speed oscillator and the internal low speed oscillator work normally;
- Through the CPU mode control register, the system can switch from high-speed mode to any other mode.
- After waking up from sleep mode, the system can enter high-speed mode.
- Low speed mode can be switched to high speed mode;
- Enter from high-speed mode to idle mode, wake up and return to high-speed mode;

3.5.2 Low speed mode

Low speed mode is the system low speed clock operation mode. The system clock source is provided by the internal low speed RC oscillator. The low-speed mode is controlled by the CLKMD bit of the CPU mode control register. When CLKMD=0, the system is in high speed mode; When CLKMD=1, the system enters the low speed mode. After entering the low speed mode, the high speed oscillator cannot be automatically disabled and must be disabled by SPTHX bit to reduce power consumption.

- The program is executed and all functions can be controlled;
- The system rate is low;
- The internal low-speed RC oscillator works normally, and the high-speed oscillator is controlled by STPHX=1. In low speed mode, it is highly recommended to stop the high speed oscillator;
- Through the CPU mode control register, the low speed mode can be switched into other operating modes;
- From low speed mode to sleep mode, wake up and return to low speed mode;
- High speed mode can be switched to low speed mode;
- Enter from low speed mode to idle mode, wake up and return to low speed mode;

3.5.3 Idle mode

Idle mode is another ideal state. In sleep mode, all functions and hardware devices are disabled, but in idle mode, the system clock is kept working and the power consumption in idle mode is greater than that in sleep mode. In the idle mode, the program is not executed, but the timers TC0 and TC1 with wake-up function are still working normally, and the clock source of TC0 and TC1 is the system clock that is still working. In idle mode, there are five ways to wake up the system: 1, P6 port input change trigger; 2, TC0 wake up; 3, TC1 wake up; 4, external INT wake up; 5, CMP wake up. The user can set the timer or TC1 for a fixed period, and the system will wake up when overflow occurs. The CPU mode control register IDLE bit determines whether to enter IDLE mode. When IDLE=1, the system enters idle mode.

- The program stops executing and all functions are forbidden;
- The timer with wake-up function works.
- The oscillator as the system clock source works normally, and the working status of other oscillators depends on the configuration of the system operating mode;
- Enter from high speed mode to idle mode, return to high speed mode after waking up;
- Enter from low speed mode to idle mode, return to low speed mode after waking up;
- In idle mode, the wake-up mode was triggered by input change of P6 port, TC0 timer overflow and TC1 cycle overflow, external interrupt wake-up, and CMP wake-up.
- In idle mode, the functions of TC0 and TC1 are still valid.

3.5.4 Sleep mode

Sleep mode is the ideal state for the system, where the program is not executed and the oscillator stops working. The power consumption of the whole chip is below 1uA. Sleep mode can be triggered by P6 port input changes to wake up, TC0 (external clock), external interrupt INT, CMP result changes to wake up. Enter sleep mode from high speed mode or low speed mode, and return to the corresponding mode after being woken up. The IDLE bit in the CPU mode control register controls whether to enter sleep mode. When IDLE=0, the system enters sleep mode.

- The program stops executing and all functions are forbidden;
- All oscillators, including the external high speed oscillator, the internal high speed oscillator, and the internal low speed oscillator are stopped working;
- Power consumption below 1uA;

- Enter from high speed mode to sleep mode, and return to high speed mode after waking up;
- Enter into sleep mode from low speed mode, return to low speed mode after waking up; .
- The wake-up source of sleep mode is P6 port input change trigger, TC0 (external clock), external interrupt INT, CMP result change;

3.6 System clock

JZ8P1530 integrates three kinds of oscillators, which can be configured by OPTION. See the table below for details:

Oscillator type	Instructions
IRC (built-in RC oscillator)	910K/1M/8M can be selected via RCM

3.6.1 Internal RC oscillator

The JZ8P1530 provides an internal RC mode with a default frequency of 8MHz.

The internal RC oscillation mode contains three frequency values of 8MHz, 1MHz and 910KHz. The IRC operating frequency can be selected by setting the configuration bit of the OPTION. The following is their corresponding relationship:

Firc	IRC frequency
8 M	The IRC frequency is chosen to be 8MHz
1 M	The IRC frequency is chosen to be 1MHz
910K	The IRC frequency is chosen to be 910KHz

JZ8P1530 provides a variety of frequency division options, can be selected in the OPTION, suitable for more occasions. The following table:

Clocks	Clocks frequency division
2clock	Frequency division is 2clock
4clock	The frequency division is 4clock
8clock	The frequency division is 8clock
16clock	The frequency division is 16clock
32clock	Frequency division is 32clock

3.7 I/O port

JZ8P1530 has a set of bidirectional I/O ports, a total of 6 inputs, 6 outputs, most of the I/O can be reused for other functions.

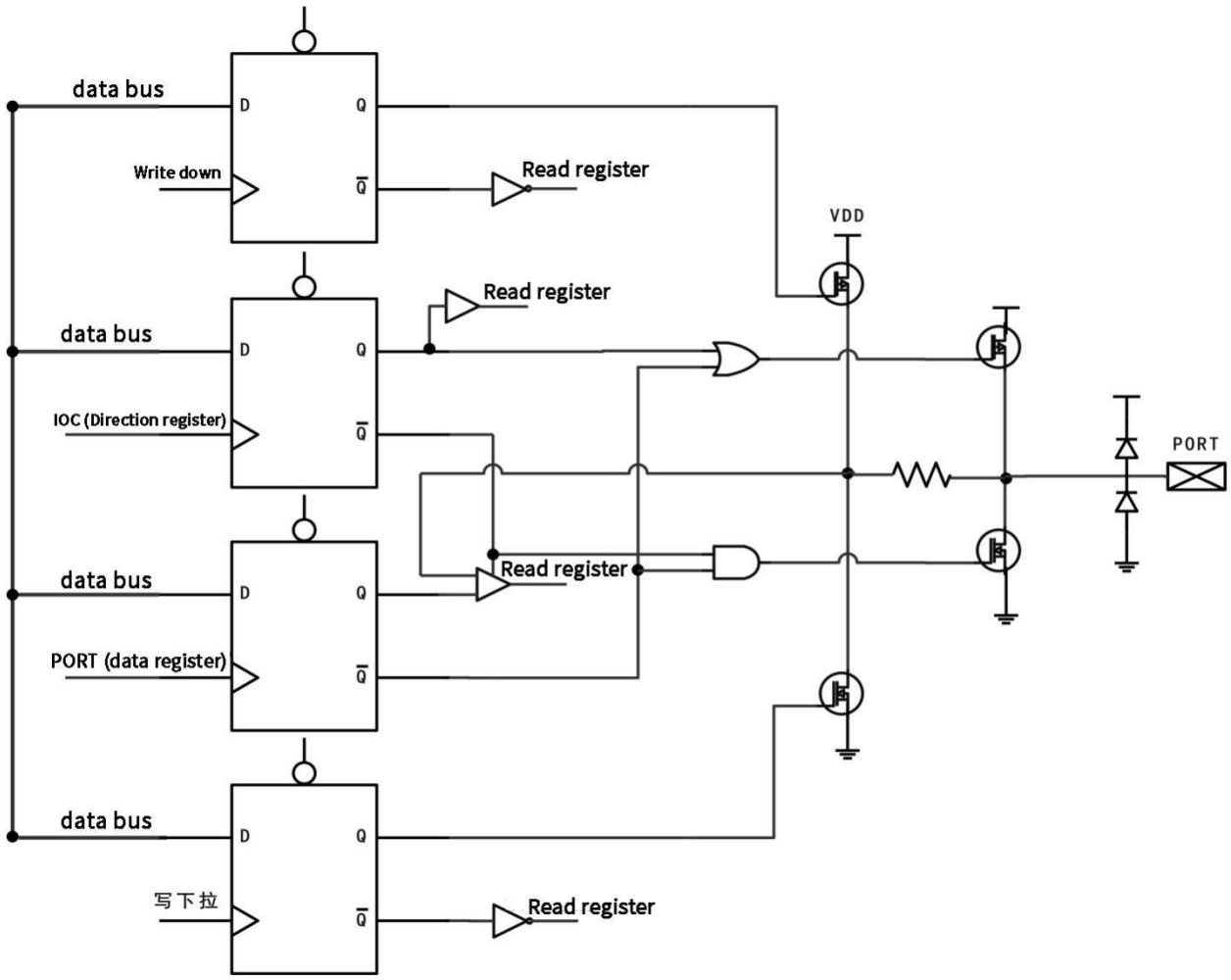
6 programmable pull-up I/O pins: P60 to P65;

6 programmable pull-down I/O pins: P60 to P65;

6 programmable port state change wake-up I/O pins: P60 ~ P65;

3.7.1 Internal structure diagram of GPIO

The following internal structure diagram is for reference only and does not represent the actual circuit.



IO control register/data register/pull-up/pull-down structure circuit

3.7.2 Port state change wake-up

The JZ8P1530 contains six programmable port state change wake-up I/ OS: P60 to P65. The chip can enter the SLEEP mode by executing the "sleep" command. At this time, the system clock stops, all modules stop working, WDT (if enabled) clear 0, but continue to run. Port state change wake-up can be selected by the program to continue the original process (execute DI before SLEEP) or execute the corresponding jump (execute EI before SLEEP), and open the corresponding enable control bit, jump to the interrupt subroutine.

Port input change query mode wake up Settings

1. The wake-up port of port P6 is set as input;

2. The internal pull up or pull down of the wake up port can be selected according to the need;

Enable P6 port input change interrupt;

4, enable port input change independent interrupt and wake-up control;

Execute DI instruction, do not enter the interrupt address port;

Execute the "SLEEP" command to enter the SLEEP mode;

7. After waking up, execute the next command of SLEEP;

Port input changes interrupt mode wake up Settings

1. The wake-up port of port P6 is set as input;

2. The internal pull up and down of the wake-up port can be selected according to the need;

3, enable port input change independent interrupt and wake-up control;

4, enable P6 port input change interrupt;

Execute "EI" instruction and wait to enter the interrupt address port;

6. Under the command "SLEEP", enter the SLEEP mode;

7. After waking up, it will enter the interrupt address port, exit the interrupt, and execute the next instruction of SLEEP;

3.7.3 Port Schmidt parameter

The Schmidt characteristics of the JZ8P1530 port are shown in the following table (for reference only) :

Ports	SMT
P6.3	0.51 * VDD
P6.0 ~ P6.2	VDD / 0.26 * 0.53 * VDD
P6.4 ~ P6.5	VDD / 0.26 * 0.53 * VDD

The above parameters are for reference only, please refer to the measured data of the target prototype.

3.8 Timing counter

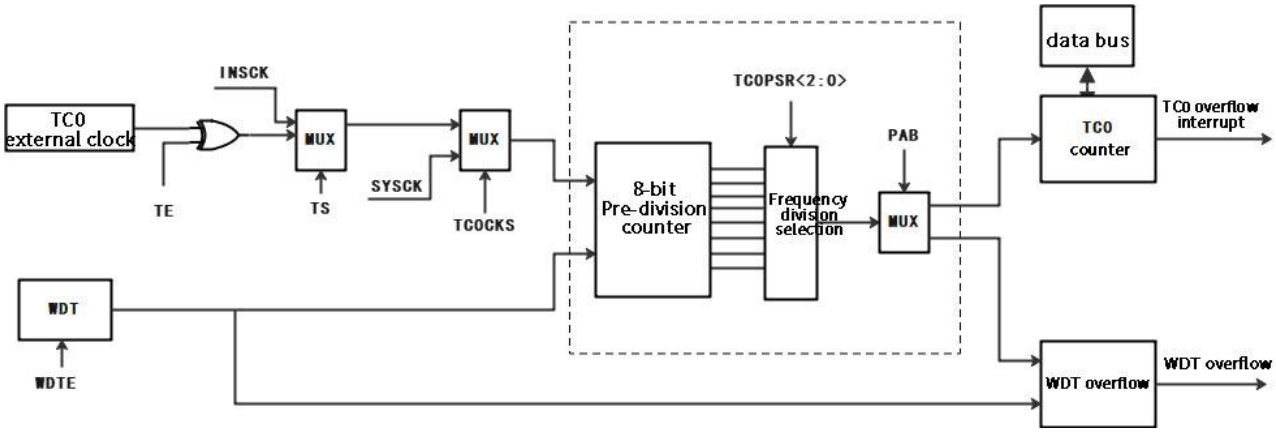
3.8.1 TC0 timing counter

The JZ8P1530 provides an 8-bit counter as a pre-divider for TC0 and WDT. The predivider can be used only for TC0 or only for WDT at the same time, and the PAB bit in the TC0CON register determines the allocation of the predivider. TC0PSR0 ~ PSR2 three bits determine the pre-division ratio. In TC0 mode, every time TC0 is written a value, the pre-division register is reset. When the predivider is assigned to WDT mode, the values of the WDT and predivider registers are reset when the "CWDT" or "SLEEP" instruction is executed. If the predivider is assigned to TC0 and then to WDT, the contents of the predivider counter will be automatically cleared, and vice versa.

TC0C(R1) is an 8Bit uplink counter that works whenever there is a clock. The clock source can be either an internal system clock (triggered by the rising edge) or optionally an external clock (entered by the TC0 pin, the triggering edge is optional), and if there is no frequency division control, each clock rising edge counter is implemented incremented by 1. System to provide a 8 bit counter as TC0 preassigned frequency. The TC0 predivider, trigger edge, clock, etc. can be set through the TCOCON register.

A TC0 count overflow can form an interrupt signal.

In the IDLE mode, the TC0 interrupt can wake up the circuit, after waking up, you can choose to interrupt or continue to execute the original program, the method refers to the port state change to wake up.



TC0/WDT structure block diagram

3.8.1.1 TC0 timing setup instructions

- Assign an initial value to the TC0C register;
- Set the value of the TCOCON register (choose as a timer or counter and predivision ratio);
- To use as a counter, you need to select the TC0 external signal in the TCOCON register to add 1 to the positive or negative edge;
- If you need to execute the interrupt function, you must set the TC0IE (Bit0) in the IOCF register to 1, and execute the EI instruction;
- The interrupt program part will manually save ACC, STATUS and R4 in the stack, after executing the RETI instruction, and then take it out from the stack. Before exiting the interrupt, the TC0 interrupt flag bit should be cleared.

3.8.1.2 TC0 timing calculation instructions

The TC0 timing function assigns the initial value to the timer by writing a value to the TC0C register, and the timer starts to accumulate from the initial value position until the timer overflows and interrupts.

TC0 timing time calculation formula (select internal instruction cycle clock) :

$$\text{TC0 timing time} = (\text{System clock frequency division/Fosc}) \times (\text{TC0 frequency division}) \times (256 - \text{TC0C initial value})$$

Example:

System clock division =2clock, Fosc=8 MHz, TC0 division selection =4 division, TC0C initial value =156;

$$\text{TC0 timing time} = (2/8) \times (4) \times (256 - 156) = 100\ \text{us}$$

TC0 timing time calculation formula (select external input clock) :

$$\text{TC0 timing time} = (\text{External clock})) \times (\text{TC0 frequency division}) \times (256 - \text{TC0 Cinitial value})$$

Example:

External input clock =1 MHz, TC0 divider selection =4 divider, TC0C initial value =156;

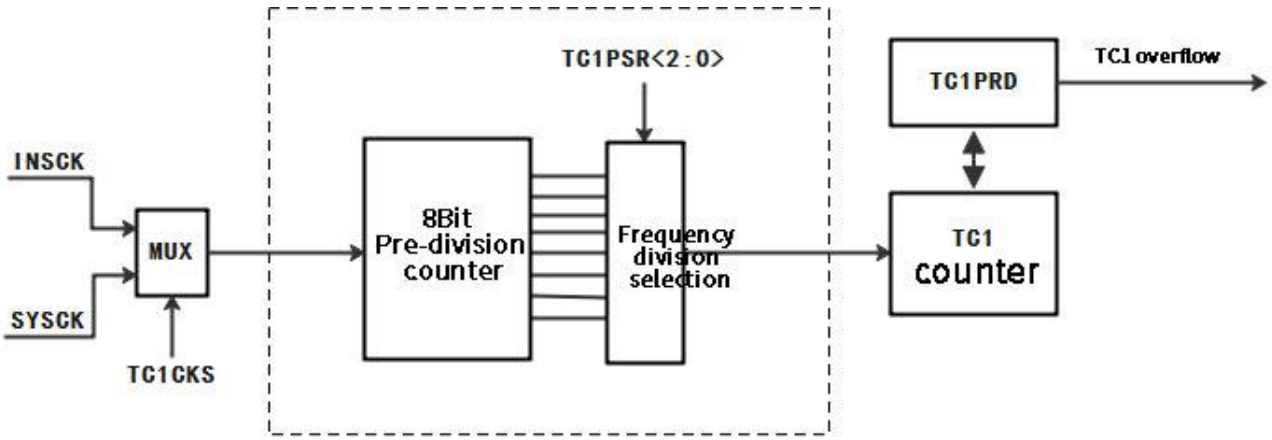
$$\text{TC0 timing time} = (1) \times (4) \times (256 - 156) = 400\ \text{us}$$

3.8.2 TC1 timing counter

The TC1 timing counter provides an 8-bit predivider, and the TC1PSR<2:0> three bits of the TC1CON register determine the predivider ratio. Each time TC1EN/BZEN/IPWME/PWME is enabled in TC1 mode, the TC1 timing counter and the predivision register are reset and reset.

TC1 is a 12Bit uplink counter. TC1 timers need to be TC1EN enabled to work. The clock source is the internal instruction clock/internal system clock, and the counter is incremented by 1 for each clock cycle. The TC1 count value is consistent with the TC1PRD register set value to produce overflow. If TC1IE and EI are enabled, the system jumps to the interrupt vector address, and the interrupt service program is executed.

In the IDLE mode, TC1 interrupt can wake up the circuit (clock needs to select the system clock), after waking up, you can choose to enter the interrupt or continue to execute the original program, the method refers to the port input to change the wake-up.



TC1 structure block diagram

3.8.2.1 TC1 timing calculation instructions

The TC1 timing function sets the counter overflow value by writing the value to the TC1PRDL and TC1PRDH registers, and the timer starts to accumulate from the initial value until the timer is consistent with the set count value, and the overflow is generated and the interrupt is triggered.

TC1 timing time calculation formula (select system clock) :

$$\text{TC1 timing time} = (1/\text{Fosc}) \times (\text{TC1frequency division}) \times (\text{TC1PRDH、TC1PRDL})$$

Example:

Fosc=1 MHz, TC1 divider selection =4 divider, TC1PRD=1000(TC1PRDH=0x03, TC1PRDL=0xE8);

$$\text{TC1 timing time} = (1/1) \times (4) \times (1000) = 250 \text{ us}$$

3.8.2.2 TC1 timing setting instructions

1. Set TC1PRDL and TC1PRDH registers and set the count value;

2. Set the TC1CON register and configure the pre-frequency ratio;

Enable TC1EN, open the TC1 timer count;

4. If you need to execute the interrupt, you must set the TC1IE (Bit0) in the IOCF register to 1, and execute the EI instruction;

5. ACC, STATUS and R4 need to be saved manually in the interrupt program, and data need to be restored before executing the RETI instruction;

3.9 PWM pulse width modulation

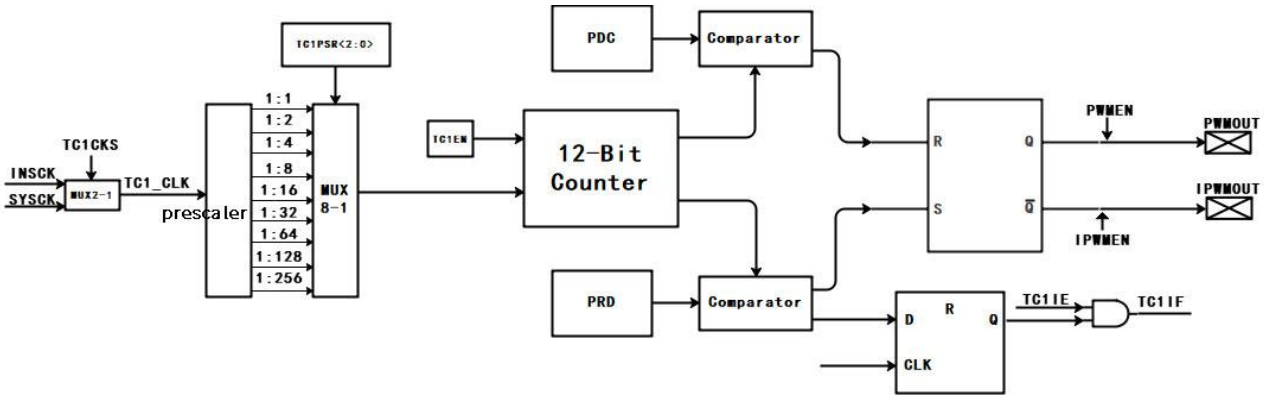
JZ8P1530 provides a 12 bit TC1 counter to generate PWM signal. The PWM output waveform is determined by the cycle and duty cycle, and the transmission rate is the reciprocal of the cycle.

TC1 has a periodic overflow interrupt, which can jump to interrupt when enabled.

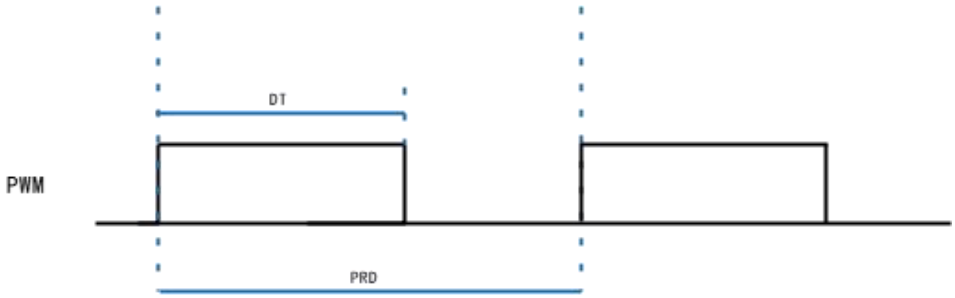
In IDLE mode, TC1 wakes up the system by selecting TC1CKS=1 in the TC1 control register and enabling TC1WE in the CPU control register.

3.9.1 PWM internal structure and timing

The following internal structure diagram is for reference only and does not represent the actual circuit.



PWM working structure circuit



PWM cycle timing instructions

3.9.2 PWM cycle and duty cycle

The PWM provides an 8bit counter as the clock divider and a 12bit counter (TC1 counter) as the baud rate clock generator for the PWM module. The TC1EN in the register can be controlled by

enabling TC1 to enable the function of PWM counter. The pre-frequency setting of TC1 counter can be carried out by TC1PTEN and TC1PSR<2:0> control bits.

The PWM cycle writes the value to the TC1 cycle register (TC1PRD). When the value of the TC1 counter is equal to the PRD value, the following events occur in the next increment cycle:

- The counter clears;
- Corresponding PWM output pin high level;
- Generate PWM cycle overflow interrupt (if enabled);
- PWM duty cycle is latched from PWMDT to DT compare register;

PWM cycle calculation formula:

$$\text{PWM period} = (\text{PRD}) \times (\frac{1}{Fosc}) \times (\text{T1frequency division})$$

Examples:

TC1PRD=100, Fosc=8 MHz, TC1 divider selection =2 divider;

$$\text{PWM period} = (100) \times \left(\frac{1}{8}\right) \times (2) = 25\ \text{us}$$

PWM duty cycle calculation formula:

$$\text{PWM duty cycle} = (\text{DT}) \times (\frac{1}{Fosc}) \times (\text{T1frequency division})$$

Example:

PWMDT=50, Fosc=8 MHz, TC1 divider selection =2 dividers;

$$\text{PWM duty cycle} = (50) \times \left(\frac{1}{8}\right) \times (2) = 12.5\ \text{us}$$

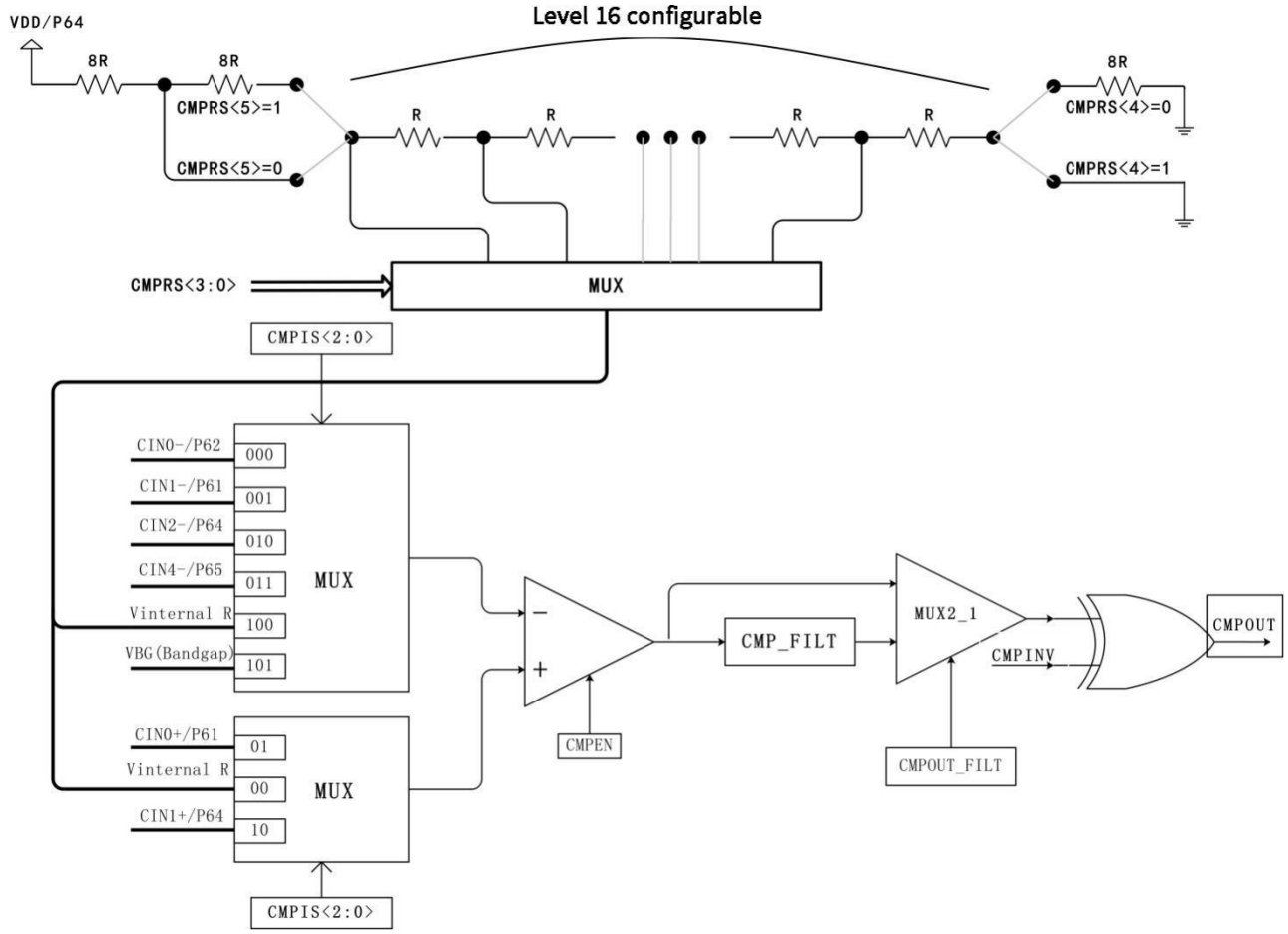
3.9.3 PWM pulse width modulation setting instructions

- Set the CPUCON register, select the IPWM inverse output, PWM clock source and PWM wake-up function;
- Set the TC1CON register and select the corresponding TC1 mode and TC1 frequency division ratio.
- Set the values of RPAGE-R9, RA and RB registers to determine the cycle and duty cycle of the TC1 channel;
- Enable TC1 cycle overflow interrupt and execute "EI" or "DI" instruction (if necessary);

3.10 CMP comparator

The JZ8P1530 has a built-in hardware comparator, which can compare any two of the input pin, the internal reference voltage $V_{internal\ R}$, and the built-in Bandgap (1.26v), selecting one as a positive input and the other as a negative input. The negative input of the comparator can be P61, P62, P64, P65, divider resistor (selected by CMPRS<5:0>), built-in Bandgap (1.26v). The positive input to the comparator can be P61, P64, divider resistor (selected by CMPRS<5:0>). (The same port cannot be used as both positive and negative inputs, nor can the voltage divider input source be used as both positive and

negative.)



Comparator schematic illustration

The divider resistor can be configured via CMPCON control register to select the input voltage source as P64 port input or VDD.

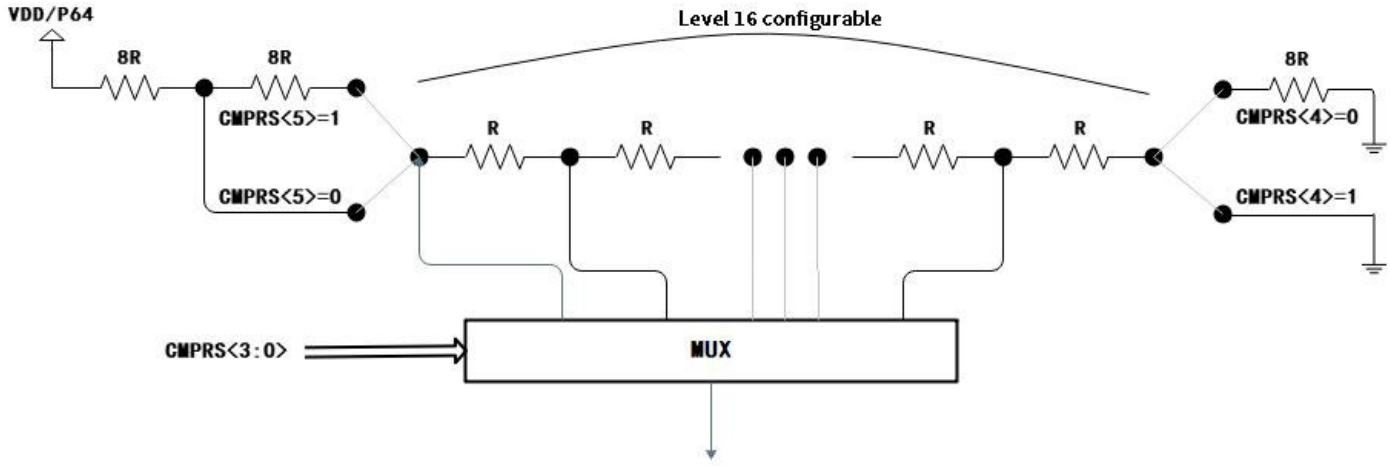
The output result of the comparator can be selected as P60 port output, and the output is supported to be negative. The chip supports digital filtering of output results, which can be selected in OPTION.

Comparator support output result change trigger interrupt, enable CMPIE can generate interrupt signal.

The comparator supports the output result change wake-up, so that CMPWE can wake up the idle mode and sleep mode. In idle mode and sleep mode, if CMPEN is enabled, the low-speed oscillator will be enabled, and the sleep power consumption will become high.

3.10.1 Divider resistor output voltage Vinternal R

The output voltage $V_{internal\ R}$ of the divider resistor is composed of a series of resistors that can generate different levels of reference voltage. CMPRS<5:0> jointly determines the size of $V_{internal\ R}$, CMPRS<5> and CMPRS<4> select the highest and lowest value of $V_{internal\ R}$, CMPRS<3:0> is used to select the desired voltage level, is from the highest and lowest value of $V_{internal\ R}$ evenly divided into 16 equal parts, selected by CMPRS<3:0>.



Schematic diagram of comparator adjustment

例 1：CMPRS<5>=0，CMPRS<4>=0

Range of values:$V_{internal\ R} = (3/4) * VDD \sim (1/4) * VDD + (1/32) * VDD$

Formula:$V_{internal\ R} = (1/4) * VDD + \frac{(n+1)}{32} * VDD$

例 2：CMPRS<5>=0，CMPRS<4>=1

Range of values:$V_{internal\ R} = (2/3) * VDD \sim (1/24) * VDD$

Formula:$V_{\textbf{internal R}} = \frac{(n+1)}{24} * VDD$

例 3：CMPRS<5>=1，CMPRS<4>=0

Range of values:$V_{\textbf{internal R}} = (3/5) * VDD \sim (1/5) * VDD + (1/40) * VDD$

Formula:$V_{\textbf{internal R}} = (1/5) * VDD + \frac{(n+1)}{40} * VDD$

例 4：CMPRS<5>=1，CMPRS<4>=1

Range of values:$V_{\textbf{internal R}} = (1/2) * VDD \sim (1/32) * VDD$

Formula:$V_{\textbf{internal R}} = \frac{(n+1)}{32} * VDD$

n=CMPRS<3:0>

3.10.2 Comparator configuration

Enable CMPEN when using the comparator, set CMPIS<5:0> to select positive and negative input sources, and set the ports of positive and negative electrodes as input. The same port cannot be used as positive and negative inputs at the same time, and the voltage divider input source cannot be used as positive and negative electrodes at the same time.

If the resistor voltage divider is selected as the input source, set the register CMPRS<5:0> according to the need, and select the required voltage divider resistor output voltage $V_{\textbf{internal R}}$ for comparison.

Example 1:

Choose P62 as the negative end input and the voltage of $V_{\textbf{internal R}}$ as (18/32)*VDD as the positive input, $V_{\textbf{internal R}}$ choose the configuration mode of CMPRS<5>=0, CMPRS<4>=0, CMPRS<3:0>=4b '1001 (n=9) to obtain

Vinternal R = (1/4)*VDD + [(9+1)/32]*VDD = (18/32)*VDD

When the configuration is completed, enable CMPCON0(R7) control register of Bit7 bit CMPEN, the comparator starts to compare, and can configure CMPCON1 (R8) control register of Bit7 bit CMPOE to select P60 port to output the comparison results (P60 port needs to be set as output), The output result can also be negated by the Bit6 bit CMPINV configured to control the register

3.10.3 Bandgap usage

The built-in Bandgap reference voltage can provide a voltage of 1.26V, which measures the external supply voltage level. This can be achieved by selecting the Bandgap reference voltage for negative input to compare with the positive input Vinternal R. The power supply of Vinternal R is set to VDD, and the voltage of VDD can be known by comparing the Vinternal R voltage level with the Bandgap reference voltage. If n (CMPRS[3:0] decimal) is set so that Vinternal R is closest to 1.26V, using the four cases in 3.10.1 as an example, the voltage of VDD can be calculated using the following formula:

For using Case 1: VDD = [32/(n+9)] * 1.26V;

For using Case 2: VDD = [24/(n+1)] * 1.26V;

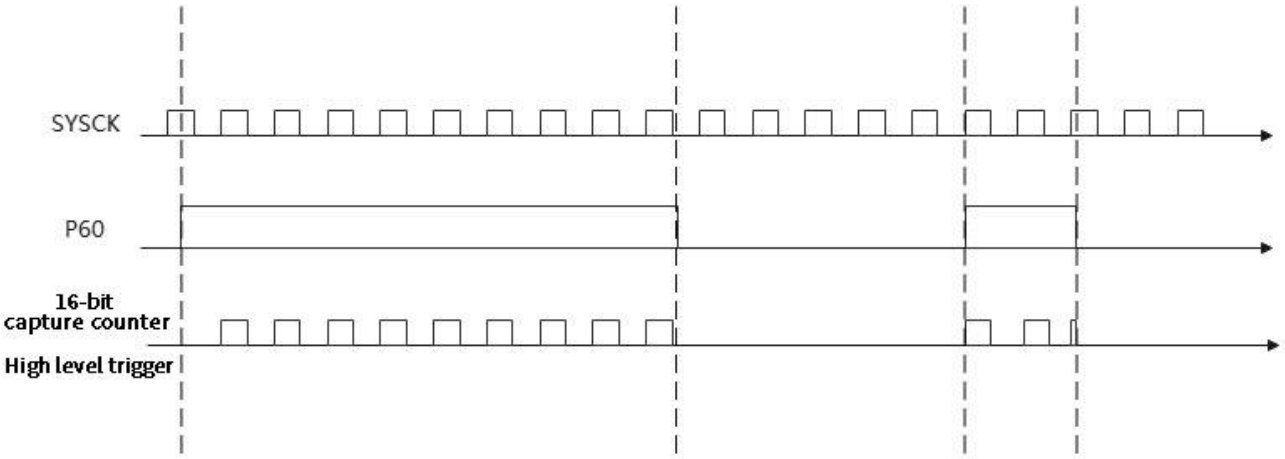
For using Case 3: VDD = [40/(n+9)] * 1.26V;

For using Case 4: VDD = [32/(n+1)] * 1.26V;

3.11 Port level capture

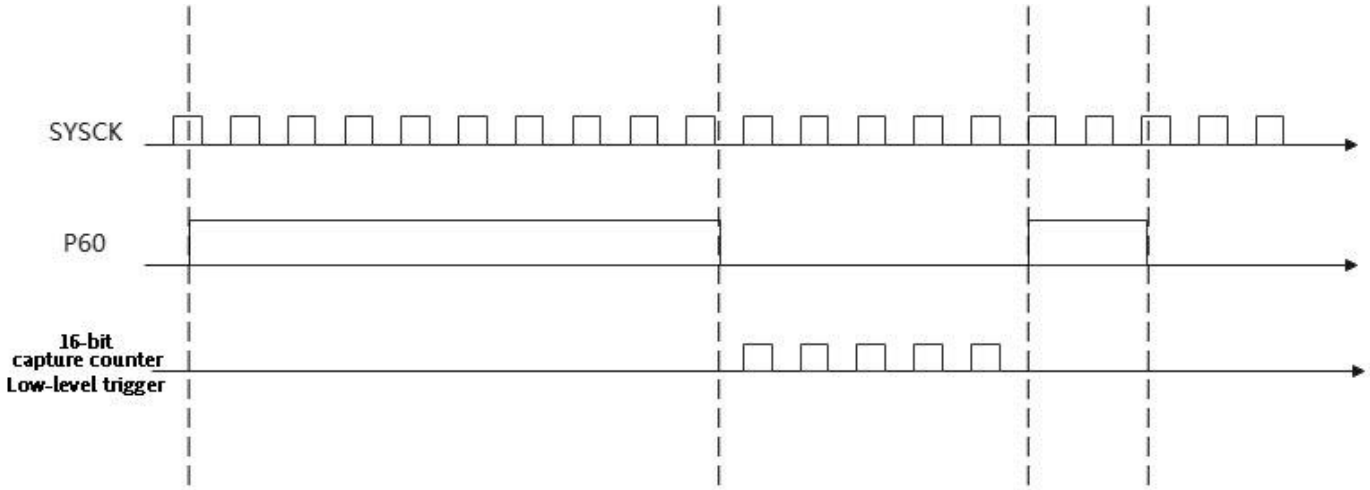
JZ8P1530 provides P60 port level capture function, by multiplexing TC0 8Bit predivider TPRE (level capture counter low 8 bits) and 8Bit counter TC0C (level capture counter high 8 bits) combined into a 16Bit level capture counter, and at the same time with the P60 external interrupt to achieve level change trigger interrupt. Determine the capture time of the previous level in the interrupt program. The P60 external interrupt can be triggered by selecting the edge through the IOCE/WDTCON register INTEDG<1:0>.

The P60 port high level acquisition is achieved by multiplexing the TC0 predivider and counter. Set IOCE/WDTCON register **TC0GATE<1>=1 select TC0 as the gate** counter and select TC0 clock source as the system clock, at the same time enable **INTEDG<0>=1 external interrupt function, finally enable TC0EN=1**. When the P60 port is high, the TC0 pre-frequency division and counter start counting, the counting clock is the system clock, and the P60 port is low, the TC0 pre-frequency division and counter stop counting, the user can trigger the interrupt through the falling edge of the P60 external interrupt and read the count value of R1/TC0C, IOC9/TPRE register in the interrupt program. In order to calculate the level time.



The 16-bit capture counter consists of a low-octet TBRE and a high-octet TC0

P60 port low level capture is similar to high level, by multiplexing TC0 predivider and counter, set IOCE/WDTCON register **TC0 gate <1>=1** select TC0 as the gate counter and select TC0 clock source as the system clock, and enable **INTEDG<1>=1 and external interrupt function. Finally, enable TC0EN=1**. When the P60 port is low, the TC0 predivider and counter start counting, the counting clock is the system clock, and the P60 port is high, the TC0 predivider and counter stop counting, the user can trigger the interrupt through the rising edge of the P60 external interrupt and read the count value of R1/TC0C, IOC9/TPRE register in the interrupt program. In order to calculate the level time.

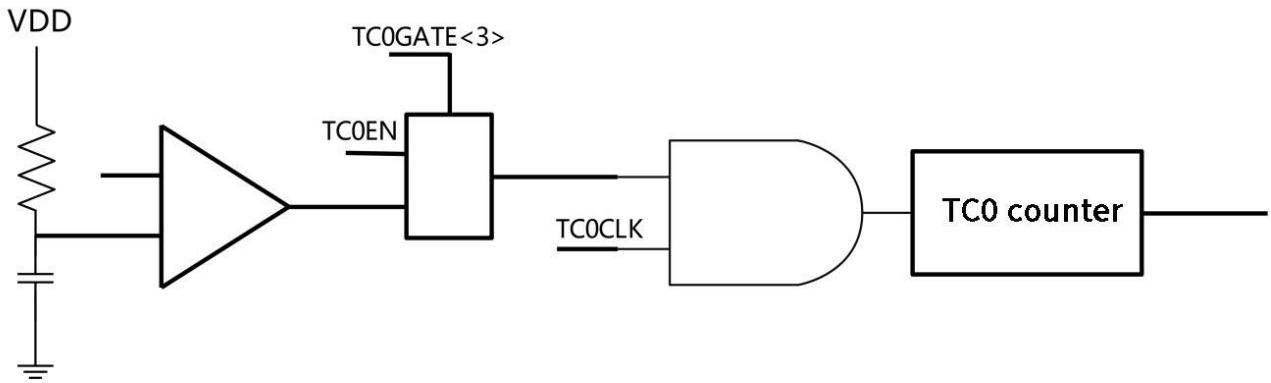


The 16-bit capture counter consists of a low-octet TBRE and a high-octet TC0

3.12 RFC Resistance Frequency Conversion

JZ8P1530 built-in RFC resistance frequency conversion function, by selecting the TC0 counting gate source as the comparator output result, to achieve the time count of external voltage change.

The specific implementation is: enable the TC0GATE<2> of the **WDTCON** register, select the TC0 count controlled by CMPOUT, when CMPOUT=1, TC0 start counting, CMPOUT=0, TC0 stop counting. Configure the comparator function through **CMPCON0**, **CMPCON1**, P6AE registers, first enable the required analog port, set the positive input source of the comparator as a fixed level, and select the negative input source of the comparator as an external port. As shown in the figure, first set the port of the negative input source to the output high level, then the comparator result output bit CMPOUT=0, the TC0 timer does not count, set the initial value of the TC0 timer. When the port of the positive input source is set as the input port, the RC circuit on the port starts charging, when the port voltage is lower than the level of the positive input source, TC0 starts counting, when the port voltage is higher than the level of the positive input source, TC0 stops counting, TC0 is equivalent to recording the charging time of RC.



RFC structure illustration diagram

4 OPTION configuration sheet

CODE OPTION	Options	Feature Description
Watchdog	Enable	Watchdog WDT enables
	Forbidden	Watchdog WDT prohibited
Clocks split frequency	2 Clocks	Choose 2 Clocks for the instruction cycle
	4 Clocks	The instruction cycle is chosen to be 4 Clocks
	8 Clocks	Choose 8 Clocks for the instruction cycle
	16 Clocks	Choose 16 Clocks for the instruction cycle
	32 Clocks	Select 32 Clocks for instruction cycles
IRC oscillator voltage source selection	Choose VDD voltage for IRC oscillator	Choose VDD voltage for IRC oscillator voltage source
	Choose LDO voltage for IRC oscillator	IRC oscillator voltage source Select LDO voltage
IRC frequency	8M	Choose 8M for IRC frequency
	1M	The IRC frequency is chosen to be 1M
	910KHz	Choose 910KHz for IRC frequency
System clock frequency multiplier selection	Forbidden	No doubling of the system clock is selected
	Enable	System clock select frequency doubling (system clock is the basic clock running inside the chip, CPUCON register can configure the system clock to low speed or high speed mode, pay attention to the difference with oscillator frequency doubling)
Low-voltage reset option	Enable	Enable the LVR feature
	Disable	LVR function is prohibited. Be aware of the risk of chip entering dead zone
Low voltage reset point selection	As = 1.2 V	Choose 1.2V for the low voltage reset point
	As = 1.6 V	Choose 1.6V as the low voltage reset point
	As = 1.8 V	Choose 1.8V as the low voltage reset point
	As = 2.6 V	Choose 2.6V as the low voltage reset point
	As = 2.8 V	Choose 2.8V for the low voltage reset point
	As = 3.6 V	Choose 3.6V for the low voltage reset point
	As = 4.0 V	Choose 4.0V as the low voltage reset point
	As = 4.3 V	Choose 4.3V as the low voltage reset point
OTP paging selection	Use 1K	The ROM area is chosen to be 1K
	Use the first 0.5K	Select the first 0.5K for the ROM area

	Use the last 0.5K	The ROM area is selected after 0.5K
Code encryption	Enable	Burn mode data encryption
	Forbidden	Burn mode data is not encrypted
Reset port pull up	Enable	Enable P63 port pull-up
	Disable	Disallow P63 port pull-up
P63 port	GPIO	P63 serves as a general purpose I/O port
	RST	P63 serves as an external reset port
Reset time	PWRT = WDT = 4.5 ms	Reset setup time =WDT overflow time (regardless of frequency) = 4.5ms
	PWRT=WDT=18ms	Reset setup time =WDT overflow time (regardless of frequency) = 18ms
	PWRT=WDT=72ms	Reset setup time =WDT overflow time (regardless of frequency) = 72ms
	PWRT=WDT=288ms	Reset setup time =WDT overflow time (regardless of frequency) = 288ms
	PWRT = 140 us, WDT = 4.5 ms	Reset setup time =140us,WDT overflow time (regardless of frequency) =4.5ms
	PWRT=140us,WDT=18ms	Reset setup time =140us,WDT overflow time (regardless of frequency) =18ms
	PWRT=140us,WDT=72ms	Reset setup time =140us,WDT overflow time (regardless of frequency) =72ms
	PWRT=140us,WDT=288ms	Reset setup time =140us,WDT overflow time (regardless of frequency) =288ms
Look-up table range	1/4K	Can look up tables 1/4K in front of program space
	1K	Tables can be looked up in program space 1K
CMP_FILT	Comparator results digitally filtered Forbidden	Comparator result bit CMPOUT is output directly without filtering
	Comparator results are digitally filtered Enable	Comparator result bit CMPOUT filtered output

5. Instruction set

Instructions	Command action	Flag impact
ADD A,R	A+R→A	Z,C,DC
ADD R,A	A+R→R	Z,C,DC
AND A,R	A&R→A	Z
AND R,A	A&R→R	Z
CLRA	0→A	Z
CLR R	0→R	Z
INVA R	/R→A	Z
INV R	/R→R	Z
DA	A register adjusts to BCD value	C
DECA R	R-1→A	Z
DEC R	R-1→R	Z
DJA R	R-1→A, skip if zero	-
DJ R	R-1→R, skip if zero	-
INCA R	R+1→A	Z
INC R	R+1→R	Z
IJA R	R+1→A, skip if zero	-
IJ R	R+1→R, skip if zero	-
MOV R,A	A→R	-
MOV A,R	R→A	Z
MOV R,R	R→R	Z
OR A,R	A∨VR→A	Z
OR R,A	A∨VR→R	Z
SUB A,R	R-A→A	Z,C,DC
SUB R,A	R-A→R	Z,C,DC
XOR A,R	A⊕R→A	Z
XOR R,A	A⊕R→R	Z
IR R	IOCR→A	-
IW R	A→IOCR	-
CTR	TCOCON→A	-
CTW	A→TCOCON	-
BTC R,b	0→R(b)	-

BTS R,b	1→R(b)	-
JBTC R,b	if R(b)=0, skip	-
JBTS R,b	if R(b)=1, skip	-
LCR R	R(n)→R(n+1),R(7)→C, C→R(0)	C
LCA R	R(n)→A(n+1),R(7)→C, C→A(0)	C
RCR R	R(n)→R(n-1),R(0)→C, C→R(7)	C
RCA R	R(n)→A(n-1),R(0)→C, C→A(7)	C
SWAP R	R(0-3) ↔ R(4-7)	-
SWAPA R	R(0-3)→A(4-7),R(4-7)→A(0-3)	-
ADD A,k	A+k→A	Z,C,DC
AND A,k	A&k→A	Z
MOV A,k	k→A	-
OR A,k	A∨k→A	Z
SUB A,k	k-A→A	Z,C,DC
XOR A,k	A⊕k→A	Z
CALL k	PC+1→[SP], (Page,k)→PC	-
DI	Disallow interruption	-
EI	Enable Interrupt	-
JMP k	K (Page,k)→PC	-
NOP	Empty instruction	-
RET	[top of stack]→PC	-
RETI	[top of stack]→PC, enable interrupt	-
RETL k	k→A,[top of stack]→PC	-
SLEEP	0→WDT, the oscillator stops oscillating (sleep mode)	T,P
CWDT	0→WDT	T,P

6. Electrical characteristics

6.1 Limit parameters

Working temperature... -40℃ ~ 85℃
Storage temperature... -65 C to 150 C
The input voltage... Vss-0.3V ~ Vdd+0.5V
The output voltage... Vss-0.3V ~ Vdd+0.5V
Working voltage... 1.2 V to 5.5 V

6.2 DC electrical characteristics

(VDD =5V, operating temperature =25 ° C, unless otherwise stated)

Symbols	Parameter description	Conditions	Minimum	Typical	Largest	Units
IRC1	IRC1 (after correction)	OPTION select 8MHz		8		MHz
IRC2	IRC2 (after correction)	OPTION select 1MHz		1		MHz
IRC3	IRC3 (after correction)	OPTION select 910KHz		910		KHz
VIL1	P65:P64, P62:P60 Input low		-	-	1.3	V
VIL2	P63 Input low		-	-	2.5	V
VIH1	P65:P64, P62:P60 Enter high level		2.5	-	-	V
VIH2	P63 Input high		2.5	-	-	V
IOH1	Output high level drive	Ioh = 4.4 V	13	16	19	mA
IOL1	Output low level drive	Iol = 0.6 V	19	22	25	mA
RPH1	Pull-up resistor	VDD=5V, GPIO connected to GND		52	55	K Ω
RPH2	Pull-up resistor	VDD=3V, GPIO connected to GND		100	105	K Ω
RPD1	Pull-down resistor	VDD=5V, the GPIO is connected to VDD		100	105	K Ω
RPD2	Pull-down resistor	VDD=3V, GPIO connected to VDD		180	190	K Ω
Isb1	Power off current 1	The input is connected to VDD, the output is	-	-	1	μA
Isb2	Power off current 2	The input is connected to VDD, the output is	-	-	12	μA
Iop2	Operating current 1 (VDD=5V)	IRC=8MHz 2clock	-	1.2	1.5	mA
Iop2	Working current 2 (VDD=5V)	IRC=1MHz 2clock	-	0.2	0.3	mA

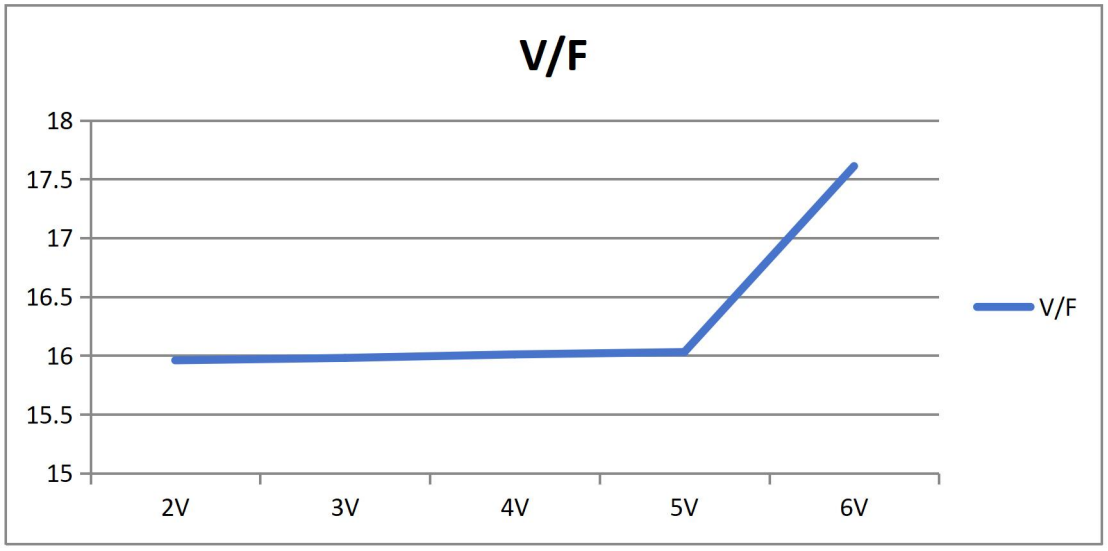
LVR	Low voltage reset voltage	Select the LVR reset point	Vlvr - 0.2 -	Vlvr	Vlvr + 0.2	V
Note: The above parameters are for reference only, please refer to the measured data of the target prototype.						

6.3 Characteristic curve diagram

The curves listed in this chapter are for design reference only, and part of the data given may exceed the specified working range of the chip. In order to ensure the normal operation of the chip, please strictly refer to the electrical characteristics.

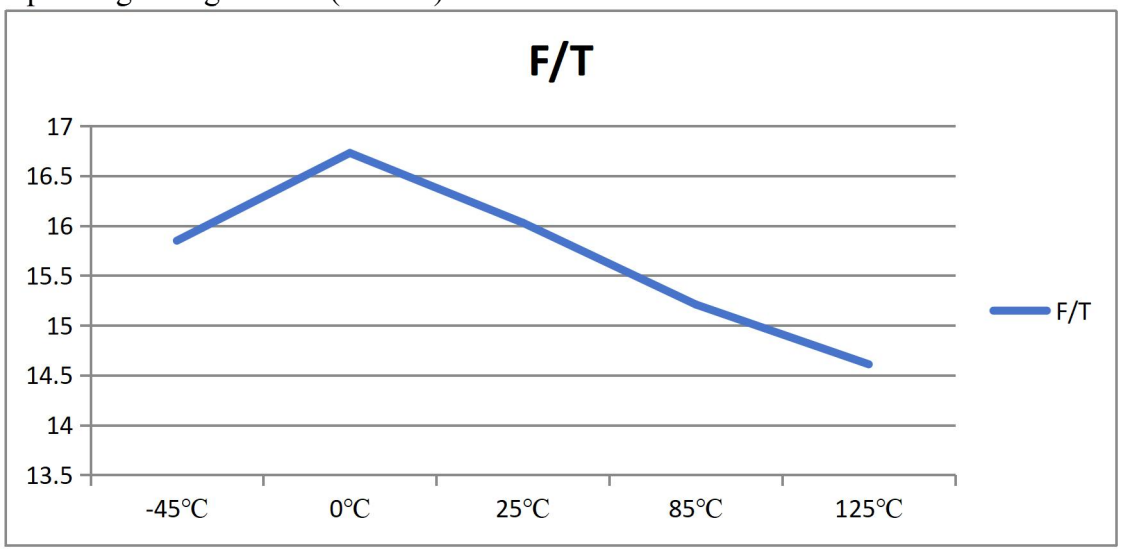
6.3.1 Internal low-speed RC oscillator - voltage-frequency characteristic curve

Operating temperature at 25℃ : (in KHz)



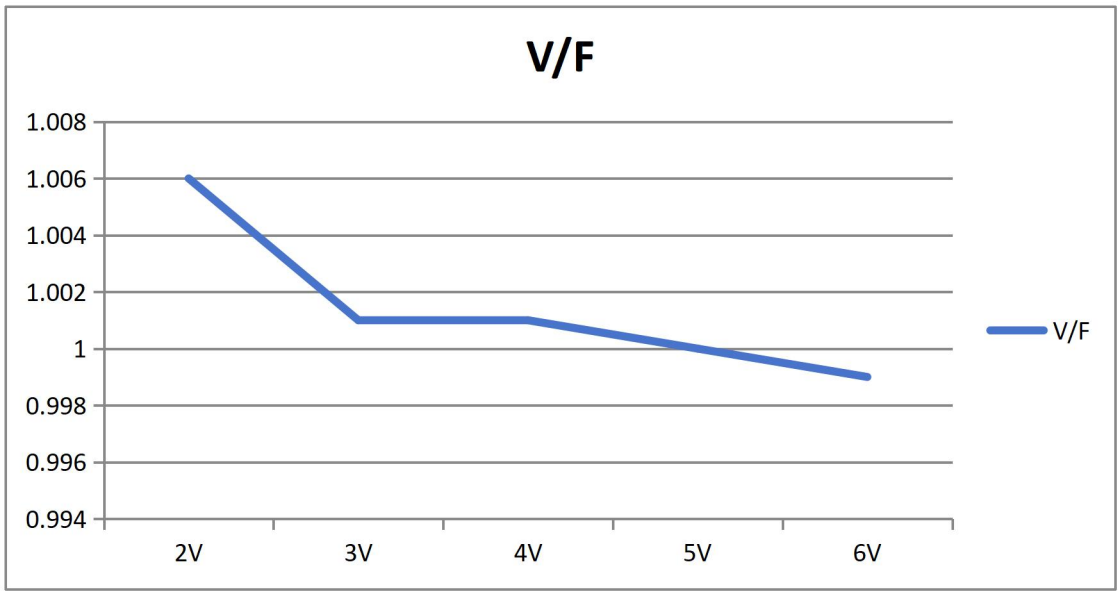
6.3.2 Internal low-speed RC oscillator - Temperature-frequency characteristic curve

Operating voltage at 5V: (in KHz)



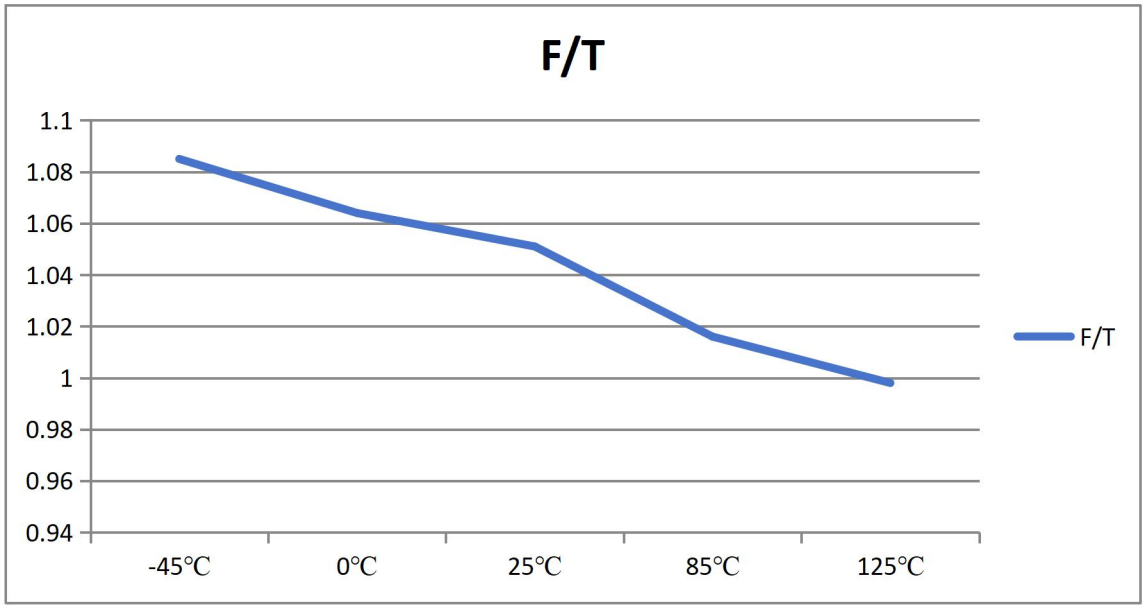
6.3.3 Internal 1MHz RC oscillator - voltage-frequency characteristic curve

Operating temperature at 25℃ : (in MHz)



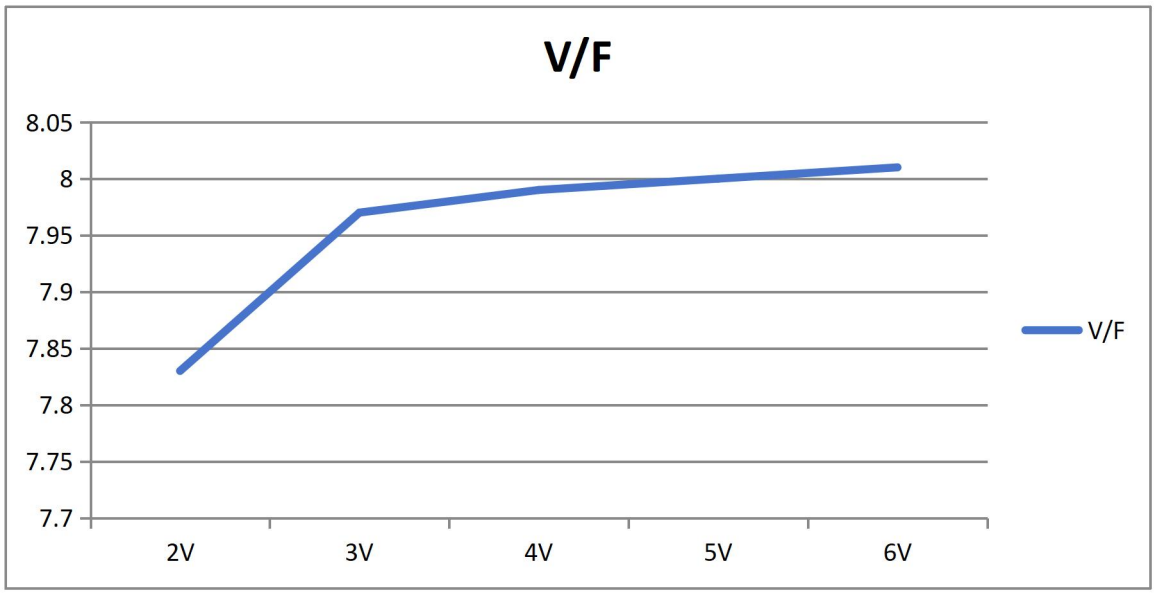
6.3.4 Internal 1MHz RC oscillator - Temperature-frequency characteristic curve

Operating voltage at 5V: (in MHz)



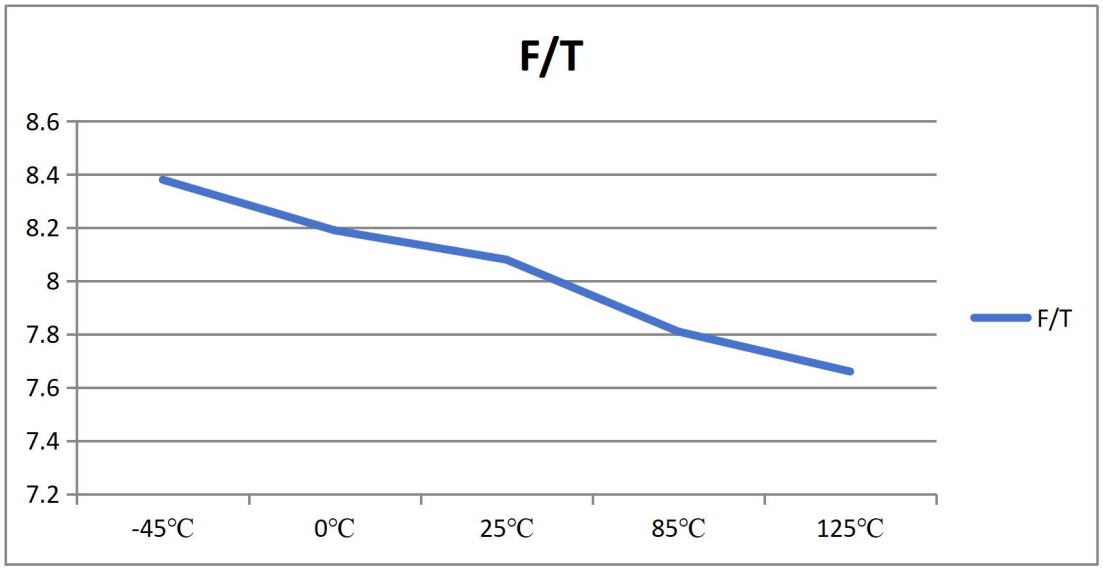
6.3.5 Internal 8MHz RC oscillator - voltage-frequency characteristic curve

Operating temperature at 25 ° C: (in MHz)



6.3.6 Internal 8MHz RC oscillator - Temperature-frequency characteristic curve

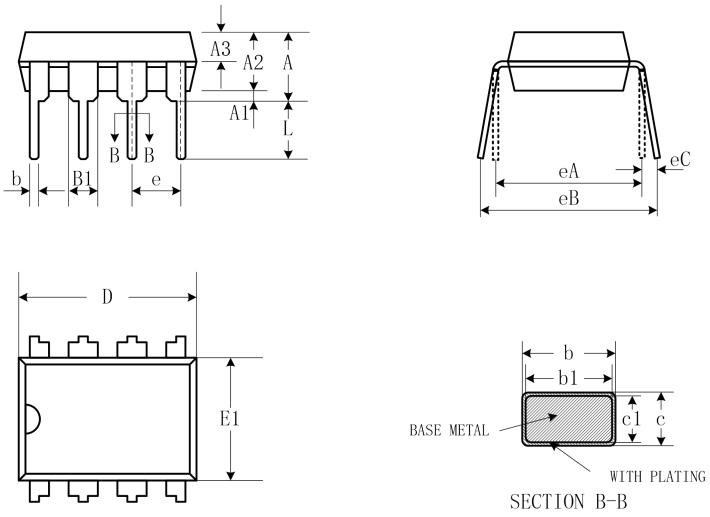
Operating voltage at 5V: (in MHz)



7 Package size

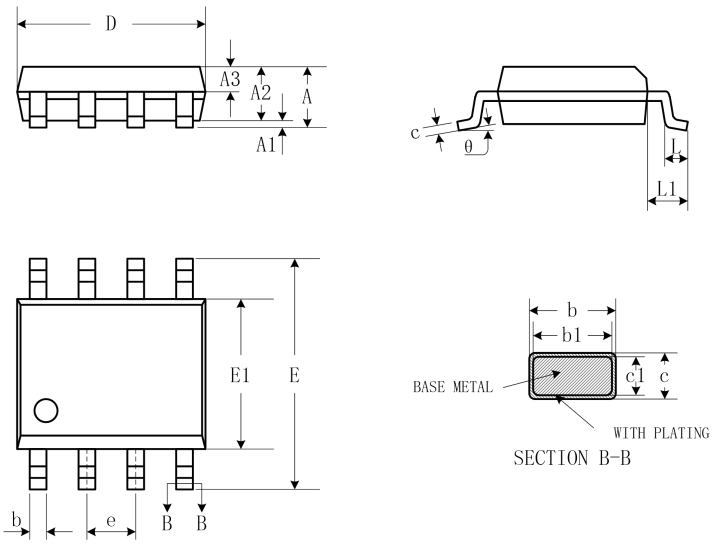
7.1 8PIN package size

DIP8



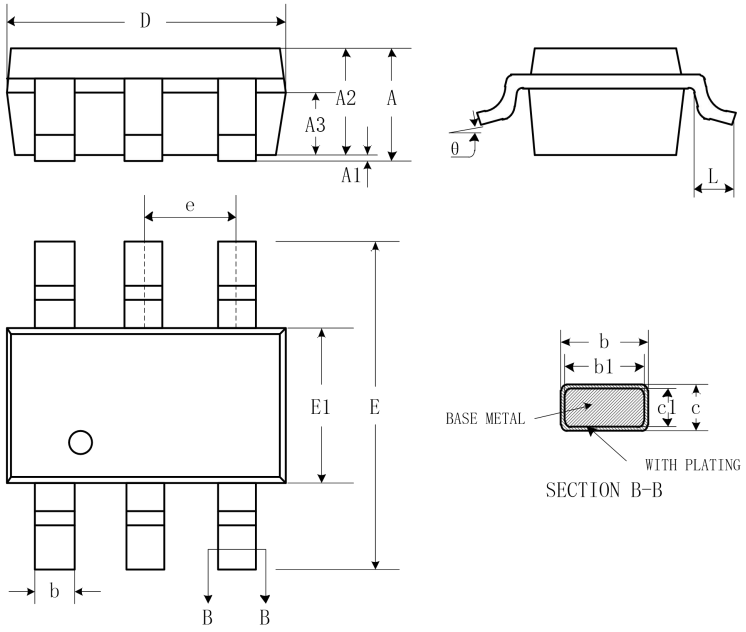
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	-	-
A2	3.10	3.30	3.50
A3	1.50	1.60	1.70
b	0.44	-	0.53
b1	0.43	0.46	0.48
B1	1.52 BSC		
c	0.25	-	0.31
c1	0.24	0.25	0.26
D	9.05	9.25	9.45
E1	6.15	6.35	6.55
e	2.54 BSC		
eA	7.62 BSC		
eB	7.62	-	9.50
eC	0	-	0.94
L	3.00	-	-

SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
L	0.50	0.65	0.80
L1	1.05 BSC		
Theta.	0	-	8 °

7.2 6PIN package size



Package Specifications:

Symbol	mm			Inch		
	MIN	NOM	MAX	MIN	NOR	MAX
A	-	-	1.35	-	-	0.053
A1	0.04	-	0.15	0.002	-	0.006
A2	1.00	1.10	1.20	0.039	0.043	0.047
A3	0.55	0.65	0.75	0.022	0.026	0.030
b	0.30	-	0.50	0.013	-	0.017
b1	0.30	0.40	0.45	0.013	0.016	0.018
c	0.08	-	0.22	0.006	-	0.008
c1	0.08	0.13	0.20	0.003	0.005	0.08
D	2.72	2.92	3.12	0.107	0.115	0.123
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95 BSC			0.037 BSC		
L	0.30	-	0.60	0.012	-	0.024
Theta.	0	-	8 DHS	0	-	8 DHS