JZ8P2508

8-bit OTP Microcontroller

User Manual

Version V2.1

Revision History

Version	Modification Description	Remarks
V1.0	Completed initial draft	
V1.1	Add register description	
V1.2	Modify PWMSCR register description	
V2.0	Modify content format	
V2.1	Modify the register description of the port wake-up part	

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1 Chip Introduction

1.1 Functional Features

CPU Configuration

- 2K×14-Bit OTP ROM
- 96×8-Bit SRAM
- 8-level stack space
- 7-level programmable voltage reset (LVR)
  1.2V, 1.6V, 1.8V, 2.4V
  2.7V, 3.5V, 3.9V
- Working current less than 1.5 mA (8MHz/5V)
- Working current 20μA (32KHz/3V)
- Sleep current less than 1 μA (sleep mode)

I/O Configuration

- 3 groups of bidirectional IO ports: P5, P6, P7
- 18 I/O pins
- Wake-up port: P5 port, P6 port
- 18 programmable pull-up I/O pins
- 17 programmable pull-down I/O pins
- External interrupt: P60
- External voltage detection: P57
- P57 (Reset Pin) Configurable Pull-up and GPIO
- 8 Programmable Open-Drain I/O Pins
- 18 Programmable Drive Enhanced I/O Pins

Working voltage

- Operating voltage range:
  1.8V～5.5V (0℃-70℃)
  2.3V～5.5V (-40℃-85℃)

Working frequency

- Built-in IRC oscillation circuit: 8MHz, 1MHz, 910KHz
- Built-in RC oscillator power supply:
  VDD, LDO 2.1V
- External XT oscillation circuit:
- Instruction cycle frequency division selection:
  2T, 4T, 8T, 16T, 32T

Peripheral modules

- 8Bit Timer/Counter
- Programmable WDT timer
- 5-channel 12Bit Pulse Width Modulator PWM

Interrupt source

- TCC Overflow Interrupt
- External interrupt
- Interrupt generated by input port state change
- Low Voltage Detection (LVD) change interrupt
- PWM cycle interrupt

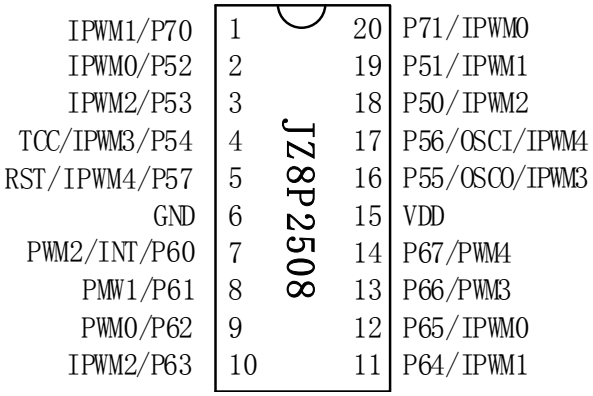
Features

- Software adjustable multi-level LVD
  2.0V~4.7V, 0.1V/level

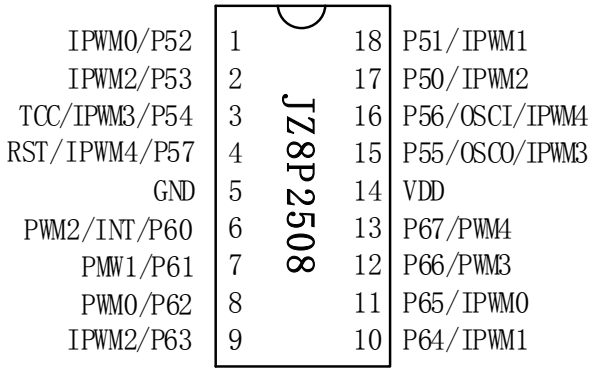
Package type

- JZ8P2508-DIP/SOP20;
- JZ8P2508-DIP/SOP18;
- JZ8P2508-DIP/SOP16;
- JZ8P2508-DIP/SOP14;
- JZ8P2508-DIP/SOP8;

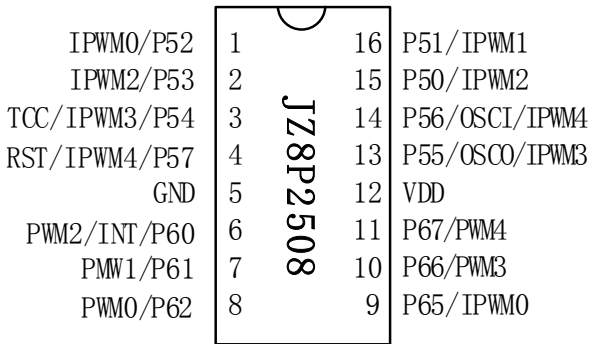
1.2 Pin assignment



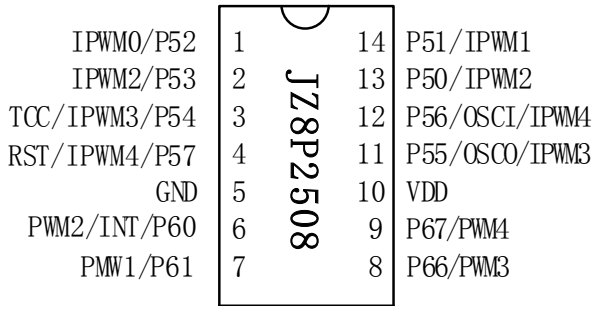
JZ8P2508-20PIN



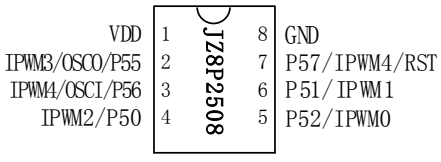
JZ8P2508-18PIN



JZ8P2508-16PIN



JZ8P2508-14PIN



JZ8P2508-8PIN

1.3 Pin Description

Serial	Pin Name	I/O	Function Description
P50	P50	I/O	GPIO, programmable pull-up/pull-down, programmable output
	IPWM2	CMOS output	PWM2 complementary output
P51	P51	I/O	GPIO, programmable pull-up/pull-down, programmable output
	IPWM1	CMOS output	PWM1 complementary output
P52	P52	I/O	GPIO, programmable pull-up/pull-down, programmable output
	IPWM0	CMOS output	PWM0 complementary output
P53	P53	I/O	GPIO, programmable pull-up/pull-down, programmable output
	IPWM2	CMOS output	PWM2 complementary output
P54	P54	I/O	GPIO, programmable pull-up/pull-down, programmable output
	TCC	I	External TCC signal source input pin
	IPWM3	CMOS output	PWM3 complementary output
P55	P55	I/O	GPIO, programmable pull-up/pull-down, programmable output
	OSCO	O	Oscillator output port
	IPWM3	CMOS output	PWM3 complementary output
P56	P56	I/O	GPIO, programmable pull-up/pull-down, programmable output
	OSCI	I	External crystal oscillator input port
	IPWM4	CMOS output	PWM4 complementary output
P57	P57	GPIO	GPI, programmable pull-up, programmable output drive
	RST	I	Reset port
	IPWM4	CMOS output	PWM4 complementary output
	EXVE	I	LVD external voltage detection port
P60	P60	I/O	GPIO, programmable pull-up/pull-down, open drain, 4-level high
	INT0	I	External interrupt input port
	PWM2	CMOS output	PWM2 output
P61	P61	I/O	GPIO, programmable pull-up/pull-down, open drain, 4-level high
	PWM1	O	PWM1 output
P62	P62	I/O	GPIO, programmable pull-up/pull-down, open drain, 4-level high
	PWM0	O	PWM0 output
P63	P63	I/O	GPIO, programmable pull-up/pull-down, open drain, programmable
	IPWM2	CMOS output	PWM2 complementary output
P64	P64	I/O	GPIO, programmable pull-up/pull-down, open drain, programmable
	IPWM1	CMOS output	PWM1 complementary output
P65	P65	I/O	GPIO, programmable pull-up/pull-down, open drain, programmable
	IPWM0	CMOS output	PWM0 complementary output
P66	P66	I/O	GPIO, programmable pull-up/pull-down, open drain, 4-level high
	PWM3	CMOS output	PWM3 output
P67	P67	I/O	GPIO, programmable pull-up/pull-down, open drain, 4-level high
	PWM4	CMOS output	PWM4 output

P70	P70	I/O	GPIO, programmable pull-up/pull-down
	IPWM1	CMOS output	PWM1 complementary output
P71	P71	I/O	GPIO, programmable pull-up/pull-down
	IPWM0	CMOS output	PWM0 complementary output
	VDD	--	Power supply
	VSS	--	Ground

2.2 Data storage area

2.2.1 RPAGE\IOPAGE\Bank Data Register Area

Address	RPAGE Page Register
0x00	R0/IAR Indirect Addressing Memory
0x01	R1/TCC Timer Counter
0x02	R2/PC Program Counter
0x03	R3/STATUS status register
0x04	R4/RSR RAM Selection Register
0x05	R5/PORT5 Data Register
0x06	R6/PORT6 Data Register
0x07	R7/PORT7 Data Register
0x08	R8/LVDCON Control Register
0x09	Reserved
0x0A	Reserved
0x0B	Reserved
0x0C	RC/P5ICECR P5 Input Status Change Interrupt Enable
0x0D	RD/P6ICECR P6 Input Status Change Interrupt Enable
0x0E	RE/CPUCON CPU Mode Control Register
0x0F	RF/ISR Interrupt Flag Register
0x10 ～ 0x6F	SRAM General Purpose Register
0x70	R70/PWM0CR (PWM0 Control Register)
0x71	R71/PWM1CR (PWM1 Control Register)
0x72	R72/PWM2CR (PWM2 Control Register)
0x73	R73/PWM3CR (PWM3 Control Register)
0x74	R74/PWM4CR (PWM4 Control Register)
0x75	R75/P5HDCR (P5 High Pull-up Current Control
0x76	R76/P5HSCR (P5 High Sink Current Control Register)
0x77	R77/P6HDCR (P6 High Current Control Register)
0x78	R78/P6HSCR (P6 High Sink Current Control Register)
0x79	R79/P5WDCR (P5 Weak Pull-up Current Control
0x7A	R7A/P5WSCR (P5 Weak Sink Current Control Register)
0x7B	R7B/DEADCR (PWM Dead Time Control Register)
0x7C	R7C/DEADTR (Dead Time Timer Register)
0x7D	Reserved
0x7E	Reserved
0x7F	Reserved

Address	IOPAGE page register
0x00	Reserved
0x01	CONT (Control Register)
0x02	Reserved
0x03	Reserved
0x04	Reserved
0x05	IOC5/P5CR (P5 Direction Control Register)
0x06	IOC6/P6CR (P6 Direction Control Register)
0x07	IOC7/P7CR (P7 Direction Control Register)
0x08	IOC8/PHDCR0 (Pull-up/Pull-down Control Register
0x09	IOC9/PHDCR1 (Pull-up/Pull-down Control Register
0x0A	IOCA/PHDCR2 (Pull-up/Pull-down Control Register
0x0B	IOCB/PDCR (Pull-down Control Register)
0x0C	IOCC/P6ODCR (P6 Port Open-Drain Control Register)
0x0D	IOCD/P6PHCR (P6 Port Pull-up Control Register)
0x0E	IOCE/CWDTR (WDT Control Register)
0x0F	IOCF/IMR (Interrupt Enable Control Register)
0x10	IOC10/PRDCH0 (PWM0 Period Duty Cycle High
0x11	IOC11/PRDL0 (PWM0 Period Low Register)
0x12	IOC12/PDCL0 (PWM0 Duty Cycle Low Register)
0x13	IOC13/PRDCH1 (PWM1 period duty cycle high
0x14	IOC14/PRDL1 (PWM1 period low register)
0x15	IOC15/PDCL1 (PWM1 duty cycle low register)
0x16	IOC16/PRDCH2 (PWM2 period duty cycle high
0x17	IOC17/PRDL2 (PWM2 period low register)
0x18	IOC18/PDCL2 (PWM2 duty cycle low register)
0x19	IOC19/PRDCH3 (PWM3 period duty cycle high
0x1A	IOC1A/PRDL3 (PWM3 period low register)
0x1B	IOC1B/PDCL3 (PWM3 duty cycle low register)
0x1C	IOC1C/PRDCH4 (PWM4 period duty cycle high
0x1D	IOC1D/PRDL4 (PWM4 Period Low Register)
0x1E	IOC1E/PDCL4 (PWM4 Duty Cycle Low Register)
0x1F	IOC1F/PWMSCR (PWM Mapping Control Register)

3 Functional Modules

3.1 Operation Registers

3.1.1 RPAGE～R0/IAR (Indirect Addressing Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R0<7:0>							

The R0 indirect addressing register is a virtual register that serves as a pointer for indirect addressing. Any instruction that uses R0 as a pointer actually corresponds to the data pointed to by the lower 6 bits FSR<5:0> of R4 (RAM selection register).

3.1.2 RPAGE～R1/TCC (TCC Data Counter)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC<7:0>							

TCC data register, readable and writable

3.1.3 RPAGE～R2/PC (PC Program Counter)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCL<7:0>							

PC pointer low-order register, readable and writable

3.1.4 RPAGE～R3/STATUS (Status Register)

03H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	RST	GP1	GP0	T	P	Z	DC	C
Read/ Write	R	R/W	R/W	R	R	R	R	R
Reset Value	0	0	0	1	1	X	X	X

Bit<7>:RST - Reset Type Flag Bit

0: Other reset types

1: Wake-up caused by pin state change

Bit<6>:GP1 - General Purpose Read/Write Bit

Bit<5>:GP0 - General Purpose Read/Write Bit

Bit<4>:T - Time Overflow Bit

0: WDT overflow

1: Execution of “SLEEP” and “CWDT” instructions or low voltage reset

The events affecting T/P are shown in the table below:

Type	RST	T	P
Power-on reset	0	1	1
Press RESET in working mode	0	Hold	Hold

RESET wake-up	0	1	0
WDT overflow in working mode	0	0	Hold
WDT overflow wake-up	0	0	0
Port status change wake-up	1	1	0
Execute CWDT instruction	Hold	1	1
Execute SLEEP instruction	Hold	1	0

Bit<3>:P - Power-down flag bit

0: Execute the “SLEEP” instruction

1: Power-on reset or execute the “CWDT” instruction

Bit<2>:Z - Zero flag is set to “1” when the result of an arithmetic or logical operation is zero

0: When the result of an arithmetic or logical operation is not 0

1: When the result of an arithmetic or logical operation is 0

Bit<1>:DC - Auxiliary carry flag

0: When performing an addition operation, no carry is generated in the lower four bits; / When performing a subtraction operation, a borrow is generated in the lower four bits

1: When performing an addition operation, a carry is generated in the lower four bits; / When performing a subtraction operation, no borrow is generated

Bit<0>:C - Carry flag

0: When performing an addition operation, no carry is generated in the high four bits; / When performing a subtraction operation, a borrow is generated in the high four bits

1: When performing an addition operation, a carry is generated in the high four bits; / When performing a subtraction operation, no borrow is generated in the high four bits

3.1.5 RPAGE～R4/RSR (RAM Selection Register)

04H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSR	1	FSR<6:0>						
Read/ Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	X	X	X	X	X	X	X

Bit7: Fixed read as 1

Bit<6:0>: FSR<6:0> - Used to select the RAM register address in indirect addressing mode (addressing range: 0X00～0X7F)

FSR is used in conjunction with R0 to implement indirect addressing operations. The user can put the address corresponding to a certain register into FSR, and then access the indirect addressing register R0, at which time the address will point to the register corresponding to the address in FSR.

3.1.6 RPAGE～R5/PORT5 (P5 Data Register)

05H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORT5	P57	P56	P55	P54	P53	P52	P51	P50
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

PORT5 data register, readable and writable

3.1.7 RPAGE～R6/PORT6 (P6 Data Register)

06H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORT6	P67	P66	P65	P64	P63	P62	P61	P60
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

PORT6 data register, readable and writable

3.1.8 RPAGE～R7/PORT7 (P7 Data Register)

07H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PORT7							P71	P70
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1

PORT7 data register, readable and writable

Bit<1:0>:P7<1:0>-PORT7 data register

3.1.9 RPAGE～R8/LVDCON (LVD Control Register)

08H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDCON	LVDEN	LVDF	EXVEN	LVDSEL<4:0>				
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:LVDEN

1: LVD Enable

0: LVD Disable

Bit<6>:LVDF

1: LVD is lower than the preset voltage point

0: LVD is higher than the preset voltage point

Bit<5>:EXVEN

1: LVD detection voltage selects P57 port input

0: LVD detection voltage selects VDD

LVDSEL<4:0>:

LVDSEL<4>	LVDSEL<3>	LVDSEL<2>	LVDSEL<1>	LVDSEL<0>	Voltage
0	0	0	0	0	2.0v
0	0	0	0	1	2.1v
0	0	0	1	0	2.2v
0	0	0	1	1	2.3v
0	0	1	0	0	2.4v
0	0	1	0	1	2.5v
0	0	1	1	0	2.6v
0	0	1	1	1	2.7v
0	1	0	0	0	2.8v
0	1	0	0	1	2.9v
0	1	0	1	0	3.0v
0	1	0	1	1	3.1v
0	1	1	0	0	3.2v
0	1	1	0	1	3.3v
0	1	1	1	0	3.4v
0	1	1	1	1	3.5v
1	0	0	0	0	3.6v
1	0	0	0	1	3.7v
1	0	0	1	0	3.8v
1	0	0	1	1	3.9v
1	0	1	0	0	4.0v
1	0	1	0	1	4.1v
1	0	1	1	0	4.2v
1	0	1	1	1	4.3v
1	1	0	0	0	4.4v
1	1	0	0	1	4.5v
1	1	0	1	0	4.6v
1	1	0	1	1	4.7v

3.1.10 RPAGE～RC/P5ICECR(P5Input State Change InterruptEnable Register)

0CH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5ICECR	P5WK<7>	P5WK<6>	P5WK<5>	P5WK<4>	P5WK<3>	P5WK<2>	P5WK<1>	P5WK<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P5WK<7:0>-P5 Input Status Change Interrupt Enable Control Bit

1: Enable

0: Disable (default)

Note: In the OPTION port wake-up setting selection, if you select P5/P6 port non-independent control, the port wake-up is not controlled by the RC register. Otherwise, the RC register needs to be processed, otherwise the port cannot be woken up.

3.1.11 RPAGE~RD/P6ICECR (P6 Input State Change Interrupt Enable Register)

0DH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6ICECR	P6WK<7>	P6WK<6>	P6WK<5>	P6WK<4>	P6WK<3>	P6WK<2>	P6WK<1>	P6WK<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P6WK<7:0>-P6 input state change interrupt enable control bit

1: Enable

0: Disable (default)

Note: In the OPTION port wake-up setting selection, if you select P5/P6 port non-independent control, the port wake-up is not controlled by the RD register, otherwise the RD register needs to be processed, otherwise the port cannot be woken up.

3.1.12 RPAGE~RE/CPUCON(CPU mode control register)

0EH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUCON	-	TxEN	TCCCKS	PWMWE	TCCWE	STPHX	CLKMD	IDLE
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: Unused, fixed at 0

Bit<6>:TxEN

1: Simultaneously enable the Tx timer (can be enabled even if T0EN, T1EN, T2EN, T3EN, T4EN are off)

0: Disable

Bit<5>:TCCCKS-TCC clock source selection

1: TCC clock selects Fosc (system clock)

0: TCC clock selects Fcpu (instruction clock)

Bit<4>:PWMWE-PWM Wake-up

1: PWM wake-up enable, can wake up idle mode

0: PWM wake-up disable

Bit<3>:TCCWE-TCC Wake-up

1: TCC wake-up enable, can wake up idle mode, can wake up sleep and idle mode in RTC mode

0: TCC wake-up disable

(In RTC mode, setting TCCWE=1&RTCS=1 will keep LXT working without stopping when sleeping, otherwise sleeping will stop LXT)

Bit<2>:STPHX-High Speed Clock

1: Stop high-speed clock, including IRC and crystal oscillator clock (excluding RTC clock)

0: High-speed clock is working normally

Bit<1>:CLKMD - System Clock

1: System clock uses low-speed RC oscillator clock

0: System clock uses high-speed IRC or crystal oscillator clock

(When the system enters low-speed mode from normal mode, first set CLKMD=1, then set STPHX=1,When the system enters normal mode from low-speed mode, first set STPHX=0, then set CLKMD=0)

Bit<0>:IDLE - Idle Mode

1: The system enters idle mode when executing the SLEEP instruction, and the system clock works normally

(TCC and PWM can continue to work in idle mode if the system clock is selected, and can wake up the system)

0: The system enters sleep mode when executing the SLEEP instruction

3.1.13 RPAGE～RF/ISR (Interrupt Flag Register)

0FH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR	PWM2IF	PWM1IF	PWM0IF	LVDIF	P5ICIF	EXIF	P6ICIF	TCIF
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:PWM2IF-PWM2 Period OverflowInterrupt Flag

1: Interrupt occurred

0: No interrupt

Bit<6>:PWM1IF-PWM1 Period OverflowInterrupt Flag

1: Interrupt occurred

0: No interrupt

Bit<5>:PWM0IF-PWM0 Period OverflowInterrupt Flag

1: Interrupt occurred

0: No interrupt

Bit<4>:LVDIF-LVD Status Change Interrupt Flag

1: Interrupt occurred (LVDF changes from 0 to 1 or from 1 to 0, set to 1, software clears to 0)

0: No interrupt

Bit<3>:P5ICIF-P5 Port Change Interrupt Flag

1: Interrupt occurred

0: No interrupt

Bit<2>:EXIF-External Interrupt Flag

1: Interrupt occurred (set to 1 by the falling edge on the INT pin, software clears to 0)

0: No interrupt

Bit<1>: P6ICIF - P6 port change interrupt flag

1: Interrupt occurred

0: No interrupt

Bit<0>: TCIF-TCC interrupt flag bit

1: Interrupt occurred

0: No interrupt

Note: When clearing the interrupt flag bit, you must use the MOV RF,A operation, and you cannot use the BTC and AND RF,A instruction operations.

3.1.14 RPAGE～R70/PWM0CR (PWM0 Control Register)

70H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0CR	T0EN	IPWM0EN	PWM0EN	PWM0CKS	T0PTEN	T0PSR<2>	T0PSR<1>	T0PSR<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:T0EN-PWM0 counter enable

1: Enable

0: Disable

Bit<6>:IPWM0EN

1:IPWM0 enabled (the corresponding port needs to be set as output to output PWM waveform)

0: Disabled

Bit<5>:PWM0EN

1:PWM0 enabled (the corresponding port needs to be set as output to output PWM waveform)

0: Disabled

Bit<4>:PWM0CKS

1: PWM0 clock selects Fosc (system clock)

0: PWM0 clock selects Fcpu (instruction clock)

Bit<3>:T0PTEN-T0 prescaler selection control bit

Bit<2:0>:T0PSR2~T0PSR0:

T0PTEN	T0PSR2	T0PSR1	T0PSR0	T0 prescaling factor
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32

1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.15 RPAGE～R71/PWM1CR (PWM1 Control Register)

71H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1CR	T1EN	IPWM1EN	PWM1EN	PWM1CKS	T1PTEN	T1PSR<2>	T1PSR<1>	T1PSR<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:T1EN-PWM1 Counter Enable

1: Enable

0: Disable

Bit<6>:IPWM1EN

1:IPWM1 enable (need to set the corresponding port to output to output PWM waveform)

0: Disabled

Bit<5>:PWM1EN

1: PWM1 enable (you need to set the corresponding port to output to output PWM waveform)

0: Disabled

Bit<4>: PWM1CKS

1: PWM1 clock selection Fosc

0: PWM1 clock selection Fcpu

Bit<3>: T1PTEN-T1 prescaler selection control bit

Bit<2:0>: T1PSR2~T1PSR0:

T1PTEN	T1PSR2	T1PSR1	T1PSR0	T1 division ratio
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.16 RPAGE～R72/PWM2CR (PWM2 Control Register)

72H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2CR	T2EN	IPWM2EN	PWM2EN	PWM2CKS	T2PTEN	T2PSR<2>	T2PSR<1>	T2PSR<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Value	0	0	0	0	0	0	0	0

Bit<7>:T2EN-PWM2 counter enable

1: Enable

0: Disable

Bit<6>:IPWM2EN

1: IPWM2 enable (need to set the corresponding port to output to output PWM waveform)

0: Disabled

Bit<5>:PWM2EN

1: PWM2 enable (need to set the corresponding port to output to output PWM waveform)

0: Disabled

Bit<4>:PWM2CKS

1: PWM2 clock selects Fosc (system clock)

0: PWM2 clock selects Fcpu (instruction clock)

Bit<3>:T2PTEN-T2 prescale selection control bit

Bit<2:0>:T2PSR2~T2PSR0:

T2PTEN	T2PSR2	T2PSR1	T2PSR0	T2 Frequency Division Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.17 RPAGE～R73/PWM3CR (PWM3 Control Register)

73H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3CR	T3EN	IPWM3EN	PWM3EN	PWM3CKS	T3PTEN	T3PSR<2>	T3PSR<1>	T3PSR<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:T3EN-PWM3 counter enable

1: Enable

0: Disable

Bit<6>:IPWM3EN

1: IPWM3 enable (need to set the corresponding port as output to output PWM waveform)

0: Disabled

Bit<5>:PWM3EN

1: PWM3 enable (need to set the corresponding port as output to output PWM waveform)

0: Disabled

Bit<4>:PWM3CKS

1: PWM3 clock selects Fosc (system clock)

0: PWM3 clock selects Fcpu (instruction clock)

Bit<3>: T3PTEN - T3 prescaler selection control bit

Bit<2:0>: T3PSR2~T3PSR0:

T3PTEN	T3PSR2	T3PSR1	T3PSR0	T3 prescale factor
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.18 RPAGE～R74/PWM4CR (PWM4 Control Register)

74H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM4CR	T4EN	IPWM4EN	PWM4EN	PWM4CKS	T4PTEN	T4PSR<2>	T4PSR<1>	T4PSR<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:T4EN-PWM4 counter enable

1: Enable

0: Disable

Bit<6>:IPWM4EN

1:IPWM4 Enable (requires setting the corresponding port as output to output PWM waveform)

0: Disabled

Bit<5>:PWM4EN

1: PWM4 enable (the corresponding port needs to be set as output to output PWM waveform)

0: Disabled

Bit<4>:PWM4CKS

1: PWM4 clock selects Fosc (system clock)

0: PWM4 clock selects Fcpu (instruction clock)

Bit<3>:T4PTEN-T4 prescale selection control bit

Bit<2:0>:T4PSR2~T4PSR0:

T4PTEN	T4PSR2	T4PSR1	T4PSR0	T4 frequency division coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.19 RPAGE～R75/P5HDCR (P5 High Current Control Register)

75H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5HDCR	P5HD<7>	P5HD<6>	P5HD<5>	P5HD<4>	P5HD<3>	P5HD<2>	P5HD<1>	P5HD<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P5 High Sink Current Control Bit

1: Enable

0: Disabled

3.1.20 RPAGE～R76/P5HSCR (P5 High Source Current Control Register)

76H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5HSCR	P5HS<7>	P5HS<6>	P5HS<5>	P5HS<4>	P5HS<3>	P5HS<2>	P5HS<1>	P5HS<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P5 High Slew Rate Current Control Bit

1: Enable

0: Disabled

3.1.21 RPAGE～R77/P6HDCR (P6 High Pull-up Current Control Register)

77H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HDCR	P6HD<7>	P6HD<6>	P6HD<5>	P6HD<4>	P6HD<3>	P6HD<2>	P6HD<1>	P6HD<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P6 High Slew Rate Current Control Bit
1: Enable
0: Disabled

3.1.22 RPAGE～R78/P6HSCR (P6 High Sink Current Control Register)

78H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HSCR	P6HS<7>	P6HS<6>	P6HS<5>	P6HS<4>	P6HS<3>	P6HS<2>	P6HS<1>	P6HS<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P6 high sink current control bit
1: Enable
0: Disabled

3.1.23 RPAGE～R79/P5WDCR (P5 Weak Pull-Down Current Control Register)

79H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5WDCR	P5WD<7>	P5WD<6>	P5WD<5>	P5WD<4>	P5WD<3>	P5WD<2>	P5WD<1>	P5WD<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P5 weak pull-down current control bit
1: Enable
0: Disabled

3.1.24 RPAGE～R7A/P5WSCR (P5 Weak Sinking Current Control Register)

7AH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5WSCR	P5WS<7>	P5WS<6>	P5WS<5>	P5WS<4>	P5WS<3>	P5WS<2>	P5WS<1>	P5WS<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P5 weak drain current control bit
1: Enable
0: Disabled

3.1.25 RPAGE～R7B/DEADCR (PWM Dead Zone Control Register)

7BH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit <2:0>		
DEADCR	DEADE<3>	DEADE<2>	DEADE<1>	DEADE<0>	DEADCKS	DEADP<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:4>:DEADEN<3:0>-PWM Dead Zone Enable Control Bit

DEADEN<0> PWM0 Dead Zone Enable Control Bit

DEADEN<1> PWM1 Dead Zone Enable Control Bit

DEADEN<2> PWM2 Dead Zone Enable Control Bit

DEADEN<2> PWM3 Dead Zone Enable Control Bit

0: Disable

1: Enable

Bit<3>:DEADCKS-PWM Dead Zone Clock Selection

1: Select Fosc as the dead zone clock

0: Select Fcpu as the dead zone clock

Bit<2:0>:DEADP-PWM Dead Zone Time Setting

DEADP<2>	DEADP<1>	DEADP<0>	Dead zone timing division coefficient
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

3.1.26 RPAGE～R7C/DEADTR (PWM Dead Zone Control Register)

7CH(R)	Bit <7:0>
DEADTR	DEADT<7:0>
Read/Write	R/W
Reset Value	0

Bit<7:0>:DEADT<7:0>-Dead Zone Timer

3.2 Control Register

3.2.1 CONT (Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTCS	INTE	TS	TE	PAB	PSR2	PSR1	PSR0

Bit<7>: RTCS-TCC signal source selection (OPTION option is valid when RTC function is enabled, otherwise bit7 is a general read-write bit)

When RTC is closed in OPTION, it acts as a general read-write bit;

When RTC is enabled in OPTION:

1:Select external crystal oscillator clock (LXT's 4 frequency division)

0:The TCC clock is determined by TCCCKS and TS. When TCCCKS=1, the clock source selects FOSC. When TCCCKS=0, the clock source is determined by TS. The TCC clock source priority is RTCS>TCCCKS>TS, and the SCT register is readable and writable.

Bit<6>:INTE - Global interrupt enable bit

1: Set bit 1 via EI/RETI

0: Clear to zero via DI or interrupt

Bit<5>:TS - TCC signal source selection bit

1: External input signal (P54 needs to be set as input port)

0: Internal instruction cycle clock as TCC clock source

Bit<4>:TE - TCC signal edge selection bit

1: TCC pin signal changes from high to low plus 1

0: TCC pin signal changes from low to high +1

Bit<3>: PAB - Prescaler Allocation Bit

1: WDT

0: TCC

Bit<2:0>:PSR<2:0> - Prescaler Selection Control Bit:

PSR2	PSR1	PSR0	TCC prescaling factor	WDT prescaling factor
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

CONT is a readable and writable register

3.2.2 IOPAGE～IOC5/P5CR (P5 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5CR<7>	P5CR<6>	P5CR<5>	P5CR<4>	P5CR<3>	P5CR<2>	P5CR<1>	P5CR<0>

Port5 direction control bit

1: Input

0: Output

3.2.3 IOPAGE～IOC6/P6CR (P6 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6CR<7>	P6CR<6>	P6CR<5>	P6CR<4>	P6CR<3>	P6CR<2>	P6CR<1>	P6CR<0>

Port6 direction control bit

1: Input (default)

0: Output

3.2.4 IOPAGE～IOC7/P7CR (P7 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P7CR<1:0>	

Bit<1:0>:P7CR<1:0>-P7 Direction Control Bit

1: Input (default)

0: Output

3.2.5 IOPAGE～IOC8/PHDCR0 (Pull-up/Pull-down Control Register 0)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P7PD<1>	P7PD<0>	-	-	P7PH<1>	P7PH<0>

Bit<5:4>:P7PD<1:0>-P7 Port Pull-down Enable Bit

Bit<1:0>:P7PH<1:0>-P7 Port Pull-up Enable Bit

0: Enable

1: Forbidden

3.2.6 IOPAGE～IOC9/PHDCR1 (Pull-up/Pull-down Control Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PD<7>	P6PD<6>	P6PD<5>	P6PD<4>	P5PH<3>	P5PH<2>	P5PH<1>	P5PH<0>

Bit<7:4>: Pull-down enable control bits for P6D<7:4>-P6<7:4> pins

Bit<3:0>: Pull-up enable control bits for P5H<3:0>-P5<3:0> pins

0: Internal pull-up/pull-down enabled

1: Internal pull-up/pull-down disabled

The PHDCR1 register is readable and writable

3.2.7 IOPAGE～IOCA/PHDCR2 (Pull-up/Pull-down Control Register 2)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	P5PD<6>	P5PD<5>	P5PD<4>	P5PH<7>	P5PH<6>	P5PH<5>	P5PH<4>

Bit<6:4>: Pull-down enable control bits for P5PD<6:4>-P5<6:4> pins

Bit<3:0>: Pull-up enable control bits for P5PH<7:4>-P5<7:4> pins

1: Internal pull-up/pull-down disabled
0: Internal pull-up/pull-down enabled

3.2.8 IOPAGE～IOCB/PDCR (Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PD<3:0>				P5PD<3:0>			

Bit<7:4>: Pull-down enable control bits for P6PD<3:0>-P6<3:0>
Bit<3:0>: Pull-down enable control bits for P5PD<3:0>-P5<3:0>
1: Forbidden
0: Enable

3.2.9 IOPAGE～IOCC/P6ODCR (P6 Open-Drain Output Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6OD<7>	P6OD<6>	P6OD<5>	P6OD<4>	P6OD<3>	P6OD<2>	P6OD<1>	P6OD<0>

Port6 port open-drain function control
1: Enable
0: Disabled (default)

3.2.10 IOPAGE～IOCD/P6PHCR (P6 port pull-up control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PH<7>	P6PH<6>	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>

Port6 port pull-up control
1: Disabled (default)
0: Enable

3.2.11 IOPAGE～IOCE/WDTCR (Watchdog Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTEN	EIS	INTEDG	ROC	1	1	1	1

Bit<7>:WDTEN-WDT Enable Control Bit
1: Enable
0: Disable
Bit<6>:EIS-P60 Pin External Interrupt Enable Control Bit
1: Enable
0: Disable
When the external interrupt pin is enabled, the I/O control bit of P60 (Bit0 of P6CR) must be set to “1”. When EIS is “0”, the EXINT channel is masked. When it is “1”, the status of the EXINT pin can be read by the P6 port.
Bit<5>:INTEDG-P60 Pin Rising/Falling Edge Function Enable Control
1: Opposite (rising edge triggered)
0: Default is consistent with the original (falling edge trigger)
Bit<4>:ROC-ROC-R function enable control

1: Enable, P5<1:0> weak pull-up enabled
0: Disabled (default)

When using the R-option function, a 430K resistor can be connected to ground on the P50 and P51 pins. If a resistor is connected, P50 and P51 are read as "0". If no resistor is connected, P50 and P51 are read as "1".

The watchdog register is readable and writable

3.2.12 IOPAGE~IOCF/IMR (Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2IE	PWM1IE	PWM0IE	LVDIE	P5ICIE	EXIE	P6ICIE	TCIE

Bit7:PWM2IE-PWM2 interrupt enable control bit
1: Enable
0: Disabled (default)
Bit6:PWM1IE-PWM1 interrupt enable control bit
1: Enable
0: Disabled (default)
Bit5:PWM0IE-PWM0 interrupt enable control bit
1: Enable
0: Disabled (default)
Bit4:LVDIE-LVD status change interrupt enable control bit
1: Enable
0: Disabled (default)
Note: LVD will enter interrupt when VDD voltage is higher than the set value or when VDD voltage is lower than the set value;
Bit3:P5ICIE-P5 port change interrupt enable control bit
1: Enable
0: Disabled (default)
Bit2:EXIE-External interrupt enable control bit
1: Enable
0: Disabled (default)
Bit1: P6ICIE - P6 port change interrupt enable control bit
1: Enable
0: Disabled (default)
Bit0: TCIE - TCC interrupt enable control bit
1: Enable
0: Disabled (default)
IOCF register is readable and writable

3.2.13 IOPAGE~IOC10/PRDCH0 (PWM0 Period Duty High Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD0<11>	PRD0<10>	PRD0<9>	PRD0<8>	PDC0<11>	PDC0<10>	PDC0<9>	PDC0<8>

Bit<7:4>:PRD0<11:8>-PWM0 Period High Bits

Bit<3:0>:PDC0<11:8>-PWM0 Duty Cycle High Bits

3.2.14 IOPAGE～IOC11/PRDL0 (PWM0 Period Low Bits Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD0<7>	PRD0<6>	PRD0<5>	PRD0<4>	PRD0<3>	PRD0<2>	PRD0<1>	PRD0<0>

Bit<7:0>:PRD0<7:0>- PWM0 period low byte

3.2.15 IOPAGE～IOC12/PDCL0 (PWM0 Duty Cycle Low Byte Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC0<7>	PDC0<6>	PDC0<5>	PDC0<4>	PDC0<3>	PDC0<2>	PDC0<1>	PDC0<0>

Bit<7:0>:PDC0<7:0>- PWM0 Duty Cycle Low Byte

3.2.16 IOPAGE～IOC13/PRDCH1 (PWM1 Period Duty Cycle High Byte Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1<11>	PRD1<10>	PRD1<9>	PRD1<8>	PDC1<11>	PDC1<10>	PDC1<9>	PDC1<8>

Bit<7:4>:PRD0<11:8>-PWM1 Period High Bits
Bit<3:0>:PDC0<11:8>-PWM1 Duty Cycle High Bits

3.2.17 IOPAGE～IOC14/PRDL1 (PWM1 Period Low Bits Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1<7>	PRD1<6>	PRD1<5>	PRD1<4>	PRD1<3>	PRD1<2>	PRD1<1>	PRD1<0>

Bit<7:0>:PRD0<7:0>- PWM1 Period Low Byte

3.2.18 IOPAGE～IOC15/PDCL1 (PWM1 Duty Cycle Low Byte Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC1<7>	PDC1<6>	PDC1<5>	PDC1<4>	PDC1<3>	PDC1<2>	PDC1<1>	PDC1<0>

Bit<7:0>:PDC0<7:0>- PWM1 Duty Cycle Low Byte

3.2.19 IOPAGE～IOC16/PRDCH2 (PWM2 Period Duty Cycle High Byte Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2<11>	PRD2<10>	PRD2<9>	PRD2<8>	PDC2<11>	PDC2<10>	PDC2<9>	PDC2<8>

Bit<7:4>:PRD2<11:8>-PWM2 period high bits
Bit<3:0>:PDC2<11:8>-PWM2 duty cycle high bits

3.2.20 IOPAGE～IOC17/PRDL2 (PWM2 Period Low Bits Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2<7>	PRD2<6>	PRD2<5>	PRD2<4>	PRD2<3>	PRD2<2>	PRD2<1>	PRD2<0>

Bit<7:0>:PRD2<7:0>-PWM2 Period Low Byte

3.2.21 IOPAGE～IOC18/PDCL2 (PWM2 Duty Cycle Low Byte Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC2<7>	PDC2<6>	PDC2<5>	PDC2<4>	PDC2<3>	PDC2<2>	PDC2<1>	PDC2<0>

Bit<7:0>:PDC2<7:0>- PWM2 duty cycle low byte

3.2.22 IOPAGE～IOC19/PRDCH3 (PWM3 Period Duty High Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD3<11>	PRD3<10>	PRD3<9>	PRD3<8>	PDC3<11>	PDC3<10>	PDC3<9>	PDC3<8>

Bit<7:4>:PRD3<11:8>-PWM3 period high bits
Bit<3:0>:PDC3<11:8>-PWM3 duty cycle high bits

3.2.23 IOPAGE～IOC1A/PRDL3 (PWM3 period low bits control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD3<7>	PRD3<6>	PRD3<5>	PRD3<4>	PRD3<3>	PRD3<2>	PRD3<1>	PRD3<0>

Bit<7:0>:PRD3<7:0>-PWM3 Period Low Byte

3.2.24 IOPAGE～IOC1B/PDCL3 (PWM3 Duty Cycle Low Byte Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC3<7>	PDC3<6>	PDC3<5>	PDC3<4>	PDC3<3>	PDC3<2>	PDC3<1>	PDC3<0>

Bit<7:0>:PDC3<7:0>- PWM3 duty cycle low byte

3.2.25 IOPAGE～IOC1C/PRDCH4 (PWM4 Period Duty High Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD4<11>	PRD4<10>	PRD4<9>	PRD4<8>	PDC4<11>	PDC4<10>	PDC4<9>	PDC4<8>

Bit<7:4>:PRD4<11:8>- High bits of PWM4 period
Bit<3:0>:PDC4<11:8>- PWM4 duty cycle high bits

3.2.26 IOPAGE～IOC1D/PRDL4 (PWM4 period low bits control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD4<7>	PRD4<6>	PRD4<5>	PRD4<4>	PRD4<3>	PRD4<2>	PRD4<1>	PRD4<0>

Bit<7:0>:PRD4<7:0>-PWM4 period low byte

3.2.27 IOPAGE～IOC1E/PDCL4 (PWM4 Duty Cycle Low Byte Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC4<7>	PDC4<6>	PDC4<5>	PDC4<4>	PDC4<3>	PDC4<2>	PDC4<1>	PDC4<0>

Bit<7:0>:PDC3<7:0>- PWM4 Duty Cycle Low Bits

3.2.28 IOPAGE～IOC1F/PWMSCR (PWM Mapping Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPWM4S	IPWM3S	IPWM2S<1:0>		IPWM1S<1:0>		IPWM0S<1:0>	

Bit<7>:IPWM4S-IPWM4 Mapping Bit:

IPWM4S	Mapping Port
0	P56
1	P57

Bit<6>:IPWM3S-IPWM3 Mapping Bit:

IPWM4S	Mapping Port
0	P55
1	P54

Bit<5:4>:IPWM2S<1:0>-IPWM2 Mapping Bit:

IPWM2S<1>	IPWM2S<0>	Mapping Port
0	0	P63
0	1	P50
1	0	P53

Bit<3:2>:IPWM1S<1:0>-IPWM1 mapping bits:

IPWM1S<1>	IPWM1S<0>	Mapping Port
0	0	P64
0	1	P51
1	0	P70

Bit<1:0>:IPWM0S<1:0>-IPWM0 mapping bits:

IPWM0S<1>	IPWM0S<0>	Mapping Port
0	0	P65
0	1	P71
1	0	P52

3.3 GPIO Functional Module

JZ8P2508 has 3 groups of bidirectional I/O ports, a total of 18 inputs, 18 outputs, and most I/Os can be reused for other functions;

18 programmable pull-up I/O pins: P50～P57, P60～P67, P70～P71;

17 programmable pull-down I/O pins: P50～P56, P60～P67, P70～P71;

16 programmable drive enhanced I/O pins: P50～P57, P60～P67; (The port drive enhancement level needs to be set in the burning option. P60, P61, P62, P66, P67 can be configured with four-level drive enhancement, and the remaining IO can be configured with one-level drive enhancement)

8 programmable weak drive I/O pins: P50～P57;

8 programmable open-drain I/O pins: P60～P67;

The port input characteristic table is as follows:

Port	EMT
P50-P57	0.28VDD
P60-P67	0.2VDD/0.4VDD
P70-P71	0.2VDD/0.4VDD

3.3.1 GPIO Register Description

RPAGE～R5 (PORT5 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	P53	P52	P51	P50

PORT5 data register, readable and writable

RPAGE～R6 (PORT6 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

PORT6 data register, readable and writable

RPAGE～R7 (PORT7 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P71	P70

PORT7 data register, readable and writable

Bit<1:0>:P7<1:0>-PORT7 Data Register

IOPAGE～IOC5/P5CR (P5 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5CR<7>	P5CR<6>	P5CR<5>	P5CR<4>	P5CR<3>	P5CR<2>	P5CR<1>	P5CR<0>

Port5 direction control bit

1: Input

0: Output

IOPAGE～IOC6/P6CR (P6 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6CR<7>	P6CR<6>	P6CR<5>	P6CR<4>	P6CR<3>	P6CR<2>	P6CR<1>	P6CR<0>

Port6 direction control bit

1: Input (default)

0: Output

IOPAGE～IOC7/P7CR (P7 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	P7CR<1:0>	

Bit<1:0>:P7CR<1:0>-P7 Direction Control Bit

1: Input (default)

0: Output

IOPAGE～IOC8/PHDCR0 (Pull-up/Pull-down Control Register 0)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P7PD<1>	P7PD<0>	-	-	P7PH<1>	P7PH<0>

Bit<5:4>:P7PD<1:0>-P7 Port Pull-down Enable Bit

Bit<1:0>:P7PH<1:0>-P7 Port Pull-up Enable Bit

1: Forbidden

0: Enable

IOPAGE～IOC9/PHDCR1 (Pull-up/Pull-down Control Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PD<7>	P6PD<6>	P6PD<5>	P6PD<4>	P5PH<3>	P5PH<2>	P5PH<1>	P5PH<0>

Bit<7:4>: Pull-down enable control bits for P6D<7:4>-P6<7:4> pins

Bit<3:0>: Pull-up enable control bits for P5H<3:0>-P5<3:0> pins

1: Internal pull-up/pull-down disabled

0: Internal pull-up/pull-down enabled

The PHDCR1 register is readable and writable

IOPAGE～IOCA/PHDCR2 (Pull-up/Pull-down Control Register 2)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	P5PD<6>	P5PD<5>	P5PD<4>	P5PH<7>	P5PH<6>	P5PH<5>	P5PH<4>

Bit<6:4>: Pull-down enable control bits for P5PD<6:4>-P5<6:4> pins

Bit<3:0>: Pull-up enable control bits for P5PH<7:4>-P5<7:4> pins

1: Internal pull-up/pull-down disabled

0: Internal pull-up/pull-down enabled

IOPAGE～IOCB/PDCR (Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PD<3:0>				P5PD<3:0>			

Bit<7:4>: Pull-down enable control bits for P6PD<3:0>-P6<3:0>
Bit<3:0>: Pull-down enable control bits for P5PD<3:0>-P5<3:0>
1: Forbidden
0: Enable

IOPAGE～IOCC (P6 Port Open-Drain Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6OD<7>	P6OD<6>	P6OD<5>	P6OD<4>	P6OD<3>	P6OD<2>	P6OD<1>	P6OD<0>

Port6 port open-drain function control
1: Enable
0: Disabled (default)

IOPAGE～IOCD/P6PHCR (P6 Port Pull-up Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PH<7>	P6PH<6>	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>

Port6 port pull-up control
1: Disabled (default)
0: Enable

RPAGE～R75/P5HDCR (P5 High Pull-up Current Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5HD<7>	P5HD<6>	P5HD<5>	P5HD<4>	P5HD<3>	P5HD<2>	P5HD<1>	P5HD<0>

Bit<7:0>:P5 High Sink Current Control Bit
1: Enable
0: Disabled

RPAGE～R76/P5HSCR (P5 High Sink Current Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5HS<7>	P5HS<6>	P5HS<5>	P5HS<4>	P5HS<3>	P5HS<2>	P5HS<1>	P5HS<0>

Bit<7:0>:P5 High Slew Rate Current Control Bit
1: Enable
0: Disabled

RPAGE～R77/P6HDCR (P6 High Pull-up Current Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HD<7>	P6HD<6>	P6HD<5>	P6HD<4>	P6HD<3>	P6HD<2>	P6HD<1>	P6HD<0>

Bit<7:0>:P6 High Slew Rate Current Control Bit
1: Enable
0: Disabled

RPAGE～R78/P6HSCR (P6 High Sink Current Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HS<7>	P6HS<6>	P6HS<5>	P6HS<4>	P6HS<3>	P6HS<2>	P6HS<1>	P6HS<0>

Bit<7:0>:P6 high sink current control bit

1: Enable

0: Disabled

RPAGE～R79/P5WDCR (P5 Weak Pull-up Current Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5WD<7>	P5WD<6>	P5WD<5>	P5WD<4>	P5WD<3>	P5WD<2>	P5WD<1>	P5WD<0>

Bit<7:0>:P5 weak pull-down current control bit

1: Enable

0: Disabled

RPAGE～R7A/P5WSCR (P5 Weak Current Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5WS<7>	P5WS<6>	P5WS<5>	P5WS<4>	P5WS<3>	P5WS<2>	P5WS<1>	P5WS<0>

Bit<7:0>:P5 weak drain current control bit

1: Enable

0: Disabled

3.4 TCC Timer Function Module

TCC is an 8-bit timer/counter. The TCC clock source can be selected from an internal clock or an external input signal (input from the TCC pin, and the trigger edge can be selected). If the internal clock is used as the TCC clock source, TCC increments by one every instruction cycle (no prescaler). The number of clock cycles per instruction cycle is determined by the number of CLKS selected in CODE OPTION. If TCC selects an external clock input as the TCC clock source, TCC will increment by 1 on each falling or rising edge input at the TCC pin.

3.4.1 TCC Timer Register Description

CONT (Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTCS	INTE	TS	TE	PAB	PSR2	PSR1	PSR0

Bit<5>:TS - TCC signal source selection bit
1: External input signal (P54 needs to be set as input port)
0: Internal instruction cycle clock as TCC clock source
Bit<4>:TE - TCC signal edge selection bit
1: TCC pin signal changes from high to low plus 1
0: TCC pin signal changes from low to high +1
Bit<3>: PAB - Prescaler Allocation Bit
1: WDT
0: TCC
Bit<2:0>:PSR<2:0> - Prescaler Selection Control Bit:

PSR2	PSR1	PSR0	TCC prescaling factor	WDT prescaling factor
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

CONT is a readable and writable register

RPAGE～R1 (TCC Data Counter)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC<7:0>							

TCC data register, readable and writable

RPAGE～RF (Interrupt Flag Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2IF	PWM1IF	PWM0IF	LVDIF	P5ICIF	EXIF	P6ICIF	TCIF

Bit<0>: TCIF-TCC interrupt flag bit

1: Interrupt occurred

0: No interrupt

The RF register is readable and writable, but can only be written with 0

Note: When clearing the interrupt flag bit, you must use the MOV RF,A operation, and you cannot use the BTC and AND RF,A instruction operations.

IOPAGF～IOCF (Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2IE	PWM1IE	PWM0IE	LVDIE	P5ICIE	EXIE	P6ICIE	TCIE

Bit<0>:TCIE-TCC Overflow Interrupt Enable Control Bit

1: Enable

0: Disabled (default)

IOCF register is readable and writable

3.4.2 TCC Timing Setting Description

1. Assign initial values to the TCC registers;

2. Set the value of the CONT register (select as timer or counter and prescale ratio);

3. When used as a counter, select the TCC external signal as positive or negative edge plus 1 in the CONT register;

4. If you need to execute the interrupt function, you must set TCIE (Bit0) in the IOCF register to 1 and execute the ENI instruction;

5. The interrupt program part needs to manually save the values of ACC, R3, and R4 registers. After executing the RETI instruction, clear the TCC interrupt flag before exiting the interrupt, and manually restore the saved values of ACC, R3, and R4 registers.

3.4.3 TCC Timing Calculation Description

The TCC timing function assigns an initial value to the timer by writing a value to the TCC register. The timer accumulates from the initial value position until the timer overflows and generates a Th interrupt.

TCC timing time calculation formula (select internal instruction cycle clock):

TCC timing time = (system clock division / FOSC) * TCC division * (256 - TCC initial value)

Example:

System clock division = 2clocks, Fosc = 8Mhz, TCC division = 4 division, TCC initial value = 156;

Then TCC timing time = (2/8) * 4 * (256-156) = 100us

TCC timing time calculation formula (when selecting external input clock):

TCC timing time = (external input clock) * TCC frequency division * (256 - TCC initial value)

Example:

External input clock = 1Mhz, TCC frequency division = 4 frequency division, TCC initial value = 156;

Then TCC timing time = 1 * 4 * (256-156) = 400us

3.5 WDT Watchdog Function Module

WDT has a free-running on-chip RC oscillator. When the CUP clock is turned off (i.e., sleep mode), the WDT can continue to run. Whether in normal mode or sleep mode, WDT timing overflow will reset the MCU (if WTD is enabled). WDT can be disabled or enabled by software in normal mode.

If you want to enable the WDT function, you must first select Enable in the WDT bit of the Code Option register, and then select "1" in the WDTEN bit in the WDT control register. Both conditions are indispensable.

3.5.1 WDT Watchdog Register Description

CONT (Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTCS	INTE	TS	TE	PAB	PSR2	PSR1	PSR0

Bit<3>: PAB - Prescaler Allocation Bit

1: WDT

0: TCC

Bit<2:0>:PSR<2:0> - Prescaler Selection Control Bit:

PSR2	PSR1	PSR0	TCC prescaling factor	WDT prescaling factor
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

CONT is a readable and writable register

IOPAGE～IOCE/WDCTR(Watchdog Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTEN	EIS	INTEDG	ROC	1	1	1	1

Bit<7>:WDTEN-WDT Enable Control Bit

1: Enable

0: Disabled (default)

The watchdog register is readable and writable

3.5.2 WDT Watchdog Setting Instructions

WDT watchdog overflow wake-up reset

1. Set Bit7 (WDTEN) in the IOCE register to select whether to use WDT;
2. Set the prescale coefficient, that is, set Bit3～Bit0 of the CONT register;

3. In the OPTION settings, enable the watchdog option;

4. When the WDT overflow wakes up, the system enters the reset state.

Note: When the WDT overflow wake-up interrupt uses the counting function, the WDT prescaler must be greater than 1:1;

3.6 Port State Change Wake-up Function Module

3.6.1 Sleep Wake-up Mode Description

The chip can enter sleep mode (low power mode) by executing the "SLEEP" instruction. When entering sleep mode, the system clock stops, all modules stop working, and the WDT (if enabled) is cleared to 0, but continues to run.

The microcontroller can be woken up by the following:

1. RST pin inputs a low level to wake up;
2. WDT overflow wake-up;
3. Port status change wake-up;
4. LVD low voltage detection wake-up;
5. External pin interrupt wake-up;

The first two types of wake-up cause the system to perform a reset, thus terminating all programs executed before sleep.

The latter three wake-up methods maintain the continuity of the program, and can choose to continue the original process (DISI executed before SLEEP) or execute the corresponding jump (ENI executed before SLEEP) through the program, and open the corresponding enable control bit to jump to the position of the interrupt vector. This module mainly describes port change wake-up, and other wake-up methods will be described in the corresponding modules.

3.6.2 Port Status Change Wake-up Register Description

RPAGE~RC/P5ICECR (P5 Input Status Change Interrupt Enable Register)

0CH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5ICECR	P5WK<7>	P5WK<6>	P5WK<5>	P5WK<4>	P5WK<3>	P5WK<2>	P5WK<1>	P5WK<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P5WK<7:0>-P5 Input Status Change Interrupt Enable Control Bit

1: Enable

0: Disable (default)

Note: In the OPTION port wake-up setting selection, if you select P5/P6 port non-independent control, the port wake-up is not controlled by the RC register. Otherwise, the RC register needs to be processed, otherwise the port cannot be woken up.

RPAGE～RD/P6ICECR (P6 Input Status Change Interrupt Enable Register)

0DH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6ICECR	P6WK<7>	P6WK<6>	P6WK<5>	P6WK<4>	P6WK<3>	P6WK<2>	P6WK<1>	P6WK<0>
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>:P6WK<7:0>-P6 input state change interrupt enable control bit

1: Enable

0: Disable (default)

Note: In the OPTION port wake-up setting selection, if you select P5/P6 port non-independent control, the port wake-up is not controlled by the RD register, otherwise the RD register needs to be processed, otherwise the port cannot be woken up.

RPAGE～RF/ISR (Interrupt Flag Register)

0FH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR	PWM2IF	PWM1IF	PWM0IF	LVDIF	P5ICIF	EXIF	P6ICIF	TCIF
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<3>:P5ICIF-P5 Port Change Interrupt Flag

1: Interrupt occurred

0: No interrupt

Bit<1>: P6ICIF - P6 port change interrupt flag

1: Interrupt occurred

0: No interrupt

Note: When clearing the interrupt flag bit, you must use the MOV RF,A operation, and you cannot use the BTC and AND RF,A instruction operations.

IOPAGE～IOCF/IMR (Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2IE	PWM1IE	PWM0IE	LVDIE	P5ICIE	EXIE	P6ICIE	TCIE

Bit3:P5ICIE-P5 port change interrupt enable control bit

1: Enable

0: Disabled (default)

Bit1: P6ICIE - P6 port change interrupt enable control bit

1: Enable

0: Disabled (default)

IOCF register is readable and writable

3.6.3 Port State Change Query Method Wake-up Setting

1. Set the PORT port wake-up port as input;
2. You can select the internal pull-up or pull-down of the wake-up port as needed;
3. The WDT prescaler setting must be greater than 1:1, and WDT is prohibited;
4. Enable PORT port state change interrupt;
5. Enable independent interrupt and wake-up control of port state change;
6. Execute the DISI instruction without entering the interrupt address port;
7. Read the PORT port (such as MOV 0X06,0X06);
8. Execute the "SLEP" instruction to enter the sleep SLEEP mode;
9. After waking up, execute the next instruction of SLEP.

3.6.4 Wake-up Setting by Port Status Change Interrupt

1. Set the PORT port wake-up port as input;
2. You can select the internal pull-up/pull-down of the wake-up port as needed;
3. The WDT prescaler setting must be greater than 1:1, and WDT is prohibited;
4. Enable independent interrupt and wake-up control for port status change;
5. Enable PORT port status change interrupt;
6. Execute the "ENI" instruction and wait to enter the interrupt address port;
7. Read the PORT port (such as MOV 0X06,0X06);
8. Execute the "SLEP" instruction to enter the sleep SLEEP mode;
9. After waking up, it will enter the interrupt address port. After exiting the interrupt, execute the next instruction of SLEP.

3.7 LVD Voltage Detection Function Module

The JZ8P2508 has a low voltage detection (LVD) function. A total of 28 voltage values can be programmed. When the CPU's operating voltage drops to the set value, Bit6 of the RPAGE-R8 register is set to 1. When the CPU's operating voltage rises from below the set value to above the set value, Bit6 of the RPAGE-R8 register is set to 0.

3.7.1 LVD Voltage Detection Register Description

RPAGE～R8/LVDCON (LVD Control Register)

08H(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDCON	LVDEN	LVDF	EXVEN	LVDSEL<4:0>				
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>:LVDEN

1: LVD Enable

0: LVD Disable

Bit<6>:LVDF

1: LVD is lower than the preset voltage point

0: LVD is higher than the preset voltage point

Bit<5>:EXVEN

1: LVD detection voltage selects P57 port input

0: LVD detection voltage selects VDD

LVDSEL<4:0>:

LVDSEL<4>	LVDSEL<3>	LVDSEL<2>	LVDSEL<1>	LVDSEL<0>	Voltage
0	0	0	0	0	2.0v
0	0	0	0	1	2.1v
0	0	0	1	0	2.2v
0	0	0	1	1	2.3v
0	0	1	0	0	2.4v
0	0	1	0	1	2.5v
0	0	1	1	0	2.6v
0	0	1	1	1	2.7v
0	1	0	0	0	2.8v
0	1	0	0	1	2.9v
0	1	0	1	0	3.0v
0	1	0	1	1	3.1v
0	1	1	0	0	3.2v
0	1	1	0	1	3.3v
0	1	1	1	0	3.4v
0	1	1	1	1	3.5v

1	0	0	0	0	3.6v
1	0	0	0	1	3.7v
1	0	0	1	0	3.8v
1	0	0	1	1	3.9v
1	0	1	0	0	4.0v
1	0	1	0	1	4.1v
1	0	1	1	0	4.2v
1	0	1	1	1	4.3v
1	1	0	0	0	4.4v
1	1	0	0	1	4.5v
1	1	0	1	0	4.6v
1	1	0	1	1	4.7v

RPAGE～RF/ISR (Interrupt Flag Register)

0FH(R)	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR	PWM2IF	PWM1IF	PWM0IF	LVDIF	P5ICIF	EXIF	P6ICIF	TCIF
Read/ Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<4>:LVDIF-LVD Status Change Interrupt Flag

1: Interrupt occurred (LVDF changes from 0 to 1 or from 1 to 0, set to 1, software clears to 0)

0: No interrupt

The RF register is readable and writable, but can only be written with 0

Note: When clearing the interrupt flag bit, you must use the MOV RF,A operation, and you cannot use the BTC and AND RF,A instruction operations.

IOPAGE～IOCF/IMR (Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2IE	PWM1IE	PWM0IE	LVDIE	P5ICIE	EXIE	P6ICIE	TCIE

Bit4:LVDIE-LVD status change interrupt enable control bit

1: Enable

0: Disabled (default)

Note: LVD will enter interrupt when VDD voltage is higher than the set value or when VDD voltage is lower than the set value;

IOCF register is readable and writable

3.7.2 LVD Voltage Detection Query Method Setting Instructions

1. Set the voltage value of LVD (LVDSEL<4>-LVDSEL<0> bits of RPAGE~R8 register);
2. Set the LVD detection port (EXVEN bit of RPAGE~R8 register);
3. Enable the LVD function (LVDEN bit of RPAGE~R8 register);

4. Use the MOV instruction to read the value of the RPAGE~R8 register and assign it to the general-purpose register;

5. Determine the LVDF bit of the RPAGE~R8 register in the general-purpose register and execute the corresponding action.

3.8 PWM Pulse Width Modulation Function Module

The JZ8P2508 has 5 built-in counters with prescalers to generate pulse width modulation signals, all with 12-bit precision. The PWM output waveform is determined by the period and duty cycle, and the transmission rate is the reciprocal of the period.

PWM0, PWM1, and PWM2 have period overflow interrupts, which can be configured in the interrupt enable control register (IMR) to jump to the interrupt after being enabled.

PWM0, PWM1, PWM2, and PWM3 have dead-time control and complementary output functions, which can be configured in the PWM mapping register (PWMSCR) to map the corresponding IPWM output port. The PWM dead-time control register (DEADCR) and PWM dead-time timer register (DEADTR) configure dead-time enable and dead-time timing.

PWM0, PWM1, PWM2, PWM3, and PWM4 all have wake-up functions. In IDLE mode, when PWM selects PWMCKS=1 in the CPU mode control register (CPUCON) and enables PWMWE, the system can be woken up after a cycle overflow.

3.8.1 PWM Pulse Width Modulation Register Description

RPAGE～R70/PWM0CR (PWM0 Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T0EN	IPWM0EN	PWM0EN	PWM0CKS	T0PTEN	T0PSR<2>	T0PSR<1>	T0PSR<0>

Bit<7>:T0EN-PWM0 counter enable

1: Enable

0: Disable

Bit<6>:IPWM0EN

1:IPWM0 enabled (the corresponding port needs to be set as output to output PWM waveform)

0: Disabled

Bit<5>:PWM0EN

1:PWM0 enabled (the corresponding port needs to be set as output to output PWM waveform)

0: Disabled

Bit<4>:PWM0CKS

1: PWM0 clock selects Fosc

0: PWM0 clock selects Fcpu

Bit<3>:T0PTEN-T0 prescaler selection control bit

Bit<2:0>:T0PSR2~T0PSR0:

T0PTEN	T0PSR2	T0PSR1	T0PSR0	T0 prescaling factor
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4

1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

RPAGE～R71/PWM1CR (PWM1 Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1EN	IPWM1EN	PWM1EN	PWM1CKS	T1PTEN	T1PSR<2>	T1PSR<1>	T1PSR<0>

Bit<7>:T1EN-PWM1 Counter Enable

1: Enable

0: Disable

Bit<6>:IPWM1EN

1:IPWM1 enable (need to set the corresponding port to output to output PWM waveform)

0: Disabled

Bit<5>:PWM1EN

1: PWM1 enable (you need to set the corresponding port to output to output PWM waveform)

0: Disabled

Bit<4>: PWM1CKS

1: PWM1 clock selection Fosc

0: PWM1 clock selection Fcpu

Bit<3>: T1PTEN-T1 prescaler selection control bit

Bit<2:0>: T1PSR2~T1PSR0:

T1PTEN	T1PSR2	T1PSR1	T1PSR0	T1 division ratio
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

RPAGE～R72/PWM2CR (PWM2 Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2EN	IPWM2EN	PWM2EN	PWM2CKS	T2PTEN	T2PSR<2>	T2PSR<1>	T2PSR<0>

Bit<7>:T2EN-PWM2 counter enable

1: Enable

0: Disable

Bit<6>:IPWM2EN

1: IPWM2 enable (need to set the corresponding port to output to output PWM waveform)

0: Disabled

Bit<5>:PWM2EN

1: PWM2 enable (need to set the corresponding port to output to output PWM waveform)

0: Disabled

Bit<4>:PWM2CKS

1: PWM2 clock selects Fosc

0: PWM2 clock selects Fcpu

Bit<3>:T2PTEN-T2 prescale selection control bit

Bit<2:0>:T2PSR2~T2PSR0:

T2PTEN	T2PSR2	T2PSR1	T2PSR0	T2 Frequency Division Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

RPAGE～R73/PWM3CR (PWM3 Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T3EN	IPWM3EN	PWM3EN	PWM3CKS	T3PTEN	T3PSR<2>	T3PSR<1>	T3PSR<0>

Bit<7>:T3EN-PWM3 counter enable

1: Enable

0: Disable

Bit<6>:IPWM3EN

1: IPWM3 enable (need to set the corresponding port as output to output PWM waveform)

0: Disabled

Bit<5>:PWM3EN

1: PWM3 enable (need to set the corresponding port as output to output PWM waveform)

0: Disabled

Bit<4>:PWM3CKS

1: PWM3 clock selects Fosc

0: PWM3 clock selects Fcpu

Bit<3>: T3PTEN - T3 prescaler selection control bit

Bit<2:0>: T3PSR2~T3PSR0:

T3PTEN	T3PSR2	T3PSR1	T3PSR0	T3 prescale factor
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

RPAGE～R74/PWM4CR (PWM4 Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T4EN	IPWM4EN	PWM4EN	PWM4CKS	T4PTEN	T4PSR<2>	T4PSR<1>	T4PSR<0>

Bit<7>:T4EN-PWM4 counter enable

1: Enable

0: Disable

Bit<6>:IPWM4EN

1:IPWM4 Enable (requires setting the corresponding port as output to output PWM waveform)

0: Disabled

Bit<5>:PWM4EN

1: PWM4 enable (the corresponding port needs to be set as output to output PWM waveform)

0: Disabled

Bit<4>:PWM4CKS

1: PWM4 clock selects Fosc

0: PWM4 clock selects Fcpu

Bit<3>:T4PTEN-T4 prescale selection control bit

Bit<2:0>:T4PSR2~T4PSR0:

T4PTEN	T4PSR2	T4PSR1	T4PSR0	T4 frequency division coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

RPAGE～R7B/DEADCR (PWM Dead Time Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEADE<3>	DEADE<2>	DEADE<1>	DEADE<0>	DEADCKS	DEADP<2>	DEADP<1>	DEADP<0>

Bit<7:4>:DEADEN<3:0>-PWM Dead Zone Enable Control Bit
DEADEN<0> PWM0 Dead Zone Enable Control Bit
DEADEN<1> PWM1 Dead Zone Enable Control Bit
DEADEN<2> PWM2 Dead Zone Enable Control Bit
DEADEN<2> PWM3 Dead Zone Enable Control Bit
1: Enable
0: Disable
Bit<3>:DEADCKS-PWM Dead Zone Clock Selection
1: Select Fosc as the dead zone clock
0: Select Fcpu as the dead zone clock
Bit<2:0>:DEADP-PWM Dead Zone Time Setting

DEADP<2>	DEADP<1>	DEADP<0>	Dead zone timing division coefficient
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

RPAGE～R7C/DEADTR (PWM Dead Time Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEADT<7>	DEADT<6>	DEADT<5>	DEADT<4>	DEADT<3>	DEADT<2>	DEADT<1>	DEADT<0>

Bit<7:0>:DEADT<7:0>-Dead Zone Timer

IOPAGE～IOC10/PRDCH0 (PWM0 period duty cycle high-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD0<11>	PRD0<10>	PRD0<9>	PRD0<8>	PDC0<11>	PDC0<10>	PDC0<9>	PDC0<8>

Bit<7:4>:PRD0<11:8>-PWM0 Period High Bits
Bit<3:0>:PDC0<11:8>-PWM0 Duty Cycle High Bits

IOPAGE～IOC11/PRDL0 (PWM0 period low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD0<7>	PRD0<6>	PRD0<5>	PRD0<4>	PRD0<3>	PRD0<2>	PRD0<1>	PRD0<0>

Bit<7:0>:PRD0<7:0>- PWM0 period low byte

IOPAGE～IOC12/PDCL0 (PWM0 duty cycle low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC0<7>	PDC0<6>	PDC0<5>	PDC0<4>	PDC0<3>	PDC0<2>	PDC0<1>	PDC0<0>

Bit<7:0>:PDC0<7:0>- PWM0 Duty Cycle Low Byte

IOPAGE～IOC13/PRDCH1 (PWM1 period duty cycle high-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1<11>	PRD1<10>	PRD1<9>	PRD1<8>	PDC1<11>	PDC1<10>	PDC1<9>	PDC1<8>

Bit<7:4>:PRD0<11:8>-PWM1 Period High Bits
Bit<3:0>:PDC0<11:8>-PWM1 Duty Cycle High Bits

IOPAGE～IOC14/PRDL1 (PWM1 period low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1<7>	PRD1<6>	PRD1<5>	PRD1<4>	PRD1<3>	PRD1<2>	PRD1<1>	PRD1<0>

Bit<7:0>:PRD0<7:0>- PWM1 Period Low Byte

IOPAGE～IOC15/PDCL1 (PWM1 duty cycle low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC1<7>	PDC1<6>	PDC1<5>	PDC1<4>	PDC1<3>	PDC1<2>	PDC1<1>	PDC1<0>

Bit<7:0>:PDC0<7:0>- PWM1 Duty Cycle Low Byte

IOPAGE～IOC16/PRDCH2 (PWM2 Period Duty High-Order Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2<11>	PRD2<10>	PRD2<9>	PRD2<8>	PDC2<11>	PDC2<10>	PDC2<9>	PDC2<8>

Bit<7:4>:PRD2<11:8>-PWM2 period high bits
Bit<3:0>:PDC2<11:8>-PWM2 duty cycle high bits

IOPAGE～IOC17/PRDL2 (PWM2 period low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2<7>	PRD2<6>	PRD2<5>	PRD2<4>	PRD2<3>	PRD2<2>	PRD2<1>	PRD2<0>

Bit<7:0>:PRD2<7:0>-PWM2 Period Low Byte

IOPAGE～IOC18/PDCL2 (PWM2 duty cycle low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC2<7>	PDC2<6>	PDC2<5>	PDC2<4>	PDC2<3>	PDC2<2>	PDC2<1>	PDC2<0>

Bit<7:0>:PDC2<7:0>- PWM2 duty cycle low byte

IOPAGE～IOC19/PRDCH3 (PWM3 period duty cycle high-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD3<11>	PRD3<10>	PRD3<9>	PRD3<8>	PDC3<11>	PDC3<10>	PDC3<9>	PDC3<8>

Bit<7:4>:PRD3<11:8>-PWM3 period high bits
Bit<3:0>:PDC3<11:8>-PWM3 duty cycle high bits

IOPAGE～IOC1A/PRDL3 (PWM3 period low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD3<7>	PRD3<6>	PRD3<5>	PRD3<4>	PRD3<3>	PRD3<2>	PRD3<1>	PRD3<0>

Bit<7:0>:PRD3<7:0>-PWM3 Period Low Byte

IOPAGE～IOC1B/PDCL3 (PWM3 duty cycle low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC3<7>	PDC3<6>	PDC3<5>	PDC3<4>	PDC3<3>	PDC3<2>	PDC3<1>	PDC3<0>

Bit<7:0>:PDC3<7:0>- PWM3 duty cycle low byte

IOPAGE～IOC1C/PRDCH4 (PWM4 period duty cycle high-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD4<11>	PRD4<10>	PRD4<9>	PRD4<8>	PDC4<11>	PDC4<10>	PDC4<9>	PDC4<8>

Bit<7:4>:PRD4<11:8>- High bits of PWM4 period
Bit<3:0>:PDC4<11:8>- PWM4 duty cycle high bits

IOPAGE～IOC1D/PRDL4 (PWM4 period low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD4<7>	PRD4<6>	PRD4<5>	PRD4<4>	PRD4<3>	PRD4<2>	PRD4<1>	PRD4<0>

Bit<7:0>:PRD4<7:0>-PWM4 period low byte

IOPAGE～IOC1E/PDCL4 (PWM4 duty cycle low-order control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC4<7>	PDC4<6>	PDC4<5>	PDC4<4>	PDC4<3>	PDC4<2>	PDC4<1>	PDC4<0>

Bit<7:0>:PDC3<7:0>- PWM4 Duty Cycle Low Bits

IOPAGE～IOC1F/PWMSCR (PWM mapping control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPWM4S	IPWM3S	IPWM2S<1:0>		IPWM1S<1:0>		IPWM0S<1:0>	

Bit<7>:IPWM4S-IPWM4 Mapping Bit:

IPWM4S	Mapping Port
0	P56

1	P57

Bit<6>:IPWM3S-IPWM3 Mapping Bit:

IPWM4S	Mapping Port
0	P55
1	P54

Bit<5:4>:IPWM2S<1:0>-IPWM2 Mapping Bit:

IPWM2S<1>	IPWM2S<0>	Mapping Port
0	0	P63
0	1	P50
1	0	P53

Bit<3:2>:IPWM1S<1:0>-IPWM1 mapping bits:

IPWM1S<1>	IPWM1S<0>	Mapping Port
0	0	P64
0	1	P51
1	0	P70

Bit<1:0>:IPWM0S<1:0>-IPWM0 mapping bits:

IPWM0S<1>	IPWM0S<0>	Mapping Port
0	0	P65
0	1	P71
1	0	P52

3.8.2 PWM pulse width modulation setting instructions

1. Set the PWMxCR register, select the corresponding timer for PWM mode, the prescaler of the timer, the timer interrupt type (if PWM interrupt is enabled), the clock source of the timer, etc.
2. Write the values of PRDCHx and PRDLx registers to determine the period of the PWM channel.
3. Write the values of PRDCHx and PDCLx registers to determine the duty cycle of the PWM channel.
4. Enable the corresponding timer.
5. Enable or disable the timer interrupt corresponding to PWM, and input “ENI” or “DISI” instruction (if needed).

3.8.3 PWM Pulse Width Modulation Calculation Description

PWM period calculation formula:

PWM period = PRD * (1/Fosc) * (Tx division) - PWM clock source selects Fosc

PWM period = PRD * (1/Fosc) * clock division * (Tx division) - PWM clock source selects Fcpu

Example:

PRD=100, Fosc=8Mhz, Tx division selects 2 division, clock division 2 division;

PWM period = 100 * (1/8) * 2 = 25us - PWM clock source selects Fosc

PWM period = 100 * (1/8) * 2 * 2 = 50us - PWM clock source selects Fcpu

Duty cycle calculation is the same as above.

3.8.4 PWM Dead Time Control Settings

JZ8P2508 PWM has dead time control and complementary output functions. The dead time and complementary output IO ports can be freely set by configuring R7B- DEADCR, R7C -DEADCR, IOCF1- PWMSCR registers.

PWM0, PWM1, PWM2, and PWM3 have dead time control functions. The dead time control of the corresponding PWM can be enabled by configuring bit<7:4> of the dead time control register R7B. By configuring bit<2:0> of the dead time control register R7B, the dead time clock division option of the PWM is selected. By configuring bit<3> of R7B, the dead time clock input source is selected as Fosc or Fcpu. By assigning the R7C bit<7:0> of the PWM dead time register, the counting time of the PWM dead time counter is set. When the value of the dead time counter is equal to the value of the dead time register (R7C - DEADTR), the original high and low level conversion of the PWM is executed, that is, the PWM dead time is realized.

The corresponding mapping output port of IPWM is controlled by configuring the IOCF1- PWMSCR register. The bit<7> bit of the PWMSCR register configures the output port of IPWM4, the bit<6> bit configures the output port of IPWM3, the bit<5:4> bit configures the output port of IPWM2, the bit<3:2> bit configures the output port of IPWM1, and the bit<1:0> bit configures the output port of IPWM0. The IPWM4 port is only the inverted output of PWM4 and does not have a dead time control function. The ports of other IPWMs can be used as complementary output ports in conjunction with the dead time.

3.9 Interrupt Function Module

JZ8P2508 has 8 interrupt sources. No matter which interrupt is used, the global interrupt must be enabled, that is, the "ENI" instruction. The interrupt vector address is a fixed address 008H. The following are the characteristics, interrupt address and priority level of each interrupt:

	Interrupt source	Enable condition	Interrupt flag	Interrupt vector
Internal	TCC overflow interrupt	ENI + TCIE = 1	TCIF	008H
External	P6 port change interrupt	ENI + P6ICIE = 1	P6ICIF	008H
External	External interrupt	ENI + EXIE = 1	EXIF	008H
External	P5 port change interruption	ENI + P5ICIE = 1	P5ICIF	008H
External	Low voltage detection interrupt	ENI + LVDIE = 1	LVDIF	008H
Internal	PWM0 cycle overflow interrupt	ENI + PWM0IE = 1	PWM0IF	008H
Internal	PWM1 cycle overflow interrupt	ENI + PWM1IE = 1	PWM1IF	008H
Internal	PWM2 cycle overflow interrupt	ENI + PWM2IE = 1	PWM2IF	008H

RPAGE～RF are interrupt status flag registers, which record the interrupt flag bits after an interrupt request is generated. PRAGE～RE, IOPAGF～IOCF are interrupt setting registers, and the enabling and disabling of interrupts are set in these 2 registers. The enabling of the global interrupt is done through the "ENI" instruction, and conversely, the disabling of the global interrupt is done through the "DISI" instruction. When an interrupt occurs, the execution of its next instruction will be executed from their specific address. The corresponding interrupt flag bit must be cleared before leaving the interrupt service routine to avoid malfunction of the interrupt.

When executing an interrupt subroutine, the contents of ACC, R3, and R4 need to be manually saved until after exiting the interrupt subroutine, when the saved values need to be manually loaded into ACC, R3, and R4. This is to prevent the values of ACC, R3, and R4 from being changed while executing the interrupt subroutine, which could cause errors when returning to the main program.

3.9.1 Interrupt Register Description

RPAGE～RF/ISR(Interrupt Flag Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2IF	PWM1IF	PWM0IF	LVDIF	P5ICIF	EXIF	P6ICIF	TCIF

Bit<7>:PWM2IF-PWM2 Period OverflowInterrupt Flag
1: Interrupt occurred
0: No interrupt
Bit<6>:PWM1IF-PWM1 Period OverflowInterrupt Flag
1: Interrupt occurred
0: No interrupt
Bit<5>:PWM0IF-PWM0 Period OverflowInterrupt Flag
1: Interrupt occurred
0: No interrupt
Bit<4>:LVDIF-LVD Status Change Interrupt Flag
1: Interrupt occurred (LVDF changes from 0 to 1 or from 1 to 0, set to 1, software clears to 0)
0: No interrupt
Bit<3>:P5ICIF-P5 Port Change Interrupt Flag
1: Interrupt occurred
0: No interrupt
Bit<2>:EXIF-External Interrupt Flag
1: Interrupt occurred (set to 1 by the falling edge on the INT pin, software clears to 0)
0: No interrupt
Bit<1>: P6ICIF - P6 port change interrupt flag
1: Interrupt occurred
0: No interrupt
Bit<0>: TCIF-TCC interrupt flag bit
1: Interrupt occurred
0: No interrupt
The RF register is readable and writable, but can only be written with 0
Note: When clearing the interrupt flag bit, you must use the MOV RF,A operation, and you cannot use the BTC and AND RF,A instruction operations.

IOPAGE～IOCF/IMR(Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2IE	PWM1IE	PWM0IE	LVDIE	P5ICIE	EXIE	P6ICIE	TCIE

Bit7:PWM2IE-PWM2 interrupt enable control bit
1: Enable
0: Disabled (default)
Bit6:PWM1IE-PWM1 interrupt enable control bit
1: Enable
0: Disabled (default)
Bit5:PWM0IE-PWM0 interrupt enable control bit

1: Enable
0: Disabled (default)

Bit4:LVDIE-LVD status change interrupt enable control bit
1: Enable
0: Disabled (default)

Note: LVD will enter interrupt when VDD voltage is higher than the set value or when VDD voltage is lower than the set value;

Bit3:P5ICIE-P5 port change interrupt enable control bit
1: Enable
0: Disabled (default)

Bit2:EXIE-External interrupt enable control bit
1: Enable
0: Disabled (default)

Bit1: P6ICIE - P6 port change interrupt enable control bit
1: Enable
0: Disabled (default)

Bit0: TCIE - TCC interrupt enable control bit
1: Enable
0: Disabled (default)

IOCF register is readable and writable

3.9.2 External Interrupt Setup Instructions

1. Set the interrupt as an input port and configure the interrupt port as an input;
2. Set the RIEN register interrupt port;
3. Enable external interrupt EXIE=1;
4. Enable ENI if you need to enter the interrupt according to customer needs, and disable DISI if you do not enter the interrupt;

Other interrupt descriptions are provided in the corresponding modules.

3.10 Reset Function Module

3.10.1 Reset Function Overview

The JZ8P2508 system provides 3 reset methods:

1. Power-on reset and low-voltage reset;
2. RESET pin input low-level reset;
3. WDT watchdog overflow reset;

The first reset time is determined by the reset time selection in OPTION, as shown in the table below:

Power-on reset setup time:

SUT	Reset setup time
PWRT=WDT=18ms	Power-up reset time = 18ms
PWRT=WDT=4.5ms	Power-up reset time = 4.5ms
PWRT=WDT=72ms	Power-up reset time = 72ms
PWRT=WDT=288ms	Power-up reset time = 288ms
PWRT=140us WDT=18ms	Power-up reset time =140us
PWRT=140us WDT=4.5ms	Power-up reset time =140us
PWRT=140us WDT=72ms	Power-up reset time =140us
PWRT=140us WDT=288ms	Power-up reset time =140us

When any of the above resets occur, all system registers return to their default state, the program stops running, and the program counter PC is cleared. After the reset, the system restarts from vector 0000H.

Any type of reset requires a certain response time, and the system provides a complete reset process to ensure the smooth execution of the reset action. The time required to complete the reset varies for different types of oscillators. Therefore, the rise rate of VDD and the start-up time of different crystal oscillators are not fixed. The RC oscillator has the shortest start-up time, while the crystal oscillator has a longer start-up time. During the use of the user terminal, attention should be paid to the host's requirements for power-on reset time.

3.10.2 Power-on Reset

Power-on reset is closely related to LVR operation. The system power-on process presents a gradually rising curve, which takes a certain amount of time to reach the normal level value.

Power-on: The system detects the power supply voltage rising and waits for it to stabilize;

External reset (limited to the external reset pin enable state): The system detects the external reset pin state. If it is not high, the system remains in the reset state until the external reset pin is released;

System initialization: All system registers are set to their initial values;

Oscillator starts working: The oscillator starts providing the system clock;

Execute program: Power-on ends and the program starts running.

3.10.3 WDT Watchdog Reset

Watchdog reset is a protection setting for the system. In normal state, the watchdog timer is cleared by the program. If an error occurs, the system is in an unknown state, and the watchdog timer overflows, at which point the system resets. After the watchdog reset, the system restarts and enters the normal state.

Watchdog timer status: The system detects whether the watchdog timer has overflowed. If it has, the system resets;

System initialization: All system registers are set to their default state;

Oscillator starts working: The oscillator starts providing the system clock;

Execute program: Power-on ends, and the program starts running.

Watchdog timer application precautions:

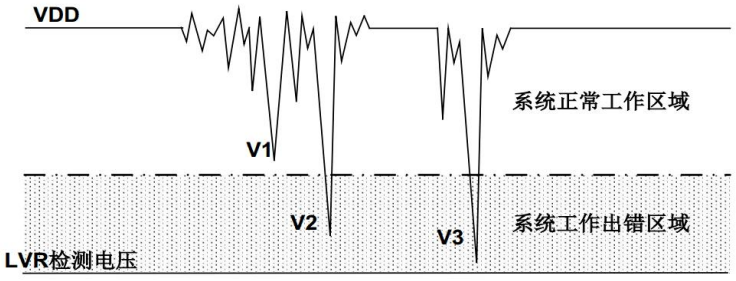
1. Checking the status of I/O ports and the contents of RAM before clearing the watchdog can enhance program reliability;

2. Do not clear the watchdog in the interrupt, otherwise the situation that the main program is running away cannot be detected;

3. The program should only have one watchdog clearing action in the main program. This architecture can maximize the protection function of the watchdog.

3.10.4 Power-Down Reset

Brown-out reset is aimed at the situation of system voltage drop caused by external factors (for example, interference or changes in external load). Brown-out reset may cause abnormal system operating status or program execution errors.



Voltage drops may enter the system dead zone. System dead zone means that the power supply cannot meet the minimum operating voltage requirements of the system. The above figure is a typical brown-out reset diagram. In the figure, VDD is severely disturbed, and the voltage value drops very low. The system works normally in the area above the dotted line. In the area below the dotted line, the system enters an unknown working state, which is called the dead zone. When VDD drops to V1, the system is still in a normal state; when VDD drops to V2 and V3, the system enters the dead zone, which can easily lead to errors. The system may enter the dead zone in the following situations:

In DC applications:

In DC applications, batteries are generally used for power supply. When the battery voltage is too low or the microcontroller drives the load, the system voltage may drop and enter the dead zone. At this time, the power supply will not further drop to the LVD detection voltage, so the system remains in the dead zone.

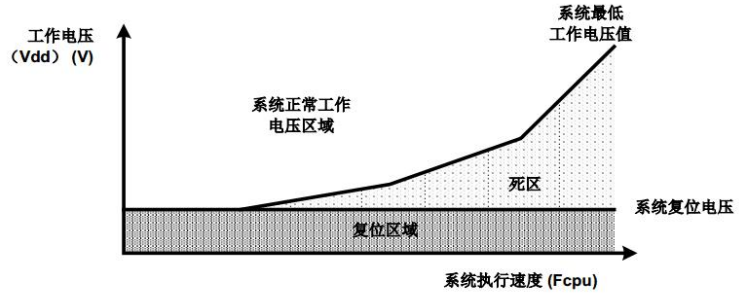
In AC applications:

When the system is powered by AC, the DC voltage value is affected by noise in the AC power supply. When the external load is too high, such as when driving a motor, the interference generated by the load action also affects the DC power supply. If VDD drops below the minimum operating voltage due to interference, the system may enter an unstable operating state.

In AC applications, the system has a longer power-on and power-off time. Among them, the power-on sequence protection enables the system to power on normally, but the power-off process is similar to that in DC applications. After the AC power is turned off, the VDD voltage is likely to enter the dead zone during the slow decline process.

3.10.5 Operating frequency and LVR low voltage detection relationship

In order to improve the performance of system brown-out reset, it is first necessary to clarify the minimum operating voltage value of the system. The minimum operating voltage of the system is related to the system execution speed, and the minimum operating voltage value is also different at different execution speeds.



系统工作电压与执行速度关系图

As shown in the figure above, the normal operating voltage area of the system is generally higher than the system reset voltage, and the reset voltage is determined by the low voltage detection (LVR) level. When the system execution speed increases, the minimum operating voltage of the system also increases accordingly, but since the system reset voltage is fixed, there will be a voltage area between the minimum operating voltage of the system and the system reset voltage where the system cannot work normally and will not reset. This area is the dead zone.

To avoid dead zone voltage, select the corresponding LVR reset voltage point when selecting the operating frequency. The following table:

Working frequency	LVR Reset Voltage Point
IRC-8M,2Clock	LVR=2.7V and above
IRC-1M,2Clock	LVR=1.8V and above
IRC-910K,2Clock	LVR=1.8V and above

Note: The corresponding values of the operating frequency and LVR reset voltage point are only recommended values. Users can appropriately adjust the reset voltage point according to the specific application occasions during use.

3.11 System Clock Function Module

JZ8P2508 integrates 4 kinds of oscillators internally, which can be configured by OPTION. See the following table for details:

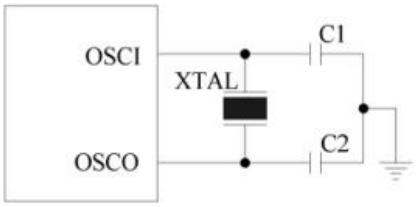
Internal Oscillator Description

Oscillator Type	Description
IRC (Internal RC Oscillator)	455K/1M/2M/4M/8M/16M can be selected
LXT (Low Speed Crystal)	32.768KHz
HXT (High Speed Crystal)	1M～16M

Note: The system frequency transition point between HXT and LXT is around 400kHz.

3.11.1 External Crystal Oscillator/Ceramic Resonator (XT)

In most applications, a crystal or ceramic resonator can be connected to the OSCO and OSCI pins to generate oscillations. The circuit diagram is as follows, which is applicable to both HXT and LXT modes. The table shows the recommended values for C1 and C2. Since the characteristics of each resonator are different, users should refer to their specifications to select appropriate values for C1 and C2.



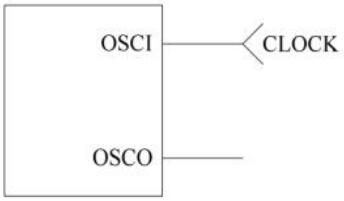
Crystal/Oscillator Circuit

Capacitor selection reference for crystal oscillator or ceramic oscillator:

Oscillator Mode	Frequency Mode	Frequency	C1(pF)	C2(pF)
Crystal Oscillator	LXT (32.768K)	32.768 KHz	40	40
	HXT (1M～16M)	1 MHz	30	30
		2 MHz	30	30
		4 MHz	20	20
		8 MHz	30	30

Note: The above data is for reference only, and everything is subject to actual testing.

The JZ8P2508 can also be driven by an external clock signal on the OSCI pin, and its application diagram is as follows:



External Clock Schematic Diagram

3.11.2 Internal RC Oscillator Mode (IRC)

JZ8P2508 provides internal RC mode.

The internal RC oscillation mode has 8MHz, 1MHz, 910KHz. By setting the configuration bits of OPTION, the IRC working frequency can be selected. The following are their corresponding relationships:

Firc	IRC Frequency
8 M	IRC frequency is selected as 8MHz
1 M	IRC frequency is selected as 1MHz
910 K	IRC frequency is selected as 910KHz

The IRC frequency can be automatically corrected by the burner, and the theoretical correction accuracy is ±1%.

IRC Frequency Drift (T=25℃, VDD=5V±5%, GND=0V)				
IRC	Drift rate			
	Temperature (-40℃～+85℃)	Voltage (1.8V～5.5V)	Process	Total
16MHz	±5%	±5%	±1%	±11%
2MHz	±5%	±5%	±1%	±11%
4MHz	±5%	±5%	±1%	±11%
8MHz	±5%	±5%	±1%	±11%
1MHz	±5%	±5%	±1%	±11%
455kHz	±5%	±5%	±1%	±11%

The JZ8P2508 provides a variety of frequency division options, which can be selected in OPTION and are suitable for more occasions. The following table:

Clocks	Clocks frequency division
2clock	Frequency division is 2clock
4 o'clock	Divide by 4clock
8clock	Divide by 8clock
16clock	Divide by 16clock
32clock	Divide by 32clock

3.11.3 Clock Module Application Notes

The internal oscillator is the most commonly used oscillation mode, which can eliminate the need for external circuits;

When using an external clock input, the clock signal should be input from OSCI, and OSCO can be left floating;

When using an external oscillator and it is greater than 400kHz, be sure to select the external high-speed oscillator in the OPTION option when burning the program. When it is less than 400kHz, select the external low-speed oscillator;

The clock frequency of each oscillation mode may vary slightly depending on external conditions, and should be selected appropriately according to needs during use.

4 CODE OPTION Register

JZ8P2508 needs to set different options during burning, as shown in the table below:

CODE OPTION	Option	Function Description
Package Pin	14/16/18/20 PIN	Chip pin selection 14/16/18/20 PIN
	8 PIN	Chip pin selection 8 PIN
Watchdog	Enable	WDT Enable
	Disable	WDT Disable
Code Encryption	Enable	Programming Mode Data Encryption
	Disable	Programming Mode Data Unencrypted
Clocks frequency division	2 Clocks	Clocks Divide Frequency Selection 2 Clocks
	4 Clocks	Clocks frequency division selection 4 Clocks
	8 Clocks	Clocks frequency division selection 8 Clocks
	16 Clocks	Clocks frequency division selection 16 Clocks
	32 Clocks	Clocks frequency division selection 32 Clocks
Oscillation mode	IRC mode	IRC mode
	LXT Mode	LXT (0K~400K) mode
	HXT mode	HXT (400K~16M) mode
IRC Frequency	8M	IRC frequency selection 8M
	1M	IRC frequency selection 1M
	910K	IRC frequency selection 910K
System clock frequency multiplication option	Enable	System clock multiplier enable
	Disable	System clock multiplier disable
Low voltage reset (LVR)	1.2V	Low voltage reset point selection 1.2V
	1.6V	Low voltage reset point selection 1.6V
	1.8V	Low voltage reset point selection 1.8V
	2.4V	Low voltage reset point selection 2.4V
	2.7V	Low voltage reset point selection 2.7V
	3.3V	Low voltage reset point selection 3.5V
	3.6V	Low voltage reset point selection 3.9V
Reset time	PWRT=WDT=4.5ms	Wake-up settling time = WDT overflow time (no division) =
	PWRT=WDT=18ms	Wake-up settling time = WDT overflow time (no division) =
	PWRT=WDT=72ms	Wake-up settling time = WDT overflow time (no prescaling)
	PWRT=WDT=288ms	Wake-up settling time = WDT overflow time (no prescaling)
	PWRT=140us,WDT=4.5ms	Wake-up settling time = 140us, WDT overflow time (no
	PWRT=140us,WDT=18ms	Wake-up settling time = 140us, WDT overflow time (no
	PWRT=140us,WDT=72ms	Wake-up settling time = 140us, WDT overflow time (no
	PWRT=140us,WDT=288ms	Wake-up settling time = 140us, WDT overflow time (no
P57 port	RST	P57 port acts as reset function
	GPIO	P57 port acts as general purpose input/output port
	GPI	P57 port acts as general purpose input port
P57 pull-up	Enable	P57 port pull-up enable
	Disable	P57 port pull-up disable
P5/P6 port wake-up	Non-independent	P5/P6 port non-independent control wake-up
	Independent control	P5/P6 port independent control wake-up
P5/P6	Enable	Enable (Pull-up: P57-P50, Pull-down: P56-P53/P67-P64/P7,

	Shield	Shield (Pull-up: P57-P50, Pull-down: P56-P53/P67-P64/P7)
Lookup table range	1/4K	The lookup table range is in the first 1/4K of ROM
	2K	The lookup table range is within the entire 2K ROM
RTC	Enable	RTC Enable
	Disable	RTC Disable
Sleep Wake-up Settings	Compatible with old 153	Compatible with old 153 series
	Multiple wake-up	Multiple wake-up sources allowed to wake up simultaneously
Pull-up/Pull-down Current Drive Enhancement	P5/P6 Level 1 Drive	P5/P6 Level 1 Drive Enhancement (IOH=50mA, IOL=60mA)
	P6 port secondary drive	P66-P67/P60-P62 secondary drive enhancement (IOH=70mA,
	P6 port tertiary drive	P66-P67/P60-P62 tertiary drive enhancement (IOH=90mA,
	P6 port quaternary	P66-P67/P60-P62 quaternary drive enhancement (IOH=110mA,
IRC oscillator	LDO voltage	IRC oscillator voltage source selection LDO voltage
	VDD voltage	IRC oscillator voltage source selects VDD voltage
POWER	HIGH	Select HIGH when VDD is powered by 5V
	LOW	Select LOW when VDD is powered by 3.3V

5 Chip Electrical Characteristics

5.1 Chip Absolute Maximum Ratings

Operating Temperature (℃):	(√) E: -40-85;
Storage Temperature (℃):	(√) -65～+150;
Limiting Voltage (V)	(√) Other -0.3～6;
Limiting Input Voltage (V)	(√) Other GND-0.3～VDD+1;
Limiting Output Voltage (V)	(√) Other GND-0.3～VDD+1;

5.2 Chip DC Parameters

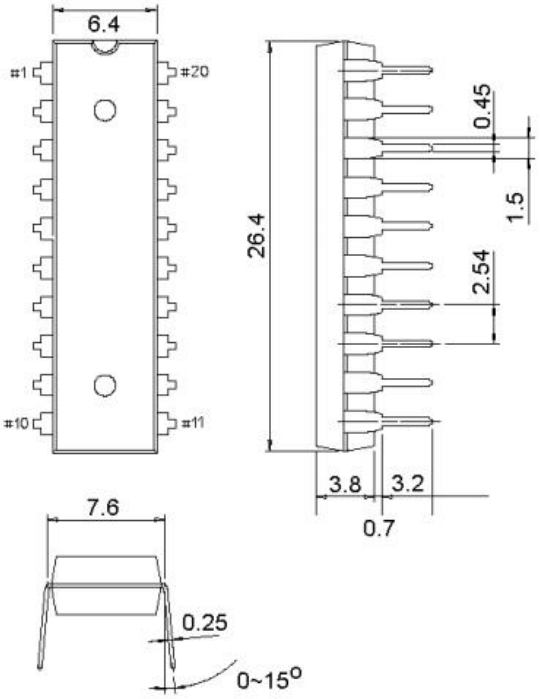
(T=25℃, VDD=5±5%V,GND=0V)

Symbol	Parameter Description	Condition	Minimum	Typical	Maximum	Unit
IRC1	IRC1 (corrected)	OPTION select 1MHz	-	1	-	MHz
IRC2	IRC2 (corrected)	OPTION selects 8MHz	-	8	-	MHz
IRC3	IRC3 (after correction)	OPTION selects 910KHz	-	910	-	KHz
IOH1	Output high level drive (except P60-62, P66, P67)	Ioh=4.4V	-	9	-	mA
IOH2	Output high-level drive one level enhancement (except P60-62, P66, P67)	Ioh=4.4V	-	15	-	mA
IOH3	Output high level drives secondary enhancement (P60-62, P66, P67)	Ioh=4.4V	-	60	-	mA
IOH4	Output high level drives tertiary enhancement (P60-62, P66, P67)	Ioh=4.4V	-	70	-	mA
IOH5	Output high level drives quaternary enhancement (P60-62, P66, P67)	Ioh=4.4V	-	75	80	mA
IOL1	IO output low level drive (except P60-62, P66, P67)	Iol=0.6V	-	18	-	mA
IOL2	IO output low level drives a single level of enhancement (excluding P60-62, P66, P67)	Iol=0.6V	-	30	-	mA

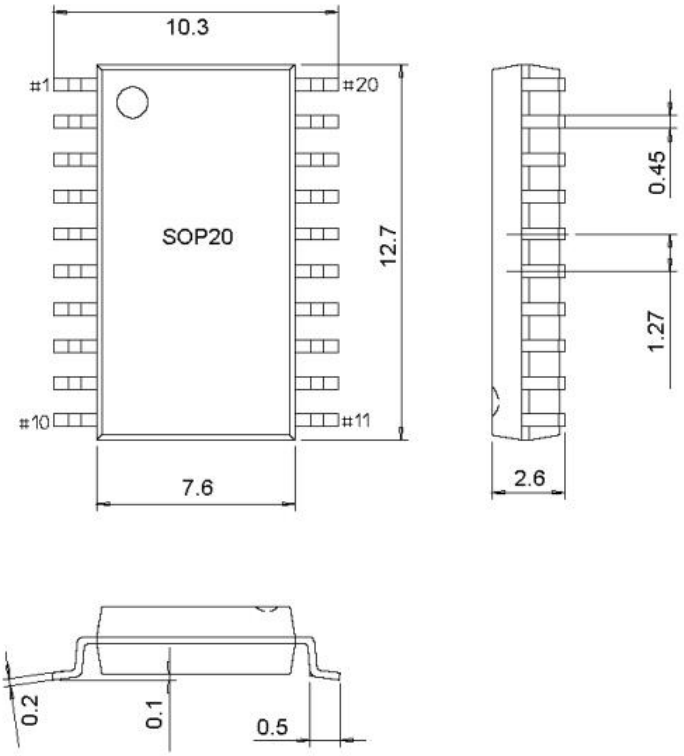
IOL3	IO output low level drives two levels of enhancement (P60-62, P66, P67)	Iol=0.6V	-	80	90	mA
IOL3	IO output low level drives three levels of enhancement (P60-62, P66, P67)	Iol=0.6V	-	100	120	mA
IOL4	IO output low level drives four levels of enhancement (P60-62, P66, P67)	Iol=0.6V	-	120	140	mA
IPH	Pull-up current	Pull-up enable, input grounded	70	100	150	μA
IPD	Pull-down current	Pull-down enable, input connected to VDD	40	60	100	μA
Isb1	Shutdown current 1	All inputs connected to VDD, output floating, WDT and LVD disabled	-	-	1	μA
Isb2	Shutdown current 2	All inputs connected to VDD, output floating, WDT enabled, LVD disabled	-	-	10	μA
Isb3	Shutdown current 3	All inputs are connected to VDD, output is floating, LVD is enabled, WDT is disabled	-	-	10	μA
Iop2	Operating current 1 (VDD=5V)	IRC=8MHz 2clock	-	-	1.2	mA
Iop2	Operating current 2 (VDD=5V)	IRC=1MHz 2clock	-	-	0.2	mA
Iop2	Operating current 3 (VDD=5V)	IRC=910KHz 2clock	-	-	0.2	mA
LVR	Low voltage reset voltage	Select LVR reset point	Vlvr-0.1	Vlvr	Vlvr+0.1	V
LVD	Low voltage detection voltage	Select the detection point as Vlvd	Vlvd-0.1	Vlvd	Vlvd+0.1	V
Note: The above parameters are for reference only. Please refer to the actual measured data of the target sample.						

6 Package Size Information

6.1 20PIN Package Size

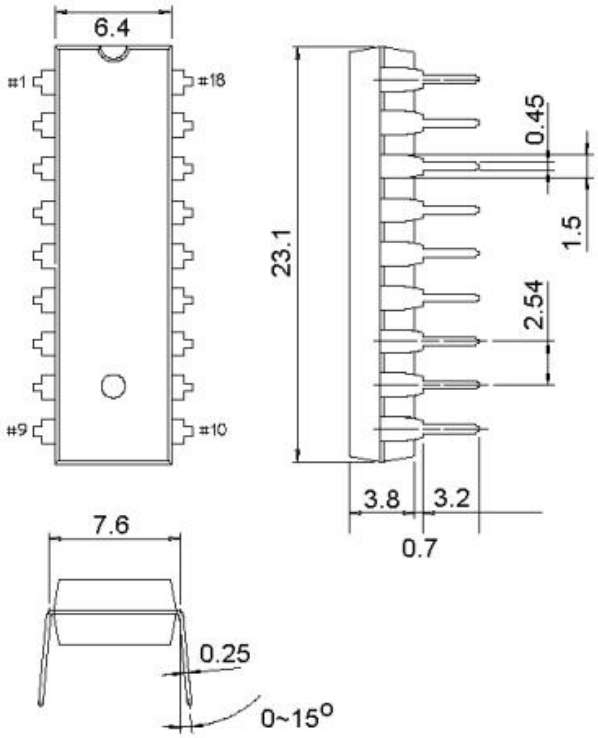


DIP20 Package Size

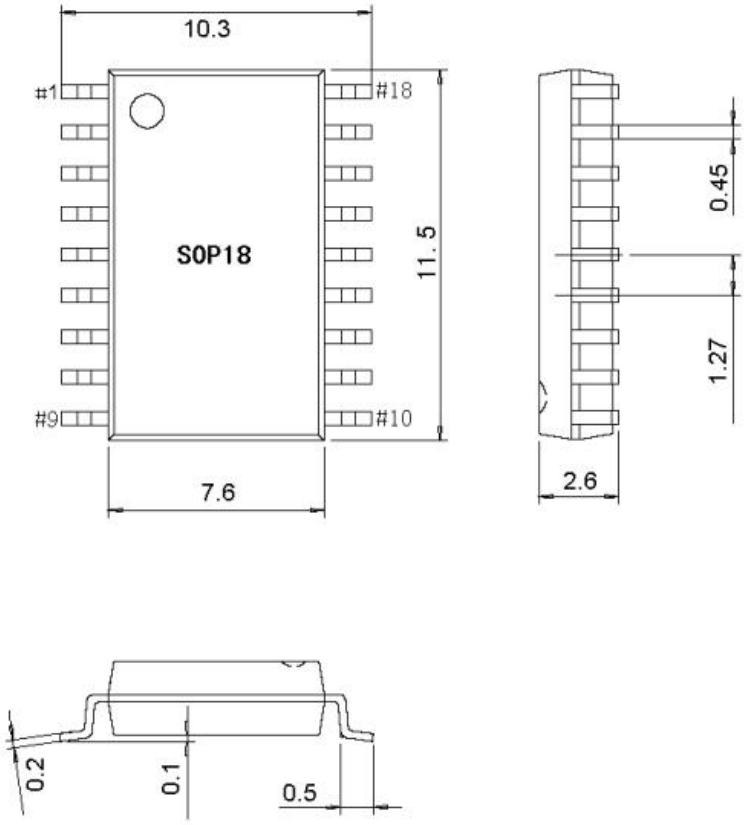


SOP20 Package Size

6.2 18PIN Package Size

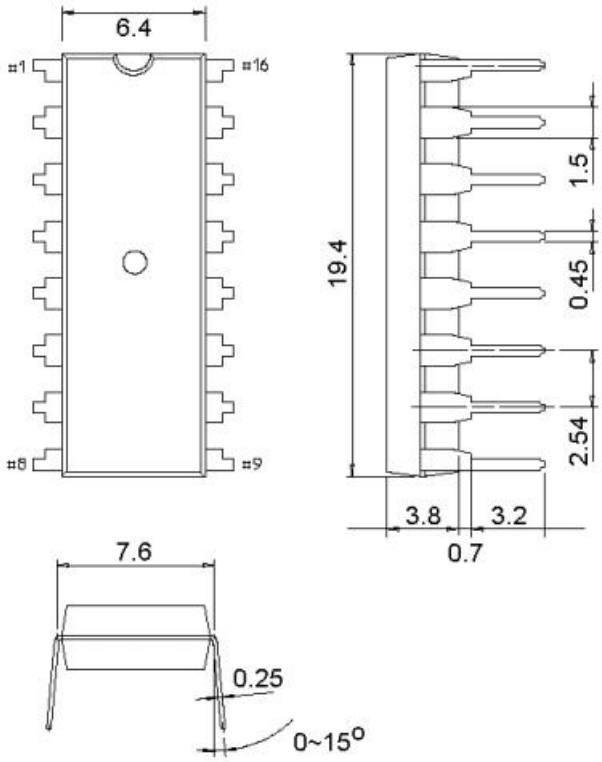


DIP18 Package Size

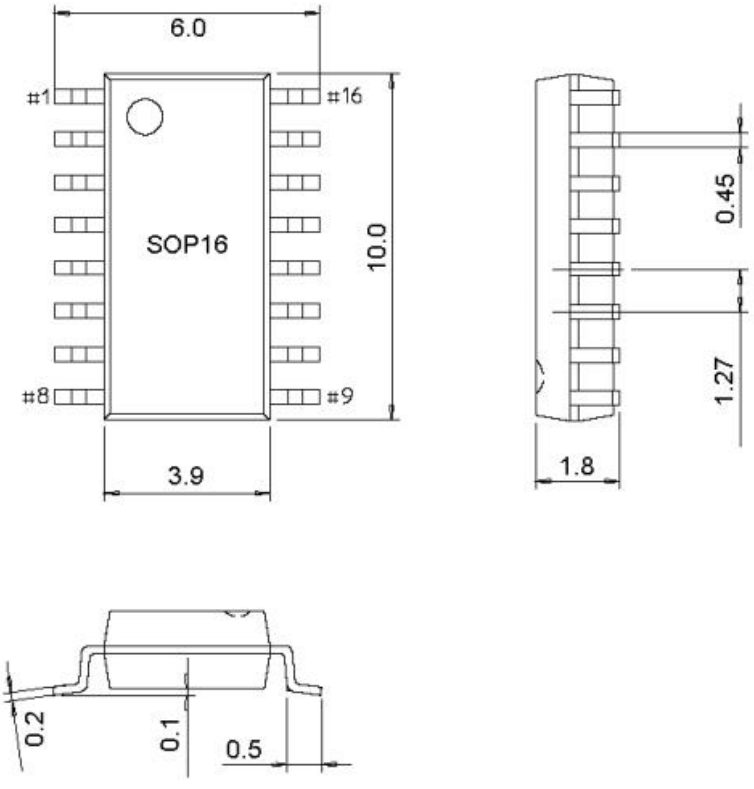


SOP18 Package Size

6.3 16PIN Package Size

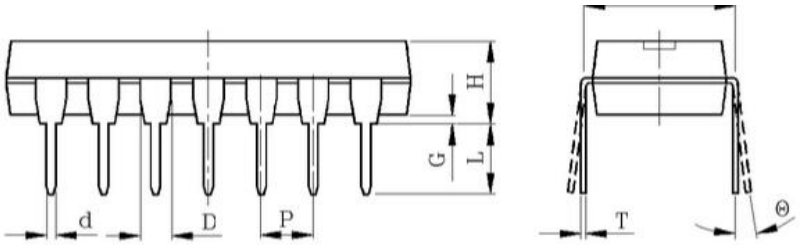


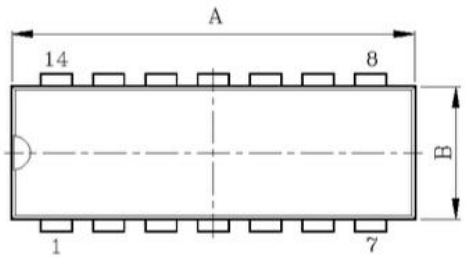
DIP16 package size



SOP16 package size

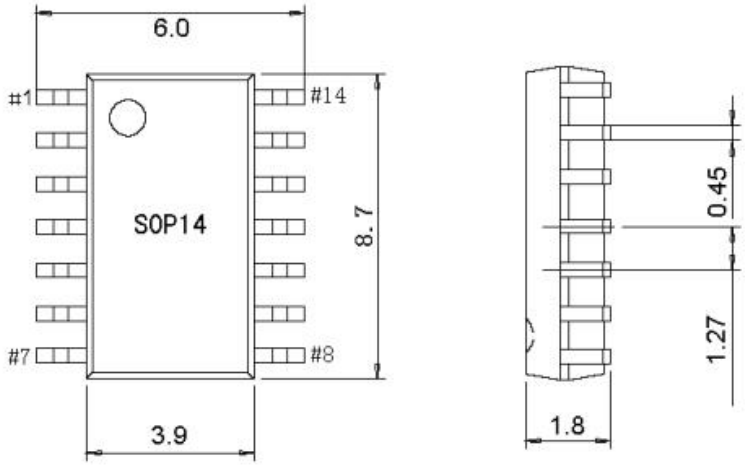
6.4 14PIN package size

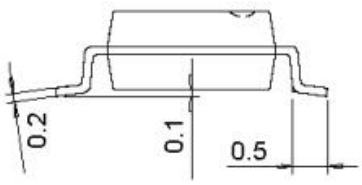




DIM	MILLIMETERS
A	19.3±0.2
B	6.45±0.2
D	1.52±0.1
d	0.46±0.1
G	0.50 MIN
H	3.8±0.3
L	3.3±0.3
P	2.54
T	0.25+0.1/−0.05
W	7.62
θ	0 ~ 15°

DIP14 package size

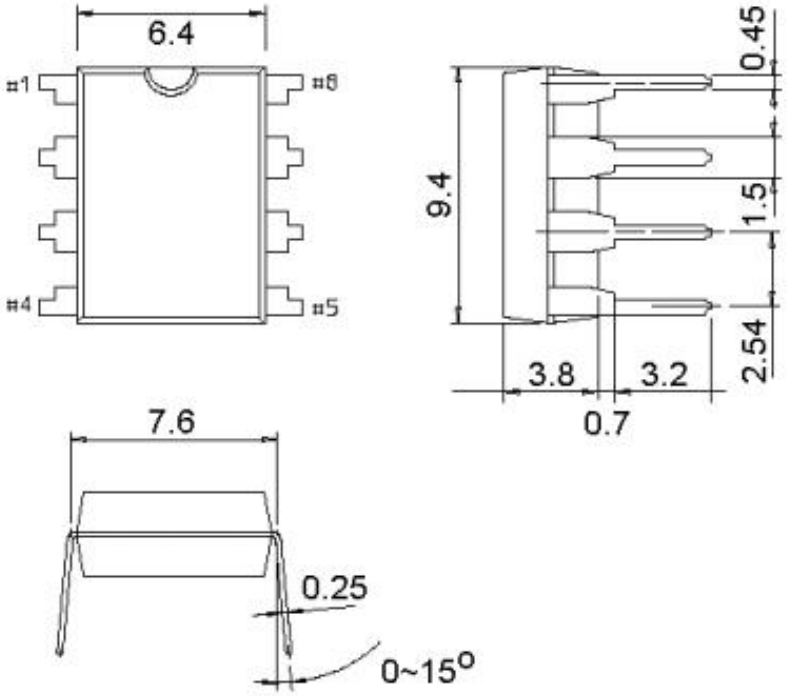




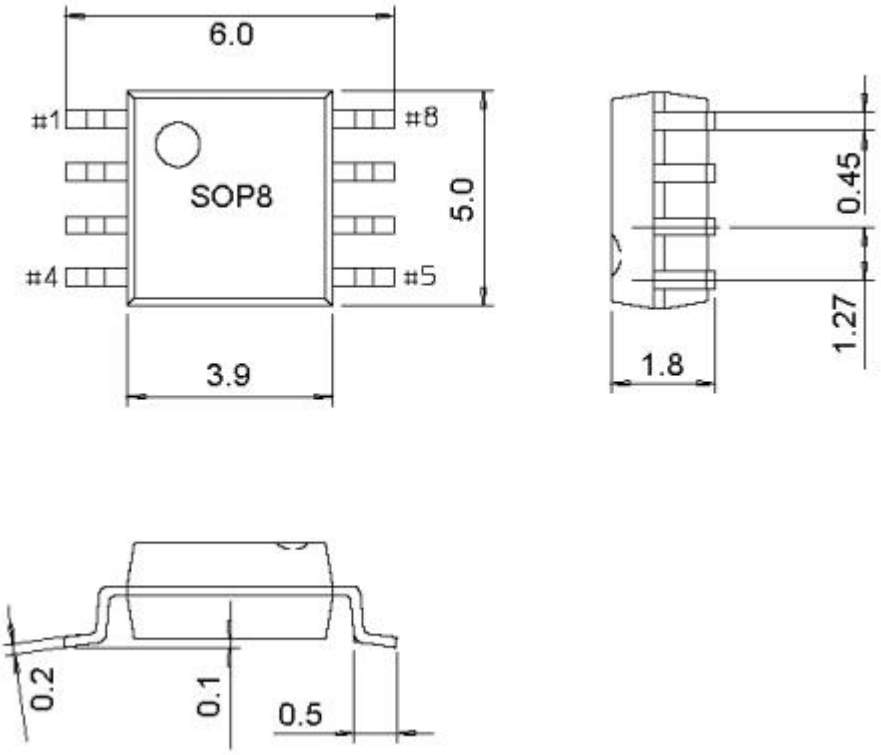
SOP14 package size

6.5 8PIN package size

Unit (mm)



DIP8 package size



SOP8 package size