JZ8P2521

8-BIT Microcontroller with OTP ROM

Product Specification

Version 1.0

Specification Revision History

Version	Revision Description	Notes
V1.0	Publishing the first draft	

Notes:

1、When the TC0CON register Bit.3(PAB) pre-division selection Bit and Bit.2 ~ 0(TC0PSR2 ~ PSR0) division selection Bit are in switching state, it is necessary to turn off the watchdog enable first, and then turn on the watchdog enable after the switching is completed, otherwise it is easy to cause reset.

2、When the port level capture function is used, the frequency division option in the TC0CON register cannot be operated after the capture and sampling is completed, otherwise the sampling value will be affected.

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1. General Description

1.1 Features

CPU configuration

- 2K×14-Bit OTP ROM
- 96×8-Bit SRAM
- 8 levels of stack space
- 8 programmable Voltage Reset (LVR)
  1.2V, 1.6V, 1.8V, 2.4V
  2.7V, 3.3V, 3.6V, 3.9V
- Operating current less than 2mA (Fcpu=4MHz/5V)
- Operating current less than 1μA (Fcpu=8KHz/5V)
- Sleep current less than 1μA(sleep mode)

I/O configuration

- 2 sets of bidirectional IO ports :P5, P6
- 14 GPIO pins
- Supports open-drain output port: P5
- Configurable driver enhancement port: P5
- You can input to change the wake-up port: P5, P6
- 14-bit programmable pull-up I/O pins
- 14-bit programmable pull-down I/O pin
- External interrupt :INT(P60 or P63)
- P63 can be configured to pull up and down and output

Working conditions

- Working voltage range:

$V_{LVR2.8\,V\sim5.5\,V}$ | Fcpu = 0 ~ 8 MHz

$V_{LVR1.8\,V\sim5.5\,V}$ | Fcpu = 0 ~ 2 MHz

Low operating temperature range:

Working temperature -40℃-85℃

Operating frequency range

- Instruction clock frequency selection: 2T/4T/8T/16T/32T
- Built-in IHRC oscillator power supply source is optional:VDD, LDO 2.1V

Source of interruption

- TC0 overflow interrupt
- External interrupt 0
- P5 port input change interrupt
- Port P6 input change interrupt
- TC1 cycle overflow interrupt
- TC2 cycle overflow interrupt
- CMP comparator result change interrupt

Features

- P60/P63 port level capture
- PWM1, PWM4 support LED cascade control
- Programmable WDT timer 4.5ms, 18ms, 72ms, 288ms

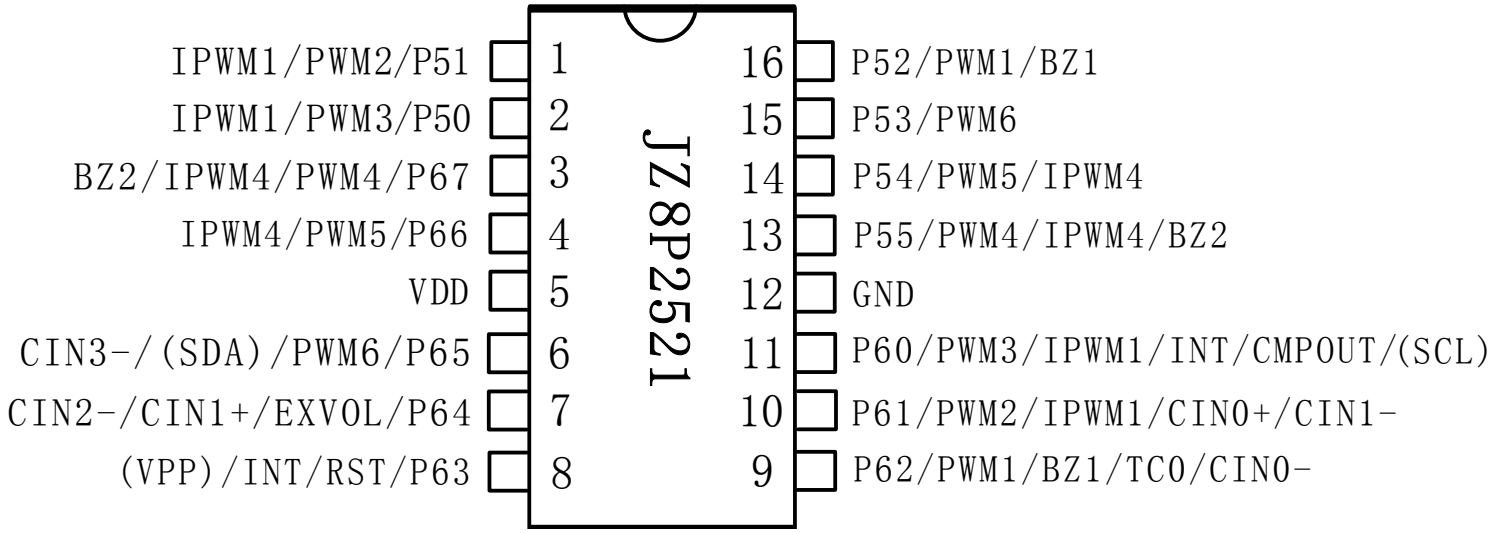
Peripheral modules

- 3-way total cycle 10bit TC1/PWM123
- 3 channels total cycle 10bit TC2/PWM456
  Comparator CMP

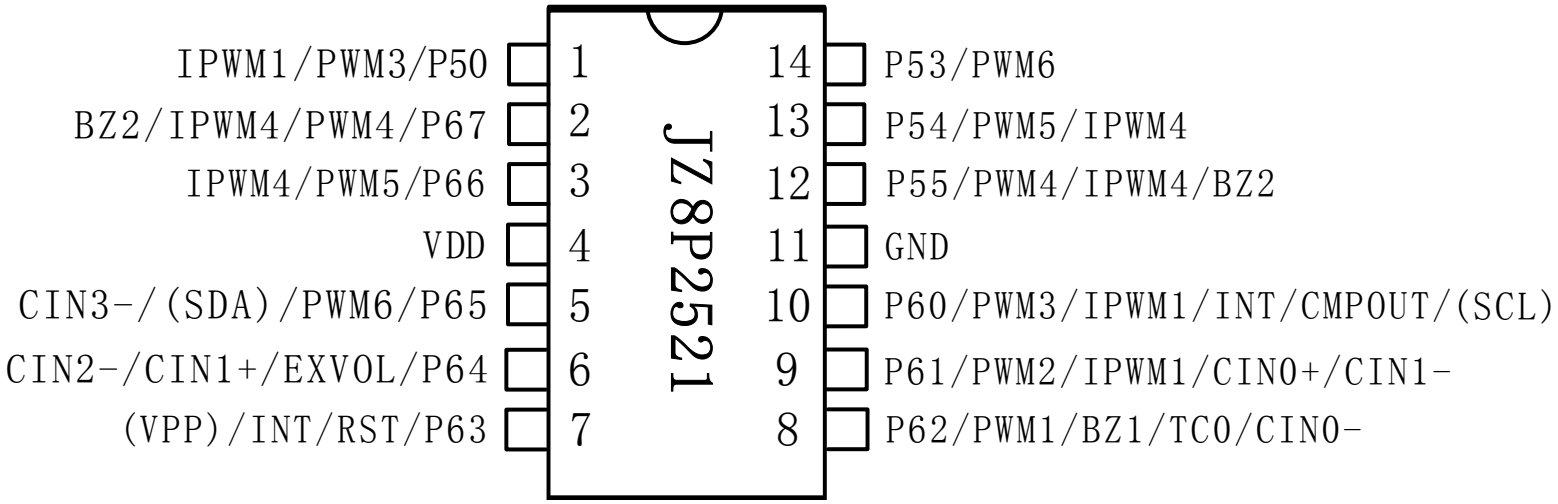
Encapsulation type

- JZ8P2521-DIP/SOP16
- JZ8P2521-DIP/SOP14
- JZ8P2521-DIP/SOP8

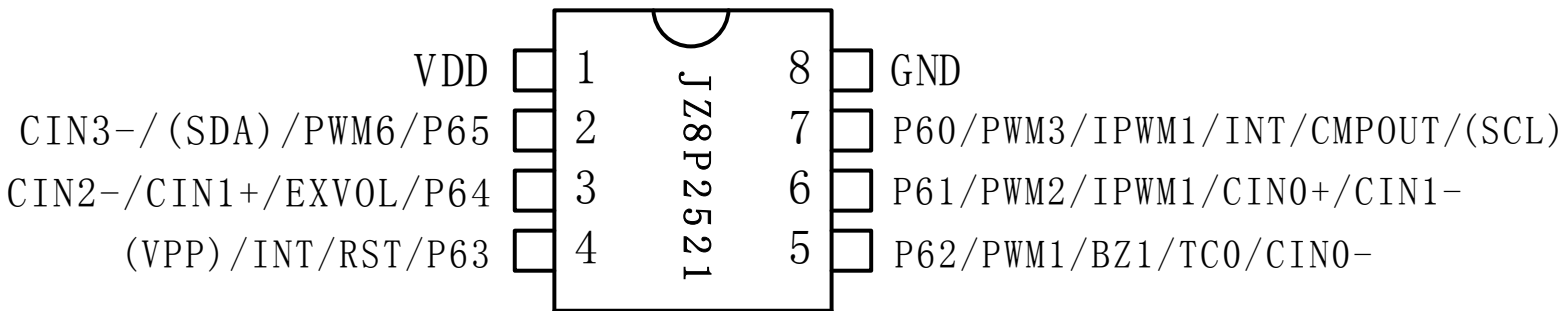
1.2 Pin Assignment



JZ8P2521-16PIN MAP



JZ8P2521-14PIN MAP



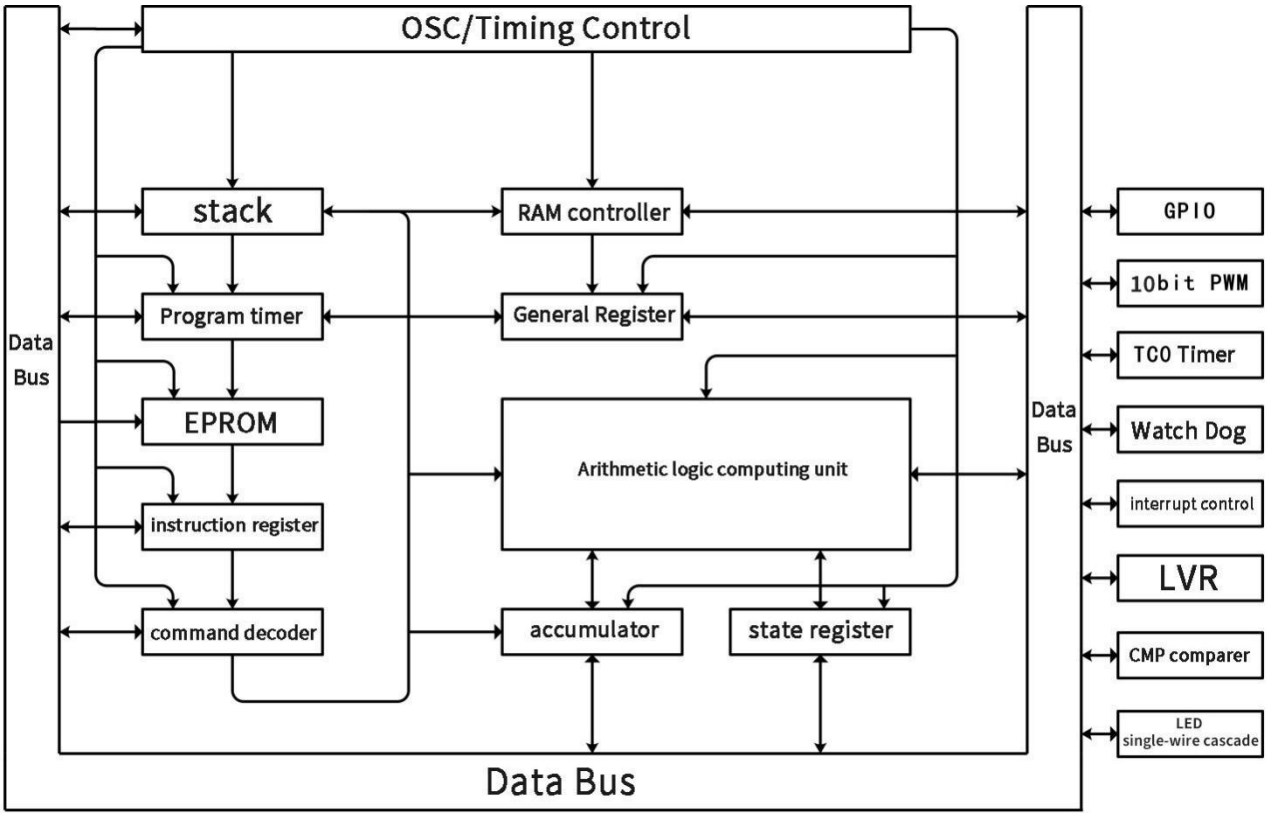
JZ8P2521-8PIN MAP

1.3 Pin Description

NUM	NAME	I/O	Description
P50	P50	I/O (up/down)	GPIO, programmable pull up/down, open/drain output, port
	PWM3	O	PWM3 outlet
	IPWM1	O	IPWM1 outlet
P51	P51	I/O (up/down)	GPIO, programmable pull up/down, open/drain output, port
	PWM2	O	PWM2 outlet
	IPWM1	O	IPWM1 outlet
P52	P52	I/O (up/down)	GPIO, programmable pull up/down, open/drain output, port
	PWM1	O	PWM1 outlet
	BZ1	O	BZ1 outlet
P53	P53	I/O (up/down)	GPIO, programmable pull up/down, open/drain output, port
	PWM6	O	PWM6 outlet
P54	P54	I/O (up/down)	GPIO, programmable pull up/down, open/drain output, port
	PWM5	O	PWM5 outlet
	IPWM4	O	IPWM1 outlet
P55	P55	I/O (up/down)	GPIO, programmable pull up and down, open-drain output, port
	PWM4	O	PWM4 outlet
	IPWM4	O	IPWM1 outlet
	BZ2	O	BZ2 outlet
P60	P60	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	PWM3	O	PWM3 output outlet
	IPWM1	O	IPWM1 outlet
	INT	I (SMT)	External interrupt input port
	CMPOUT	O	Comparator result output port
	SCL	I (SMT)	Burn the clock port
P61	P61	I/O (up/down)	GPIO, programmable pull up and down, port wake-up
	PWM2	O	PWM2 outlet
	IPWM1	O	IPWM1 outlet
	CIN0+	I	Comparator positive input port
	CIN1-	I	Comparator negative input port
P62	P62	I/O (up/down)	GPIO, programmable pull up and down, port wake-up
	TC0	I	External TC0 signal source input foot
	PWM1	0	PWM1 outlet
	BZ1	O	BZ1 outlet
	CIN0-	I	Comparator negative input port
P63	P63	I/O (pull-up)	GPIO, programmable pull-up, port wake-up
	RST	I (SMT)	Reset pin
	INT	I (SMT)	External interrupt input port
	VPP	I	Burn the high pressure port
P64	P64	I/O (up/down)	GPIO, programmable pull up/down, port wake-up

	EXVOL	I	Divider resistor input voltage
	CIN1+	I	Comparator positive input port
	CIN2-	I	Comparator negative input port
P65	P65	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	PWM6	0	PWM6 outlet
	CIN3-	I	Comparator negative input port
	SDA	I (SMT)	Burn data port
P66	P66	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	PWM5	0	PWM5 outlet
	IPWM4	O	IPWM1 outlet
P67	P67	I/O (up/down)	GPIO, programmable pull up/down, port wake-up
	PWM4	0	PWM4 outlet
	IPWM4	O	IPWM1 outlet
	BZ2	O	BZ2 outlet
	VDD	--	Power supply
	VSS	--	to

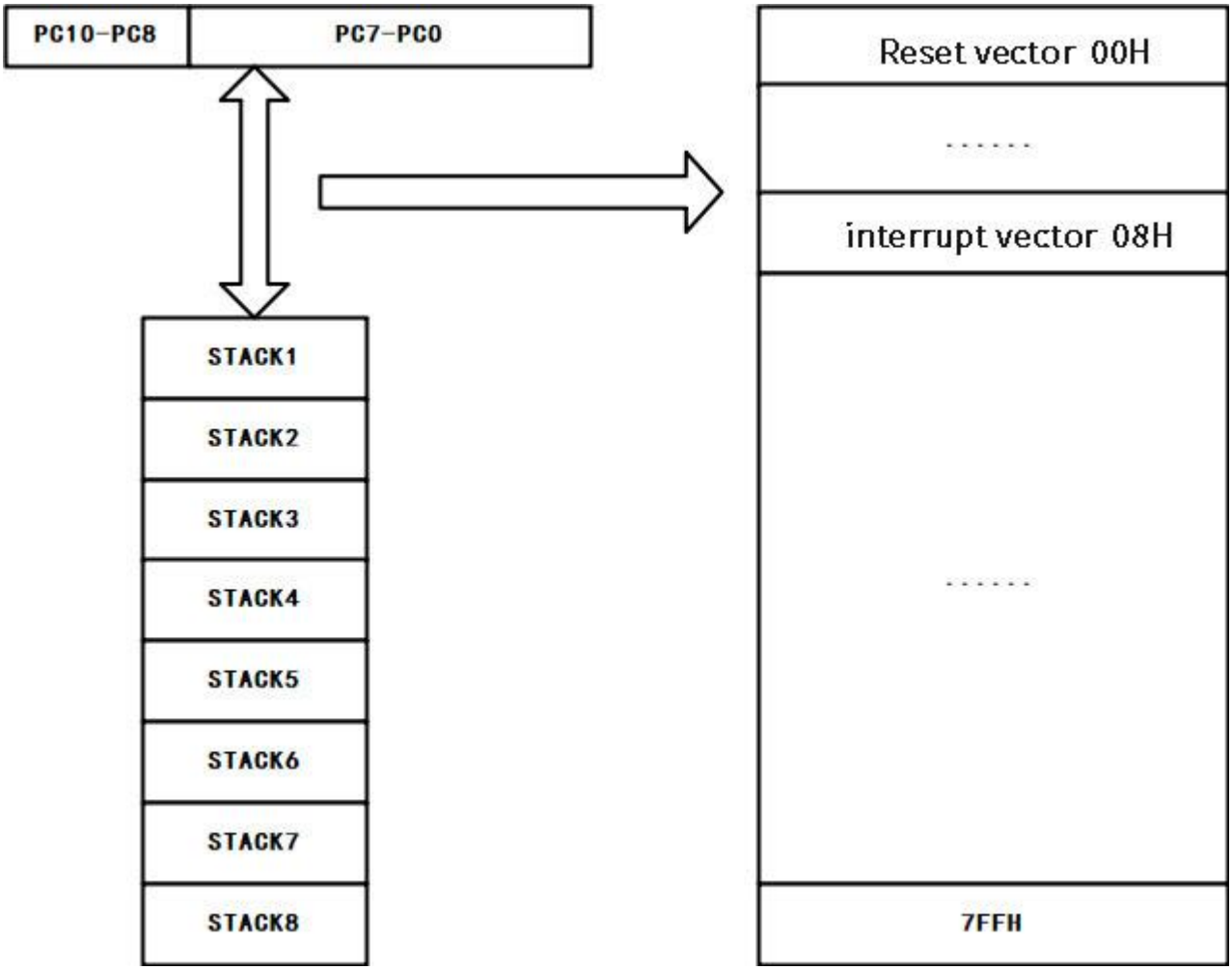
1.4 System block diagram



System circuit block diagram

2. Memory structure

2.1.Program Memory Area



Program store structure diagram

2.2 Data Memory Area

R page \IOC page register area (IOC pages are special pages and can only be read and written using IR/IW instructions)

Address	R page register	IOC page register
0x00	R0/IAR(Indirect addressing register)	Reserve
0x01	R1/TC0C (TC0 count register)	Keep
0x02	R2/PCL(program count low 8-bit register)	IOC2/TC0CON (TC0 control register)
0x03	R3/STATUS(status flag register)	Retain
0x04	R4/RSR(RAM select register)	Reserve
0x05	R5/P5 (P5 data register)	IOC5/P5CON (P5 control register)
0x06	R6/P6 (P6 data register)	IOC6/P6CON (P6 control register)
0x07	R7/CMPCON0 (CMP control register 0)	IOC7/P5PD (P5 pull-down control register)
0x08	R8/CMPCON1 (CMP control register 1)	IOC8/P5PH (P5 pull-up control register)
0x09	R9/P6AE (P6 analog port enable register)	IOC9/TPRE (TC0/WDT pre-division read value
0x0A	Reserved	Keep
0x0B	Reserved	IOCB/P6PD (P6 pull-down control register)
0x0C	RC/P5IWE (P5 input change interrupt/wake enable	IOCC/P5OD (P5 open-drain control register)
0x0D	RD/P6IWE (P6 input change interrupt/wake enable	IOCD/P6PH (P6 pull-up control register)
0x0E	RE/CPUCON (CPU mode control register)	IOCE/WDTCON (Watchdog control register)
0x0F	RF/INTF (interrupt flag register)	IOCF/INTE (Interrupt enable register)
0x10 ... 0x6F	**General Purpose Register (SRAM)**	
0x70	R70/TC1CON (TC1 control register)	
0x71	R71/TC1PRDL (TC1/PWM123 cycle low 8-bit register)	
0x72	R72/PWM1DTL (PWM1 lower duty cycle 8-bit	
0x73	R73/PWM2DTL (PWM2 low duty cycle 8-bit register)	
0x74	R74/PWM3DTL (PWM3 low duty cycle 8-bit register)	
0x75	R75/TC1PRDTH (TC1/PWM123 cycle duty cycle 2 bit higher register)	
0x76	R76/PWMCON0 (PWM control register 0)	
0x77	R77/TC2CON (TC2 control register)	
0x78	R78/TC2PRDL (TC2/PWM456 cycle low 8-bit register)	
0x79	R79/PWM4DTL (PWM4 low duty cycle 8-bit register)	
0x7A	R7A/PWM5DTL (PWM5 lower duty cycle 8-bit	
0x7B	R7B/PWM6DTL (PWM6 low duty cycle 8-bit register)	
0x7C	R7C/TC2PRDTH (TC2/PWM456 cycle duty cycle high 2-bit register)	
0x7D	R7D/PWMCON1 (PWM control register 1)	
0x7E	Reserved	
0x7F	Reserved	

3 Feature description

3.1 Operate registers

3.1.1 RPAGE ~ R0/IAR (Indirect addressing Register)

00H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAR	IAR<7:0>							
Read/write	R							
Reset values	X							

The indirection addressing register is not an actual register, its main function is to act as a pointer to indirection addressing. Any instruction that has R0 as a pointer actually corresponds to the address pointed to by RSR<6:0>, the lower 7 bits of R4 (RAM select register).

3.1.2 RPAGE ~ R1/TC0C (TC0 count register)

01H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0C(R)	TC0C<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

TC0 is an 8Bit uplink counter, clock source optional internal clock/external clock, count overflow can form interrupts, TC0C can be read and written.

If the PAB bit is cleared (TC0CON.3), there will be a predivider assigned to TC0, and when a value is written to the TC0C register, the value of the predivider will be cleared to 0.

If an external clock is selected, the TC0 can be triggered by the TE bit (defined by the TC0CON.4 bit) to select the signal to trigger the edge, and the increment operation is generated when the clock arrives.

3.1.3 RPAGE ~ R2/PCL(Program Count Low 8-bit register)

02H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCL	PC<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

The program counter (PC) is a pointer used to record the instructions to be processed by the CPU in each instruction cycle. During the CPU run cycle, the PC pushes the instruction pointer into

the program memory, and the pointer is incremented by 1 to enter the next cycle. The JZ8P2521 has an 11-bit wide program counter (PC) whose low bytes come from the read-write PCL and high bytes (PC<10:8>) are unreadable.

The stack is used to record the instruction pointer returned by the program. When a subprogram is called, the PC pushes the instruction pointer onto the stack. When the return instruction is to be executed, the stack sends the instruction pointer back to the PC to continue the original process. The JZ8P2521 has an 8-level stack that occupies neither program nor data storage space, and the stack pointer cannot be read or written.

(1) Both the register PC and the built-in 8-level stack are 11 bits wide and are used for addressing the 2K×14Bit ROM. The JZ8P2521 program memory area is mapped.

(2) In general, PC increases by one; When reset, all bits of PC are reset.

(3) Instruction "JMP" allows direct loading of 11-bit address, therefore, JMP instruction can achieve the current page (within 2K range) any position jump. Instruction "JMP" directly loads the low 11 bit address, and pushes PC +1 onto the stack, so that the subroutine entry address can be accurately located as long as it is in the same page.

(4) When executing "RET" instruction, the top data of the stack is sent to PC.

(5) When setting the table lookup ability of PC to 1/4K (setting the table lookup range in the OPTION option to 0 ~ 256), any instruction that directly modifies the content of PC will cause the 9th, 10th and 11th bits of PC to be reset. Therefore, the jump generated is limited to the first 256 addresses of the same page, and the instruction to change the content of the PC needs 2 instruction cycles.

When the lookup ability of PC is set to 2K, any instruction that rewrites the value of PC will correspondingly affect the top three bits of PC. Therefore, the generated jumps can be expanded to the 2K range.

When an interrupt occurs, the value of the program counter changes, and PC is assigned the value 0x08.

7. The stack works like a loop buffer, that is, after eight stack pushes, the data in the ninth push overwrites the data in the first push, the data in the tenth push overwrites the data in the second push, and so on.

3.1.4 RPAGE ~ R3/STATUS(status flag register)

03H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	RST	GIE	LVREN	T	P	Z	DC	C
Reading/Writing	R	R	R/W	R	R	R/W	R/W	R/W

Reset value	0	0	0	1	1	X	X	X

Bit<7> : Rst-reset type flag bit

0: Other reset type

1: If the sleep mode is changed by the pin input to wake up

Bit<6>：GIE-Interrupt enable flag bit

0: Masked by DIT instructions or hardware interrupts

1: Interrupt enabled by EIT/RTI instruction

Bit<5>：LVREN-LVR Software enablement

0: LVR enabled

1: LVR disabled (OPTION only works when LVR disabled is selected)

Bit<4> : T- time overflow bit

0: WDT overflow

1: Perform "SLEEP" and "CWDT" commands or low voltage reset

Bit<3> : P- power down flag bit

0: Execute the "SLEEP" command

1: Power on reset or execute "CWDT" command

The events that affect T/P are listed in the table below:

Type	RST	T	P
Power on reset	0	1	1
Press RESET in work mode	0	Keep	Keep
RESET Wake up	0	1	0
WDT overflows in working	0	0	Keep
WDT overflow wakes up	0	0	0
Port state change wake up	1	1	0
Execute the CWDT command	Keep	1	1
Execute the SLEEP command	Keep	1	0

Bit<2> : Z- Set to "1" if the result of an arithmetic or logical operation is zero.

0: When the result of an arithmetic or logical operation is not 0

1: When the result of an arithmetic or logical operation is 0

Bit<1> : DC- Auxiliary carry flag

0: When performing the addition, no carry is generated for the lower four bits; / when performing a subtraction operation, the lower four bits produce a borrow

1: When performing the addition operation, the lower four bits have carry generation; / When performing subtraction, no borrow is generated for the lower four bits

Bit<0> : C- Carry flag

0: When performing the addition, no carry is generated for the upper four bits; / when performing subtraction, the high four bits produce a borrow

1: When performing the addition operation, the higher four bits have carry generation; / When performing subtraction, no borrows are generated

3.1.5 RPAGE ~ R4/RSR(RAM select register)

04H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSR	-	RSR<6:0>						
Read/write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	X	X	X	X	X	X	X

RSR<6:0> Used to select RAM register address in indirect addressing mode (addressing range: 0X10 to 0X6F)

RSR is used to cooperate with IAR to realize indirect addressing operation. Users can put the address corresponding to a register into the RSR, and then read and write the general register data at the corresponding address of the RSR by accessing the indirect addressing register IAR.

3.1.6 RPAGE ~ R5/P5(P5 data register)

06H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORT5	-	-	P55	P54	P53	P52	P51	P50
Reading/Writing	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Input/output data register for port 5, 6 bits for port P5

3.1.7 RPAGE ~ R6/P6(P6 data register)

06H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORT6	P67	P66	P65	P64	P63	P62	P61	P60
Reading/Writing	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Input/output data register for port 6, 8 bits for port P6

3.1.8 RPAGE ~ R7/CMPCON0(CMP control register 0)

07H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON0	CMPEN	CMPOUT	CMPRS<5:0>					
Read/write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : CMPEN-CMP enables the control bit

1: Enable

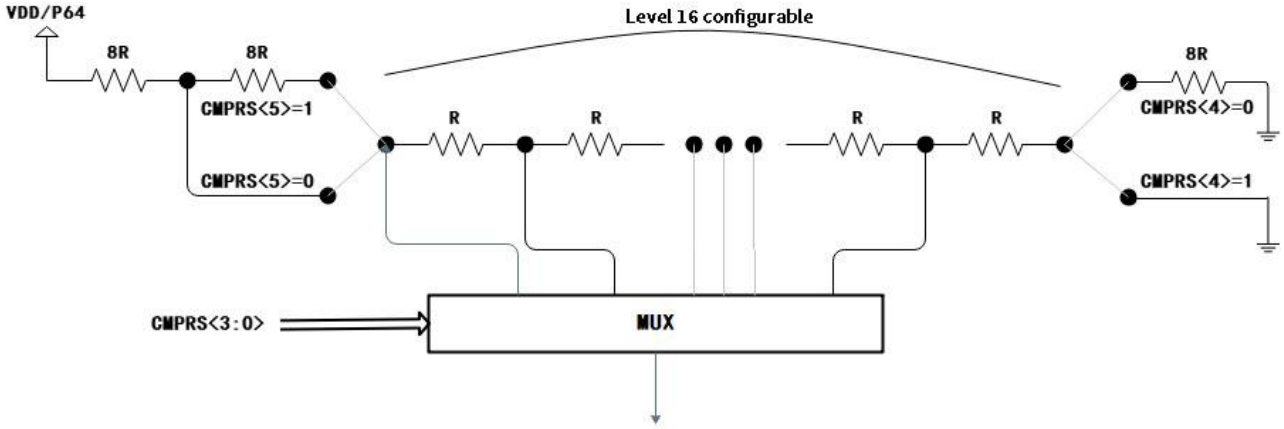
0: Forbid

Bit<6> : CMPOUT-CMP result output bit

1: The comparator positive voltage is greater than the negative voltage

0: The comparator positive voltage is less than the negative voltage

Bit<5:0> : CMPRS<5:0>- Comparator adjustment



When CMPCON1 register =0x85, comparator positive select resistor voltage division, comparator negative select VBG, different resistor voltage division gear CMPRS<5:0> corresponding to different detection voltage, the specific table is as follows:

CMPRS	Detecting voltage	CMPRS	Detecting voltage	CMPRS	Detecting voltage	CMPRS	Detecting voltage
00H	4.48 V	10H	30.24 V	20H	5.60 V	30H	40.32 V
01H	4.03 V	11H	15.12 V	21H	5.04 V	31H	20.16 V
02H	3.67 V	12H	10.08 V	22H	4.58 V	32H	13.44 V
03H	3.36 V	13H	7.56 V	23H	4.20 V	33H	10.08 V
04H	3.10 V	14H	6.05 V	24H	3.88 V	34H	8.06 V
05H	2.88 V	15H	5.04 V	25H	3.60 V	35H	6.72 V
06H	2.69 V	16H	4.32 V	26H	3.36 V	36H	5.76 V
07H	2.52 V	17H	3.78 V	27H	3.15 V	37H	5.04 V
08H	2.37 V	18H	3.36 V	28H	2.96 V	38H	4.48 V

09H	2.24 V	19H	3.02 V	29H	2.80 V	39H	4.03 V
0AH	2.12 V	1AH	2.75 V	2AH	2.65 V	3AH	3.67 V
0BH	2.02 V	1BH	2.52 V	2BH	2.52 V	3BH	3.36 V
0CH	1.92 V	1CH	2.33 V	2CH	2.40 V	3CH	3.10 V
0DH	1.83 V	1DH	2.16 V	2DH	2.29 V	3DH	2.88 V
0EH	1.75 V	1EH	2.02 V	2EH	2.19 V	3EH	2.69 V
0FH	1.68 V	1FH	1.89 V	2FH	2.10 V	3FH	2.52 V

Note: The gray part of the detection voltage is prohibited.

3.1.9 RPAGE ~ R8/CMPCON1(CMP control register 1)

08H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON1	CMPOE	CMPINV	CMPIS<5:0>					
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7>：CMPOE-The comparator result output function was enabled

1: Comparator result output from P60

0:P60 as GPIO

Bit<6>：CMPINV-CMPOUT the output is reversed

1: Negate

0: No negation

Bit<5> : CMPIS<5>- Voltage divider resistor input voltage

1:P64 input

0:VDD

Bit<4:3> : CMPIS<4:3>- Comparator positive input source selection

CMPIS<4>	CMPIS<3>	Positive input source
0	0	Resistance partial pressure
0	1	CIN0+/P61
1	0	CIN1+/P64

Bit<2:0> : CMPIS<2:0>- Comparator negative input source selection

CMPIS<2>	CMPIS<1>	CMPIS<0>	Negative input source
0	0	0	CIN0-/P62
0	0	1	CIN1-/P61
0	1	0	CIN2-/P64
0	1	1	CIN3-/P65
1	0	0	Resistance partial pressure
1	0	1	VBG (Bandgap voltage 1.26V)

3.1.10 RPAGE ~ R9/P6AE(P6 analog port control register)

09H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6AE	PWM4_LEDEN	PWM1_LEDEN	P6AE<5:0>					
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : PWM4_LEDEN-PWM4 single-wire cascaded LED enable bit

1: Enable

0: Forbid

Note: the data cycle is TC2PRD, the duty cycle of data 0 is PWM4 duty cycle, the duty cycle of data 1 is PWM5 duty cycle, and the data register is PWM6 duty cycle register, which enables PWM4_LEDEN+TC2EN to start sending 8-bit cascade data, and automatically reset and reset TC2EN after sending.

Bit<6> : PWM1_LEDEN-PWM4 single line cascaded LED enable bit

1: Enable

0: Forbid

Note: the data cycle is TC1PRD, the duty cycle of data 0 is PWM1 duty cycle, the duty cycle of data 1 is PWM2 duty cycle, and the data register is PWM3 duty cycle register, which enables PWM1_LEDEN+TC1EN to start sending 8-bit cascade data, and automatically reset and reset TC1EN after sending.

Bit<5:0> : P6AE<5:0>-P6 analog port enable control bit

1: P6x set to analog port (disable input function)

0: P6x is GPIO

3.1.11 RPAGE ~ RC/P5IWE (P5 Input change interrupt/wake enable register)

0CH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5IWE	-	-	P5IWE<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P5 Input port state change interrupt/wake up enable control register:

0: Forbidden

1: Enable

3.1.12 RPAGE ~ RD/P6IWE (P6 input change interrupt/wake enable register)

0DH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6IWE	P6IWE<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P6 Input change interrupt/wake up enable control register:

0: Forbidden

1: Enable

3.1.13 RPAGE ~ RE/CPUCON(CPU Mode Control register)

0EH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	CMPWE	INTWE	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : CMPWE-CMP wakeup enable bit

1: CMP wakeup enabled, can wake up the idle mode

0: CMP wakeup disabled

Bit<6>：INTWE-external interrupt wake up enable bit

1: INT wakeup enable to wake up idle mode

0: INT wakeup disabled

Bit<5>：TC2WE-TC2/PWM456 wake up enable bit

1: TC2 wakeup enable to wake up idle mode

0: TC2 wakeup disabled

Bit<4>：TC1WE-TC1/PWM123 wake up enable bit

1: TC1 wakeup enable to wake up idle mode

0: TC1 wakeup disabled

Bit<3>：TC0WE-TC0 wake up enable bit

1: Enable TC0 wakeup to wake up idle mode

0: Disable TC0 wakeup

Bit<2>：STPHX-High speed clock control bit

1: Stop the high speed clock

0: The high-speed clock is working properly

Bit<1>：CLKMD-System clock selection bit

1: System clock using low speed RC oscillator clock

0: System clock using high speed RC oscillator clock

When the system enters the low speed mode from the high speed mode, set CLKMD=1 first, then set STPHX=1;

When the system enters the high speed mode from low speed mode, set STPHX=0 first, and then set CLKMD=0.

Bit<0>：IDLE-Idle mode select bit

1: The system enters idle mode when it executes the SLEEP command, and the system clock works normally

(TC0 and PWM can continue to work in idle mode if the system clock is selected, and the system can be woked up)

0: The system enters SLEEP mode when it executes the sleep command

3.1.14 RPAGE ~ RF/INTF(Interrupt flag register)

0FH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF	-	P5ICIF	TC2IF	CMPIF	TC1IF	INTIF	P6ICIF	TC0IF
Read/write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : Unused

Bit<6> : P5ICIF-P5 port input change interrupt flag bit

Bit<5> : TC2IF-TC2/PWM456 cycle interrupt flag

Bit<4> : CMPIF-comparator state change interrupt flag

Bit<3> : TC1IF-TC1/PWM123 cycle interrupt flag

Bit<2> : INTIF- External port change interrupt flag bit

Bit<1> : P6ICIF-P6 port input change interrupt flag bit

Bit<0> : TC0IF-TC0 counter overflow interrupt flag bit

1: There is an interrupt, software clear 0

0: no interruption

INTF can be reset 0, but can not be reset 1.

Note: When clearing the interrupt flag bit, you must use MOV RF,A operation, not BTC AND AND RF,A instruction operation.

3.1.15 RPAGE ~ R70/TC1CON(TC1 control register)

70H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GAT	TC1CKS	TC1PTEN	TC1PSR<2:0>		

			E					
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7>：TC1EN -TC1/PWM123 counter enable control

(If the TC1PRD register is set, TC1 counts to the preset value reset, TC1 counts from 1)

1: Enable 0: Forbid

Bit<6>：TC21EN-TC1/PWM123、TC2/PWM456 the counter also enables the control bit

1: Enable 0: Forbid

Bit<5> : PWM1GATE-PWM1 gate output enable control bit

1: PWM1 output is controlled by the comparator result, when CMPOUT=0 output PWM waveform, CMPOUT=1 keep PWM1 low level

0: No limit

Bit<4> : TC1CKS-TC1 clock selection

1: System clock

0: Instruction clock

Bit<3:0> : TC1PTEN, TC1PSR2 ~ TC1PSR0 frequency division coefficient selection bit:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	TC1 frequency division coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.16 RPAGE ~ R71/TC1PRDL(TC1/PWM123 cycle low 8-bit register)

71H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : TC1PRD<7:0>-TC1/PWM123 cycle low 8 bit data

3.1.17 RPAGE ~ R72/PWM1DTL(PWM1 low duty cycle 8-bit register)

72H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DTL	PWM1DT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWM1DT<7:0>-PWM1 duty cycle lower 8 bits of data

3.1.18 RPAGE ~ R73/PWM2DTL(PWM2 duty cycle lower 8 bit register)

73H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2DTL	PWM2DT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWM2DT<7:0>-PWM2 duty cycle lower 8 bits of data

3.1.19 RPAGE ~ R74/PWM3DTL(PWM3 8 bit lower duty cycle register)

74H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM3DTL	PWM3DT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWM3DT<7:0>-PWM3 duty cycle lower 8 bits of data

3.1.20 RPAGE ~ R75/TC1PRDTH(TC1/PWM123 cycle duty cycle higher 2 bit register)

75H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<9:8>		PWM3DT<9:8>		PWM2DT<9:8>		PWM1DT<9:8>	
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:6> : TC1PRD<9:8>-TC1/PWM123 cycle high 2 bits of data

Bit<5:4> : PWM3DT<9:8>-PWM3 duty cycle higher 2 bits of data

Bit<3:2> : PWM2DT<9:8>-PWM2 duty cycle higher 2 bits of data

Bit<1:0> : PWM1DT<9:8>-PWM1 duty cycle higher 2 bits of data

3.1.21 RPAGE ~ R76/PWMCON0(PWM control register 0)

76H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON0	BZ1EN	PWM3S	PWM2S	PWM1S	IPWM1EN	PWM3EN	PWM2EN	PWM1EN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : BZ1EN-BZ1 waveform output enable control bit

1: Output BZ1 waveform (need to set BZ1EN=1, PWM1EN=0)

(Set P62/P52 as output to output BZ1 waveform)

0: Forbidden

Bit<6>：PWM3S-PWM3 output selection control

1: PWM3 output from P50

0: PWM3 output from P60

Bit<5>：PWM2S-PWM2 output selection control

1: PWM2 output from P51

0: PWM2 output from P61

Bit<4> : PWM1S-PWM output select control bits

1: PWM1 outputs from P52

0: PWM1 output from P62

Bit<3>：IPWM1EN-IPWM1 enable control bit

1: Output PWM2 and PWM3 XOR

(Choose the output port according to PWM2EN (P61/P51) or PWM3EN (P60/P50))

0: Forbidden

Bit<2>：PWM3EN-PWM3 enable control bit

1: Output PWM3 waveform enable

(Need to set the corresponding port to output to output PWM3 waveform)

0: Forbidden

Bit<1>：PWM2EN-PWM2 enable control bit

1: Output PWM2 waveform enable

(Need to set the corresponding port to output to output PWM2 waveform)

0: Forbidden

Bit<0>：PWM1EN-PWM1 enable control bit

1: Output PWM1 waveform enable

(Need to set the corresponding port to output to output PWM1 waveform, and BZ1EN=0)

0: Forbidden

3.1.22 RPAGE ~ R77/TC2CON(TC2 control register)

77H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7>：TC2EN-TC2/PWM456 Counter enable control

1: Enable

0: Forbid

Bit<6> : PWM4GATE<1>-PWM4 gate output enables control bit 1

1: PWM4 output is controlled by external interrupt INT (P60 or P63), output PWM waveform when INT=1

0: No limit

Bit<5> : PWM4GATE<0>-PWM4 gate output enables control bit 0

1: PWM4 output is controlled by the comparator result, when CMPOUT=0 output PWM waveform, CMPOUT=1 keep PWM4 low level

0: No limit

Bit<4> : TC2CKS-TC2 clock selection

1: System clock

0: The instruction clock

Bit<3:0> : TC2PTEN, TC2PSR2 ~ TC2PSR0 frequency division coefficient selection bit:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 frequency division coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.23 RPAGE ~ R78/TC2PRDL(TC2/PWM456 cycle low bit register)

78H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : TC2PRD<7:0>-TC2/PWM456 cycle low 8 bit data

3.1.24 RPAGE ~ R79/PWM4DTL(PWM4 duty cycle low bit register)

79H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM4DTL	PWM4DT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWM4DT<7:0>-PWM4 duty cycle lower 8 bits of data

3.1.25RPAGE ~ R7A/PWM5DTL(PWM5 duty cycle low bit register)

7AH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM5DTL	PWM5DT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWM5DT<7:0>-PWM5 duty cycle lower 8 bits of data

3.1.26 RPAGE ~ R7B/PWM6DTL(PWM6 duty cycle low bit register)

7BH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM6DTL	PWM6DT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWM6DT<7:0>-PWM6 duty cycle lower 8 bits of data

3.1.27 RPAGE ~ R7C/TC2PRDTH(TC2/PWM456 Cycle Duty Cycle High bit Register)

7CH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD<9:8>		PWM6DT<9:8>		PWM5DT<9:8>		PWM4DT<9:8>	

Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:6> : TC2PRD<9:8>-TC1/PWM456 cycle high 2 bits of data

Bit<5:4> : PWM4DT<9:8>-PWM6 duty cycle higher 2 bits of data

Bit<3:2> : PWM5DT<9:8>-PWM5 duty cycle higher 2 bits of data

Bit<1:0> : PWM6DT<9:8>-PWM4 duty cycle higher 2 bits of data

3.1.28 RPAGE ~ R7D/PWMCON1(PWM control register 1)

7DH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON1	BZ2EN	PWM6S	PWM5S	PWM4S	IPWM4EN	PWM6EN	PWM5EN	PWM4EN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : BZ2EN-BZ2 waveform output enable control bit

1: Output BZ2 waveform (need to set BZ2EN=1, PWM4EN=0)

(Set P55/P67 as output to output BZ2 waveform)

0: Forbidden

Bit<6>：PWM6S-PWM6 Output select control bit

1: PWM6 output from P65

0: PWM6 is output from P53

Bit<5>：PWM5S-PWM5 Output select control bit

1: PWM5 output from P66

0: PWM5 output from P54

Bit<4> : PWM4S-PWM4 output select control bits

1: PWM4 output from P67

0: PWM4 output from P55

Bit<3>：IPWM4EN-IPWM4 Enable control bit

1: Output PWM5 XOR with PWM6

0: Forbidden

(Select output port based on PWM5EN (P54/P66) or PWM6EN (P65/P53))

Bit<2>：PWM6EN-PWM6 enable control bit

1: Output PWM6 waveform enable

(Need to set the corresponding port to output to output PWM6 waveform)

0: Forbidden

Bit<1>：PWM5EN-PWM5 enable control bit

1: Output PWM5 waveform enabled

(Need to set the corresponding port to output to output PWM5 waveform)

0: Forbidden

Bit<0>：PWM4EN-PWM4 enable control bit

1: Output PWM4 waveform enable

(Need to set the corresponding port to output to output PWM4 waveform, and BZ2EN=0)

0: Forbidden

3.2 Control register

3.2.1 IOPAGE ~ IOC2/TC0CON(TC0 control register)

02H(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CON	TC0EN	TC0CKS<1:0>		TC0EDG	PAB	PSR<2:0>		
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1	1	1	1	1

Bit<7>：TC0EN-TC0 Counter enable bit

1: Enable

0: Forbid

Bit<6:5> : TC0CKS<1:0>-TC0 signal source select bit

00: Instruction cycle clock

01: External input signal (at this time P62/EXCK is set as input)

10: The system clock

11: ILRC clock (low speed oscillator)

Bit<4> : TC0EDG-TC0 signal edge selection bit (only P62 is valid as an external input clock, and TC0GATE<1>=1)

0: TC0 pin signal changes from high to low plus 1

1: TC0 pin signal change from low to high add 1

Bit<3>：PAB-Pre-divider allocates bits

0: predivider is assigned to TC0

1: predivider is assigned to WDT

Bit<2:0> : PSR<2:0>-TC0/WDT pre-divider selection control bit:

PSR2	PSR1	PSR0	TC0 divider coefficient	WDT division coefficient
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Note: When switching between PAB and PSR2 ~ PSR0, the watchdog must be disabled first, and the watchdog can be enabled after the switch is completed.

(Do you need to keep the tips?)

3.2.2 IOPAGE ~ IOC5/P5CON(P5 control register)

05H(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5CON	-	-	P5CON<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P5CON<5:0>-P5 port direction control bit

1: Define the corresponding I/O pin as the high resistance input state

0: Define the corresponding I/O as the output state

3.2.3 IOPAGE ~ IOC6/P6CON(P6 control register)

06H(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6CON	P6CON<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P6CON<7:0>-P6 port direction control bit

1: Define the corresponding I/O pin as the high resistance input state

0: Define the corresponding I/O as the output state

3.2.4 IOPAGE ~ IOC7/P5PD(P5 pull-down control register)

07H(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PD	-	-	P5PD<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P5PD<5:0>-P55 to P50 pin pull-down enable control bit

0: Internal pull-down enable

1: Internal pull-down is forbidden

3.2.5 IOPAGE ~ IOC8/P5PH(P5 pull-up control register)

08H(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PH	-	-	P5PH<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P5PH<5:0>-P55 to P50 pin pull-up enable control bit

0: Internal pull up enable

1: Internal pull-up is forbidden

3.2.6 IOPAGE ~ IOC9/TPRE(TC0/WDT pre-frequency read value register)

09H(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TPRE	TPRE<7:0>							
Read/write	R	R	R	R	R	R	R	R
Reset values	0	0	0	0	0	0	0	1

TC0/WDT predivider value (read only)

3.2.7 IOPAGE ~ IOCB/P6PD(P6 pull-down control register)

0BH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PD	P6PD<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P6PD<7:0>- pull-down enable control bit for P67 to P60 pins

0: Internal pull-down enabled

1: Internal pull-down is forbidden

3.2.8 IOPAGE ~ IOCC/P5OD(P5 open-drain control register)

0CH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5OD	-	-	P5OD<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P5OD<5:0>-P55 ~ P50 pin open drain enable control bit

0: Forbidden

1: Enable

3.2.9 IOPAGE ~ IOCD/P6PH(P6 pull-up control register)

0DH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PH	P6PH<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P6PH<7:0>- Pull-up enable control bit for P67 to P60 pins

0: Internal pull-up enable

1: Internal pull-up is forbidden

3.2.10 IOPAGE ~ IOCE/WDTCON(Watchdog control register)

0EH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTEN	INTS	INTEDG<1:0>		TC0GATE<3:0>			
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	0	0	0	0	0

Bit<7>：WDTEN-WDT the watchdog timer enables control

0: WDT disabled

1: WDT enabled

Note: Watchdog enable requires WDTEN enable and OPTION option [Watchdog] select [Enable].

Bit<6> : INTS- External interrupt port selection

0: External interrupt is P60 port

1: External interrupt is P63 mouth

Bit<5> : INTEDG<1>- External interrupt rising edge triggers control bit

0: External interrupt rising edge trigger forbidden

1: The external interrupt rising edge triggers the enable

Bit<4>：INTEDG<0>-external interrupt drop edge trigger control bit

0: External interrupt falling edge trigger forbidden

1: External interrupt falling edge trigger enable

Bit<3>：TC0GATE<3>-TC0 count gating Enable control 3

0: CMP gating is disabled

1: TC0 count is controlled by CMPOUT, which counts TC0 when CMPOUT=1

Bit<2>：TC0GATE<2>-TC0 count gating Enable control 2

0: INT gating is disabled

1: The TC0 count is controlled by INT, which is low when INTEDG1=1 and high when INTEDG0=1

Bit<1>：TC0GATE<1>-TC0 count gating Enable control 1

0: TC0 external count is disabled

1: TC0 external count enabled (P62 as external count port)

Bit<0>：TC0GATE<0>-TC0 count gating Enable control 0

0: TC2 timing on TC0 external counting function disabled

1:TC2 periodically enables the TC0 external counting function. (P62 serves as the external counting port) When TC2 period overflows, counting is enabled. When the next TC2 period overflows, counting is stopped and TC0GATE<0> automatically clears 0

3.2.11 IOPAGF ~ IOCF/INTE(interrupt enable register)

0FH(IOC)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE	-	P5ICIE	TC2IE	CMPIE	TC1IE	INTIE	P6ICIE	TC0IE
Read/write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7>：unused

Bit<6>：P5ICIE-P5 port input changes the interrupt enable control bit

1: Enable 0: Forbid

Bit<5> : TC2IE-TC2/PWM456 cycle interrupt enable control bit

1: Enable

0: Forbid

Bit<4>：CMPIE-Comparator state change interrupts enable control bit

1: Enable

0: Forbid

Bit<3> : TC1IE-TC1/PWM123 cycle interrupt enable control bit

1: Enable

0: Forbid

Bit<2> : INTIE- External interrupt enable control bit

1: Enable

0: Forbid

Bit<1>：P6ICIE-P6 port input changes the interrupt enable control bit

1: Enable

0: Forbid

Bit<0>：TC0IE-TC0 overflow interrupt enables control bit

1: Enable

0: Forbid

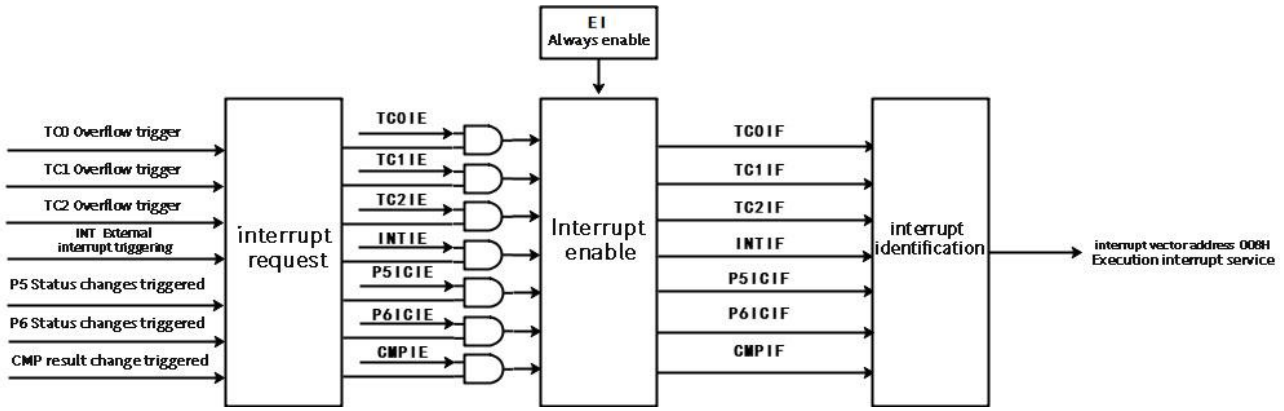
Note: It is no longer necessary to set ICIE=1 for external port wakeup

3.3 Interrupts

JZ8P2521 has 7 interrupt sources, whichever interrupt is used, the total interrupt must be enabled, that is, the "EI" instruction. The interrupt vector is the fixed default address 008H. The following are the characteristics of each interrupt:

Interrupt Type	Interrupt source	Enabling condition	Interrupt flag
Exterior	External interruption	EI + INTIE=1	INTIF
Outside	P5 Port input change interrupt	EI + P5ICIE=1	P5ICIF
Exterior	P6 Port input change interrupt	EI + P6ICIE=1	P6ICIF
Inside	TC0 overflow interrupt	EI + TC0IE=1	TC0IF
Inside	TC1/PWM123 cycle overflow interrupt	EI + TC1IE=1	TC1IF
Inside	TC2/PWM456 cycle overflow interrupt	EI + TC2IE=1	TC2IF
Inside	CMP result change interrupted	EI + CMPIE=1	CMPIF

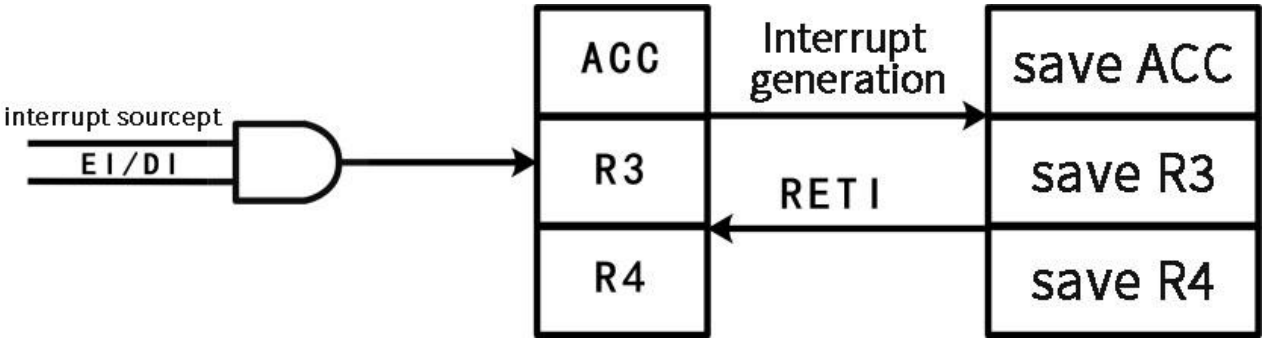
The RF of RPAGE is the interrupt status flag register, which records the interrupt flag bit after an interrupt request is generated. IOCF sets registers for interrupts, and allows and disallows interrupts are set in these two registers. The total interrupt is allowed by the "EI" instruction, and conversely, the total interrupt is forbidden by the "DI" instruction. When an interrupt is generated, the execution of its next instruction will be performed from the interrupt vector address 008H. The corresponding interrupt flag must be reset before leaving the interrupt service routine, so that the wrong action of the interrupt can be avoided.



Schematic diagram of interrupt principle

3.3.1 Interrupt site protection

In the process of responding to interrupts, it is strongly recommended to use interrupt protection in the program. The contents of ACC, R3, and R4 are saved until the interrupt subroutine is left, and the saved values are reloaded into ACC, R3, and R4. This is to avoid instructions to change the values of ACC, R3, and R4 when executing the interrupt subroutine. An error occurred while trying to return to the main program. As shown in the following image:



Schematic diagram of software interrupt site protection

3.4 Reset

3.4.1 Overview of reset function

The JZ8P2521 system provides four reset methods:

- POR Power on reset
- RESET foot input low reset
- WDT Watchdog overflow reset
- LVR low voltage reset

When any of the above reset occurs, all system registers are initialized to the reset value, the program stops running, and the program counter PC is reset. After the reset, the system starts running again from the vector 0000H.

Any reset situation requires a certain response time, and the system reset mechanism can ensure a reliable reset of the MCU. Different types of oscillators require different time to complete reset. Therefore, the rising rate of VDD and the starting time of different oscillators are not fixed. The RC oscillator has the shortest onset time, while the crystal oscillator has a longer onset time. In the process of using the user terminal, attention should be paid to the requirements of the application scene for power on and reset time.

3.4.2 WDT watchdog reset

The watchdog reset is a protective setting for the system. In the normal state, the watchdog timer is reset by the program. If an error occurs, the system is in an unknown state, the watchdog timer overflows, and the system is reset. After the watchdog is reset, the system is restarted into a normal state.

- Watchdog timer state: The system detects whether the watchdog timer is overflowing, if it is overflowing, the system is reset;
- System initialization: all system registers are set to their initial default values;
- Oscillator starts working: The oscillator starts providing the system clock.
- Execute the program: the power on ends, and the program starts to run;

Watch dog timer application notes:

- Check the state of the I/O port and the contents of the RAM before the watchdog is reset to enhance the reliability of the program;
- Do not reset the watchdog in an interrupt, otherwise the main program running cannot be detected;
- The program should only clear the watchdog once in the main program. This structure can maximize the protection function of the watchdog.

3.4.3 POR Power-on reset

Power on reset is closely related to LVR operation. The power-on process of the system is in the form of a gradually rising curve, and it takes a certain time to reach the normal level value.

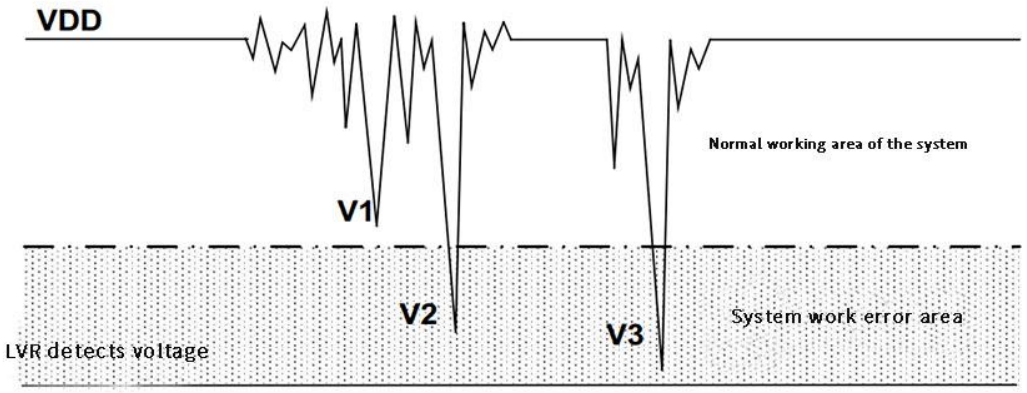
- Power on: the system detects the rise of the power supply voltage and waits for it to stabilize;
- External reset (limited to external reset pin enabled state) : The system detects the external reset pin state. If it is not high, the system remains reset until the external reset pin is released;
- System initialization: all system registers are set to their initial values;
- Oscillator starts working: the oscillator starts to supply the system clock;
- Execute the program: the power on ends, and the program starts to run;

The power-on reset time is determined by the [Reset Time] selection in the OPTION, as shown in the following table:

PWRT vs WDT	Reset setup time
PWRT=WDT	4.5ms(follow watchdog reset time)
PWRT=WDT	18ms(follow watchdog reset time)
PWRT=WDT	72ms(follow watchdog reset time)
PWRT=WDT	288ms(follow watchdog reset time)
PWRT≠WDT	140us(independent fixed reset time)

3.4.4 LVR low voltage reset

Power down reset is aimed at the system voltage sag caused by external factors (e.g., interference or external load changes). Power down may cause abnormal system working status or program execution errors.



The voltage sag may enter the system dead zone. System dead zone means that the power supply does not meet the minimum operating voltage requirements of the system. The figure above is a schematic of a typical power-down reset. In this picture, the VDD is severely disturbed and the voltage drop is very low. Above the dotted line, the system works normally. Below the dotted line, the system enters an unknown operating state. This region is called the dead zone. When VDD drops to V1, the system is still in a normal state; When VDD falls to V2 and V3, the system enters the dead zone, which is prone to errors. The system may enter the dead zone if:

DC in use:

Battery power supply is generally used in DC application. When the battery voltage is too low or the microcontroller drives the load, the system voltage may drop and enter the dead zone. At this time, the power supply will not further drop to the LVR detection voltage, so the system remains in the dead zone.

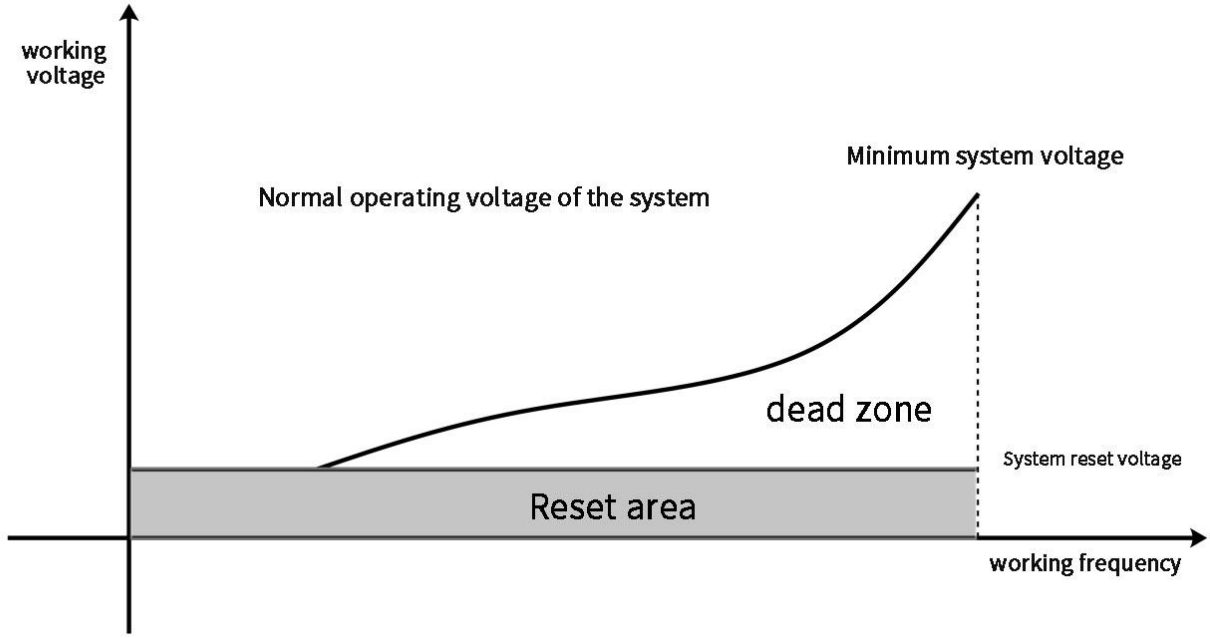
In AC operation:

When the system uses AC power supply, the DC voltage value is affected by the noise in the AC power supply. When the external load is too high, such as when driving the motor, the interference caused by the load action also affects the DC power supply. If the VDD falls below the minimum operating voltage due to interference, the system will likely enter an unstable working

state. In the AC application, the system power on and power off time are long. Among them, the power on timing protection makes the system power on normally, but the power down process is similar to the situation in the DC application. After the AC power is turned off, the VDD voltage is easy to enter the dead zone in the process of slow decline.

3.4.5 Relationship between working frequency and LVR low voltage detection

In order to improve the performance of the system power down reset, first of all, the minimum operating voltage value of the system must be clarified. The minimum operating voltage of the system is related to the execution speed of the system, and the minimum operating voltage value is different under different execution speed.



As shown in the above, the normal work of the system voltage area generally higher than the system reset voltage, at the same time reset voltage is determined by the low voltage detection (as) level. When the system execution speed increases, the minimum operating voltage of the system also increases accordingly. However, since the system reset voltage is fixed, there will be a voltage region between the minimum operating voltage of the system and the system reset voltage. The system will not work properly and will not reset, and this region is called dead zone.

To avoid voltage dead zone, in choosing a working frequency, to select the corresponding points as reset voltage. The following table:

IRC Frequency	Frequency doubling of the system clock	Clocks frequency division	LVR reset voltage point
IRC-8MHz	Frequency doubling	2 Clocks	As = 2.8 V
IRC-8MHz	Not octave	2 Clocks	As = 2.4 V
IRC-1MHz	Frequency doubling	2 Clocks	As = 1.8 V
IRC-1MHz	Not octave	2 Clocks	As = 1.8 V

Note: 1, working frequency = instruction cycle frequency =IRC frequency + Clocks frequency; 2, this working frequency and the corresponding value of the LVR reset voltage point, only recommended value, the user in the use of the process, according to the specific application can be adjusted reset voltage point.

3.5 Working mode

The JZ8P2521 can operate at different clock frequencies in four operating modes, which can control the operation of the oscillator, the execution of the program, and the functional loss of the analog circuit.

- High speed mode: the system clock selects high speed IRC clock;
- Low speed mode: system clock select internal low speed clock;
- Idle mode: the system clock works normally, and other parts go to sleep (TC0, TC1, TC2 select the system clock to continue to work and can wake up the system, and the port state changes can wake up the system);
- Sleep mode: all functions stop working, the system goes to sleep, can be woked up by port state change, WDT overflow, external reset pin input;

Functional modules	High speed mode	Low Speed mode	Idle mode	Sleep mode
IHRC	Run	STPHX control	STPHX controls	Stop
ILRC	Run	Run	Run	Stop
CPU instructions	execute	Execution	Stop	Stop
TC0	Working	Workable	Workable	Stop
TC1	Workable	Workable	Workable	Stop
TC2	Workable	Be available for work	Workable	Stop
Internal interruption	All valid	All valid	Valid for TC0,TC1,TC2	Valid
External interruption	Valid	Effective	Invalid	Valid
Wakeup function	-	-	P5IC,P6IC,TC0,TC1,TC2, WDT, external RESET	P5IC,P6IC,WDT, external RESET
Watchdog timer	WDT option controls	WDT Option control	WDT Option control	WDT Option control

3.5.1 High Speed mode

High-speed mode is the system high-speed clock operation mode, and the system clock source is provided by the high-speed RC oscillator. The program is executed. After a power-on reset or either reset is triggered, the system goes into high speed mode to execute the program. When the system is awakened from sleep mode, it enters high speed mode. In high speed mode, the high speed oscillator works normally and consumes the most power.

- The program is executed and all functions can be controlled;
- The system rate is high;
- Both the high speed oscillator and the internal low speed oscillator work normally;
- Through the CPU mode control register, the system can switch from high speed mode to any other mode.
- After waking up from sleep mode, the system can enter high-speed mode.
- Low speed mode can be switched to high speed mode;
- Enter from high-speed mode to idle mode, wake up and return to high-speed mode;

3.5.2.Slow mode

Low speed mode is the system low speed clock operation mode. The system clock source is provided by the internal low speed RC oscillator. The low-speed mode is controlled by the CLKMD bit of the CPU mode control register. When CLKMD=0, the system is in high speed mode; When CLKMD=1, the system enters the low speed mode. After entering the low speed mode, the high speed oscillator cannot be automatically disabled and must be disabled by SPTHX bit to reduce power consumption.

- The program is executed and all functions can be controlled;
- The system rate is low;
- The internal low-speed RC oscillator works normally, and the high-speed oscillator is controlled by STPHX=1. In low speed mode, it is highly recommended to stop the high speed oscillator;
- Through the CPU mode control register, the low speed mode can be switched into other operating modes;

- From low speed mode to sleep mode, wake up and return to low speed mode;
- High speed mode can be switched to low speed mode;
- Enter from low speed mode to idle mode, wake up and return to low speed mode;

3.5.3 Idle mode

Idle mode is another ideal state. In sleep mode, all functions and hardware devices are disabled, but in idle mode, the system clock is kept working and the power consumption in idle mode is greater than that in sleep mode. In idle mode, the program is not executed, but the timer and PWM with wakeup function are still working normally, and the clock source of the timer and PWM is the system clock that is still working. In idle mode, there are three ways to wake up the system: 1, P5/P6 port status change trigger; 2, TC0 timer wake-up; 3, TC1/TC2 cycle overflow wake-up. The user can set the timer TC0 or TC1, TC2 for a fixed period, and the system will be woked up when the overflow occurs. The CPU mode control register IDLE bit decides whether to enter the IDLE mode. When IDLE=1, the system enters the idle mode.

- The program stops executing and all functions are forbidden;
- The timer with wakeup function works properly;
- The oscillator as the system clock source works normally, and the working status of other oscillators depends on the configuration of the system operating mode;
- Enter from high speed mode to idle mode, return to high speed mode after waking up;
- Enter from low speed mode to idle mode, return to low speed mode after waking up;
- In the idle mode, the wake-up mode was triggered by the change of P5/P6 port state, TC0 timer overflow and TC1, TC2 cycle overflow.
- In idle mode, the functions of TC0, TC1 and TC2 are still valid.

3.5.4 Sleep mode

Sleep mode is the ideal state of the system, the program is not executed, and the oscillator also stops working. The power consumption of the whole chip is below 1uA. Sleep mode can be triggered by P5/P6 port state change to wake up, external reset pin input, WDT overflow. Enter the sleep mode from high speed mode or low speed mode, and return to the corresponding mode after

being woken up. The IDLE bit in the CPU mode control register controls whether to enter sleep mode. When IDLE=0, the system enters sleep mode.

- The program stops executing and all functions are forbidden;
- All oscillators, including the external high speed oscillator, the internal high speed oscillator, and the internal low speed oscillator are stopped working;
- Power consumption below 1uA;
- Enter from high speed mode to sleep mode, and return to high speed mode after waking up;
- Enter into sleep mode from low speed mode, return to low speed mode after waking up;
- The wake-up source of sleep mode was triggered by the input change of P5 and P6 ports, the input of external reset pin, and the overflow of WDT.

3.6 System clock

JZ8P2521 is integrated with two kinds of oscillators, namely, high speed oscillator IHRC and low speed oscillator ILRC. The system clock can be switched by corresponding configuration. Please refer to the table below for details:

Oscillator types	High speed mode	Low Speed mode	Instructions
IHRC	Run	-	IRC frequency selection is configured via OPTION: 910KHz/1MHz/8MHz
ILRC	-	Run	Default 16KHz

Note: High and low speed mode switching is achieved through STPHX bit and CLKMD bit of CPUCON register.

3.6.1 Internal RC oscillator

The JZ8P2521 provides internal IHRC and ILRC, and the IHRC frequency defaults to 8MHz.

The IHRC oscillation mode includes three frequency values of 8MHz, 1MHz and 910KHz. The IRC operating frequency can be selected by setting the configuration bit of the OPTION, and the following is their corresponding relationship:

Oscillator frequency	IRC frequency
8 M	The IRC frequency is chosen to be 8MHz
1 M	The IRC frequency is chosen to be 1MHz
910K	The IRC frequency was chosen to be 910KHz

JZ8P2521 provides a variety of instruction clock frequency division options, the system defaults to 2 frequency division. This can be selected in the OPTION configuration, as shown in the following table:

Clocks	Clocks frequency division
2clock	Frequency division is 2clock
4clock	The frequency division is 4clock
8clock	The frequency division is 8clock
16clock	The frequency division is 16clock
32clock	Frequency division is 32clock

3.7 I/O port

JZ8P2521 has 2 sets of bidirectional I/O ports, 14 inputs and 14 outputs in total, most of the I/O can be reused for other functions.

8 driver enhanced I/O pins: P60 to P67;

6 configurable selectable driver enhanced I/O pins: P50 to P55;

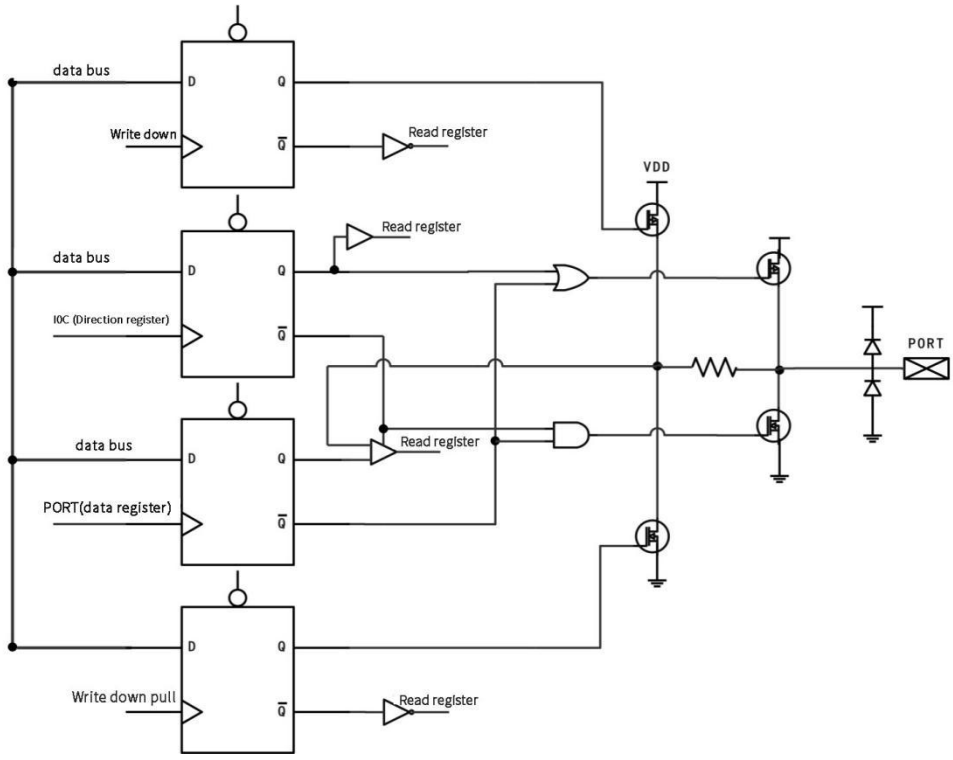
14 programmable pull-up I/O pins: P50 to P55, P60 to P67;

14 programmable pull-down I/O pins: P50-P55, P60-P67;

14 programmable port state change wake-up I/O pins: P50 ~ P55, P60 ~ P67;

3.7.1 Internal structure diagram of GPIO

The following internal structure diagram is for reference only and does not represent the actual circuit.



IO control register/data register/pull-up/pull-down structure circuit

3.7.2 Port state change wake-up

The JZ8P2521 contains 14 programmable port state change wake-up I/ OS: P50 to P55, P60 to P65. The chip can enter the SLEEP mode by executing the "sleep" command. At this time, the

system clock stops, all modules stop working, WDT (if enabled) clear 0, but continue to run. Port state change wake-up can be selected by the program to continue the original process (execute DI before SLEEP) or execute the corresponding jump (execute EI before SLEEP), and open the corresponding enable control bit, jump to the interrupt subroutine.

Port input change query mode wake up Settings

1, P5/P6 port wakeup port set as input;

2. The internal pull up or pull down of the wake up port can be selected according to the need;

3, enable P5/P6 port input change interrupt;

4, enable port input change independent interrupt and wake-up control;

Execute DI instruction, do not enter the interrupt address port;

6. Execute the "SLEEP" command to enter the SLEEP mode.

7. After waking up, execute the next command of SLEEP;

Port input changes interrupt mode wake up Settings

1. The wake-up port of P5/P6 is set as input;

2. The internal pull up and down of the wake-up port can be selected according to the need;

3, enable port input change independent interrupt and wake-up control;

4, enable P5/P6 port input change interrupt;

Execute "EI" instruction and wait to enter the interrupt address port;

6. Under the command "SLEEP", enter the SLEEP mode;

7. After waking up, it will enter the interrupt address port, exit the interrupt, and execute the next instruction of SLEEP;

3.7.3 Port Schmidt parameter

The Schmidt characteristics of the JZ8P2521 port are shown in the following table (for reference only) :

Port	SMT
P6.3	0.51 * VDD
P6.0 ~ P6.2	0.26 *VDD / 0.55 * VDD
P6.4 ~ P6.5	0.26 *VDD / 0.55 * VDD

The above parameters are for reference only, please refer to the actual measured data of the target prototype.

3.8 Timing counter

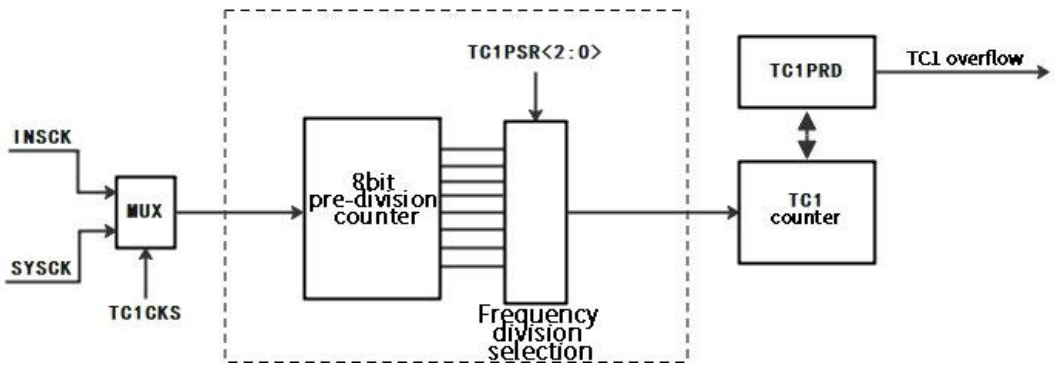
3.8.1 TC0 timing counter

The JZ8P2521 provides an 8-bit counter as a pre-divider for TC0 and WDT. The predivider is used only for TC0 or only for WDT at the same time, and the PAB bit in the TC0CON register determines the allocation of the predivider. PSR0 ~ PSR2 three bits determine the pre-division ratio. In TC0 mode, every time TC0 is written a value, the pre-division register is reset. When the predivider is assigned to WDT mode, the values of the WDT and predivider registers are reset when the "CWDT" or "SLEEP" instruction is executed. If the predivider is assigned to TC0 and then to WDT, the contents of the predivider counter will be automatically cleared, and vice versa.

TC0 is an 8Bit uplink counter that works whenever there is a clock. The clock source can be either a system clock, an instruction cycle clock, or a low-speed oscillator clock (triggered by the rising edge), or an external clock can be selected (entered by the TC0 pin, and the trigger edge is optional), if there is no frequency division control, each clock edge arrives and the counter is implemented incremented by 1. The system provides an 8Bit counter as a pre-divider for TC0. The TC0 predivider, signal trigger edge, clock source, etc. can be set through the TC0CON register.

A TC0 count overflow can form an interrupt signal.

In the IDLE mode, the TC0 interrupt can wake up the circuit, after waking up, you can choose to interrupt or continue to execute the original program, the method refers to the port state change to wake up.



TC0/WDT structure block diagram

3.8.1.1 TC0 timing setup instructions

- Assign an initial value to the TC0 register;
- Set the value of TC0CON register (select clock predivision, signal trigger edge, clock source);
- To use as a counter, you need to select the TC0 external signal in the TC0CON register for the positive edge or negative edge plus 1;
- If you need to execute the interrupt function, you must set TC0IE (Bit0) in the IOCF register to 1, and execute EI instruction;
- The interrupt program part will manually save ACC, STATUS and R4 in the stack, after executing the RETI instruction, and then take it out from the stack, clear the TC0 interrupt flag bit before exiting the interrupt;

3.8.1.2 TC0 timing calculation instructions

The TC0 timing function assigns the initial value to the timer by writing a value to the TC0 register, and the timer starts to accumulate from the initial value position until the timer overflows and interrupts.

TC0 timing time calculation formula (select internal instruction cycle clock) :

$$\text{TC0 timing time} = (\text{System clock frequency division/Fosc}) \times (\text{TC0fractional frequency}) \times (256 - \text{TC0initial value})$$

Example:

System clock division =2clock, Fosc=8 MHz, TC0 division selection =4 division, TC0 initial value =156;

$$\text{TC0 timing time} = (2/8) \times (4) \times (256 - 156) = 100\ \text{us}$$

TC0 timing time calculation formula (select external input clock) :

$$\text{TC0 timing time} = (\text{External input clock}) \times (\text{TC0fractional frequency}) \times (256 - \text{TC0initial value})$$

Example:

External input clock =1 MHz, TC0 divider selection =4 divider, TC0 initial value =156;

$$\text{TC0 timing time} = (1) \times (4) \times (256 - 156) = 400\ \text{us}$$

3.8.1.3 Description of TC0 timing gating

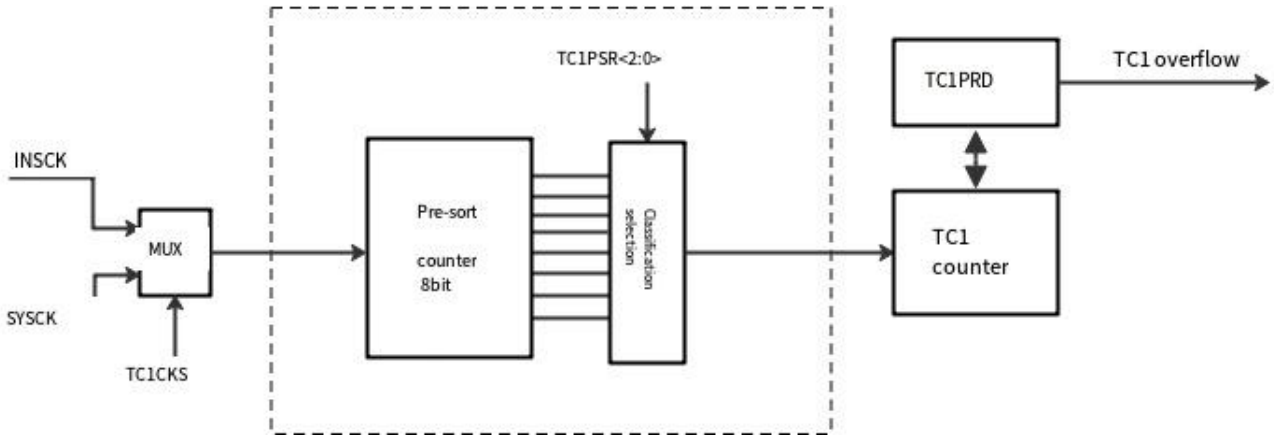
The gating function of the TC0 timer is controlled by TC0GATE<3:0> in the WDTCON register.

When TC0GATE<0>=1, TC2 regularly turns on the TC0 external counting function (P62 as an external counting port) and enables counting when TC2 cycle overflows, and stops counting when the next TC2 cycle overflows and TC0GATE<0> automatically clers 0.

When TC0GATE<1>=1, TC0 external counting is enabled (P62 is used as external counting port);

When TC0GATE<2>=1, the TC0 count is controlled by INT, when INTEDG1=1 INT is low TC0 count, when INTEDG0=1 INT is high TC0 count;

When TC0GATE<3>=1, the TC0 count is controlled by CMPOUT, when CMPOUT=1, the TC0 count.



3.8.2 TC1 timing counter

The TC1 timing counter provides an 8-bit predivider, and the TC1PSR<2:0> three bits of the TC1CON register determine the predivider ratio. Enable TC1PTEN after each TC1EN/TC21EN enable in TC1 mode, and the predivision counter starts to work.

TC1 is a 10Bit uplink counter. TC1 timer needs to enable TC1EN/TC21EN to work, the clock source is the internal instruction clock/internal system clock, each clock cycle arrives, the counter is incremented by 1. The TC1 count value is consistent with the TC1PRD register set value to produce overflow. If TC1IE and EI are enabled, the system jumps to the corresponding interrupt vector address, and the interrupt service program is executed.

In IDLE mode, TC1 interrupt can wake up the circuit (clock select system clock), after waking up, you can choose to enter the interrupt or continue to execute the original program, the method refers to the change of port state to wake up.

TC1 structure block diagram

3.8.2.1 TC1 timing calculation instructions

The TC1 timing function generates a TC1 timing interrupt by writing a value to the TC1PRD register, when the TC1 timer count value is consistent with the TC1PRD value.

TC1 timing time calculation formula:

$$\text{TC1 timing time} = (1/\text{Fosc}) \times (\text{TC1 fractional frequency}) \times (\text{TC1PRD})$$

Example:

Fosc=1 MHz, TC1 divider selection =4 divider, =500;TC1PRD

$$\text{TC1timing time} = (1/1) \times (4) \times (500) = 2000\text{us}$$

3.8.2.2 TC1 10Bit timing setting instructions

1. Assign initial values to TC1PRDL and TC1PRDH registers;

2. Set the TC1CON register, enable automatic loading and configure the pre-frequency ratio on demand;

Enable TC1EN, open the TC1 timer count;

4. If you need to execute the interrupt function, set the TC1IE (Bit0) in the IOCF register to 1, and execute the EI instruction;

5. The interrupt program part will manually save ACC, STATUS and R4 in the stack, and then take out from the stack after executing the RET instruction;

3.8.3 TC2 timing counter

The TC2 timing counter provides an 8-bit predivider, and the TC2PSR<2:0> three bits of the TC2CON register determine the predivider ratio. Enable TC2PTEN after each TC2EN/TC21EN enable in TC2 mode, and the predivision counter starts to work.

TC2 is a 10Bit uplink counter. TC2 timer needs to enable TC2EN/TC21EN to work, the clock source is the internal instruction clock/internal system clock, each clock cycle arrives, the counter is incremented by 1. The TC2 count value is consistent with the TC2PRD register set value to produce overflow. If TC2IE and EI are enabled, the system jumps to the corresponding interrupt vector address, and the interrupt service program is executed.

In IDLE mode, TC2 interrupt can wake up the circuit (clock select system clock), after waking up, you can choose to enter the interrupt or continue to execute the original program, the method refers to the change of port state to wake up.

TC2 structure block diagram

3.8.3.1 TC2 timing calculation instructions

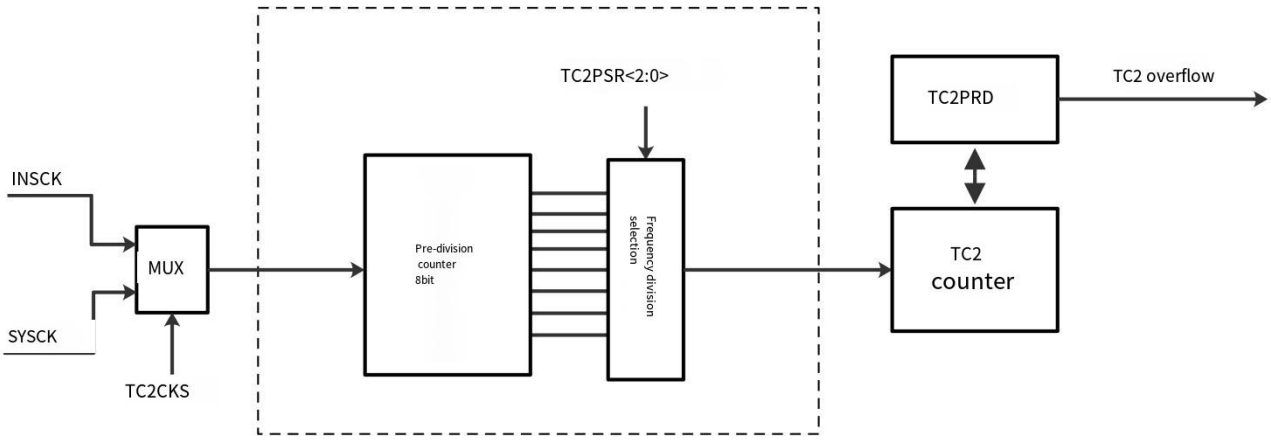
The TC2 timing function generates a TC2 timing interrupt by writing a value to the TC2PRD register when the TC2 timer count value is consistent with the TC2PRD value.

TC2 timing time calculation formula:

$$\text{TC1 timing time} = (1/\text{Fosc}) \times (\text{TC1fractional frequency}) \times (\text{TC2PRD})$$

Example:

Fosc=1 MHz, TC2 divider selection =4 divider, TC2PRD=1000;



$$\text{TC1 timing time} = (1/1) \times (4) \times (1000) = 4000\text{us}$$

3.8.3.2 TC2 10Bit timing setting instructions

1. Assign initial values to TC2PRDL and TC2PRDH registers;

2. Set the TC2CON register, enable automatic loading and configure the pre-frequency ratio on demand;

3, enable TC2EN, open TC2 timer counting;

4. If you need to execute the interrupt function, set the TC2IE (Bit0) in the IOCF register to 1, and execute the EI instruction;

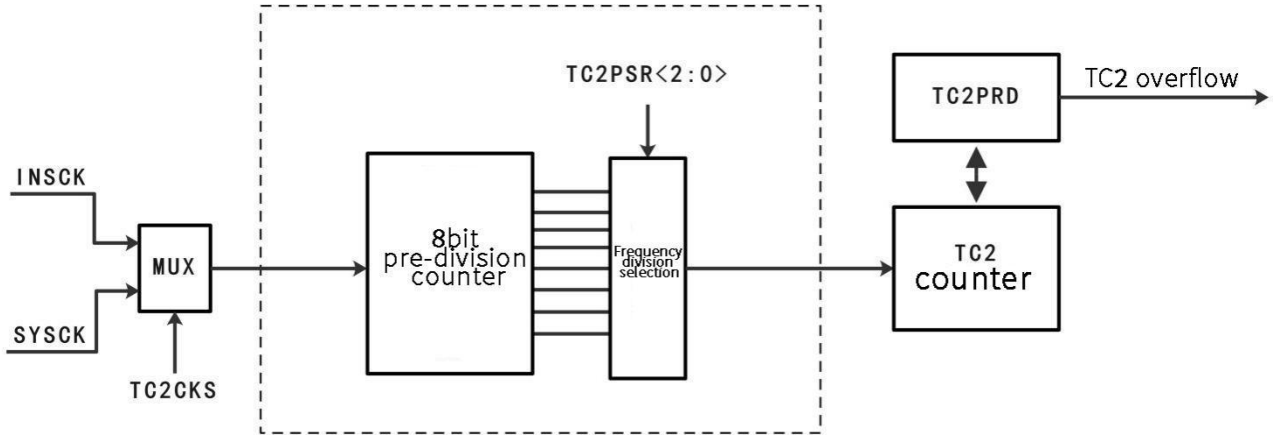
5. The interrupt program part will manually save ACC, STATUS and R4 in the stack, and then take out from the stack after executing the RET instruction;

3.9 PWM pulse width modulation

The JZ8P2521 provides 2 sets of 10 bit TC1 and TC2 counters, which are used to generate 2 sets of pulse width modulation signals with common period. PWM1, PWM2, PWM3 are a group of pulse width modulation signals sharing TC1 counter, PWM4, PWM5, PWM6 are a group of pulse width modulation signals sharing TC2 counter.

TC1 and TC2 have a periodic overflow interrupt, and when enabled, they can jump to the interrupt vector address when the counter matches the periodic value.

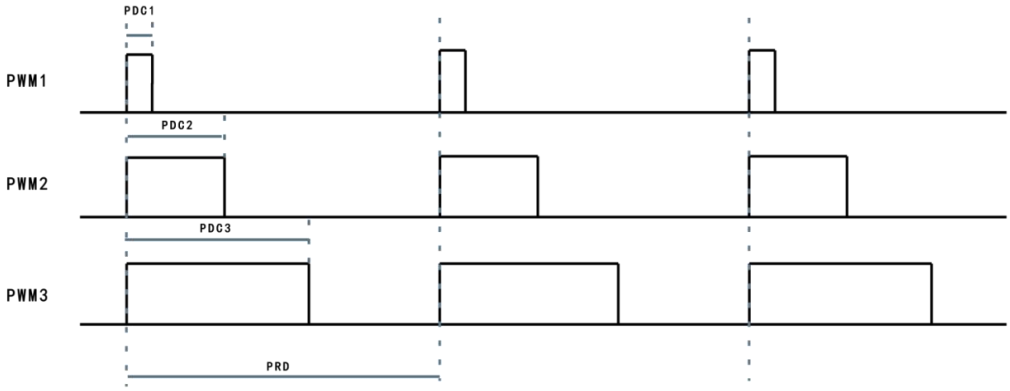
In IDLE mode, TC1 and TC2 can wake up the system by selecting TC1CKS=1 and TC2CKS=1 in TC1 and TC2 control registers and enabling TC1WE and TC2WE in CPU mode control registers.



3.9.1 PWM internal structure and timing

The following internal structure diagram is for reference only and does not represent the actual circuit.

PWM working structure circuit



3 way common cycle PWM timing instructions

3.9.2 PWM cycle and duty cycle

PWM1, PWM2, and PWM3 share a clock divider and a 10bit counter (TC1 counter), and the TC1 counter serves as the baud rate clock generator for the PWM123. By enabling TC1 to control the TC1EN in the register, the TC1 counter function can be enabled. Through the TC1PTEN and TC1PSR<2:0> control bits, the TC1 counter can be predivided.

The PWM4, PWM5, and PWM6 share a clock divider and a 10bit counter (TC2 counter), which is used as the baud rate clock generator for the PWM456. TC2 can be enabled to control the TC2EN in the register, enable the function of the TC2 counter, through the TC2PTEN and TC2PSR<2:0> control bit, the TC2 counter can be pre-frequency set.

The principle of TC2 and TC1 is the same, and TC1 is taken as an example below.

The PWM cycle writes values to the PWM cycle registers (TC1PRDTH, TC1PRDL). When the value of the TC1 counter is equal to the TC1PRD value, the following event occurs in the next increment cycle:

- The TC1 counter clears;
- Corresponding PWM output pin high level;
- Generate PWM cycle overflow interrupt (if enabled);

PWM cycle calculation formula:

$$\text{PWM cycle} = (\text{PRD}) \times (\frac{1}{Fosc}) \times (\text{T1 frational frequency})$$

Example:

TC1PRD=100, Fosc=8 MHz, TC1 divider selection =2 divider;

$$\text{PWM cycle} = (100) \times \left(\frac{1}{8}\right) \times (2) = 25 \text{ us}$$

PWM duty cycle calculation formula:

$$\text{PWM duyt cycle} = (\text{PWMDT}) \times (\frac{1}{Fosc}) \times (\text{T1fractional frequency})$$

Example:

PWMDT=50, Fosc=8 MHz, T1 divider selection =2 dividers;

$$\text{PWM duyt cycle} = (50) \times \left(\frac{1}{8}\right) \times (2) = 12.5 \text{ us}$$

3.9.3 PWM gating function description

The PWM1 gating function is controlled by the PWM1GATE of the TC1CON register. When PWM1GATE=1, the PWM1 output is controlled by the comparator result, that is, the output PWM waveform when CMPOUT=0.

The gating function of PWM4 is controlled by PWM4GATE<1:0> of the TC2CON register. When PWM4GATE<0>=1, the PWM4 output is controlled by the comparator result, that is, the output PWM waveform when CMPOUT=0. When PWM4GATE<1>=1, the PWM4 output is controlled by an external interrupt INT (P60 or P63), and the PWM waveform is output when an external interrupt INT=1.

3.9.4 PWM dead-time complementary function description

PWM1 and IPWM1 form a set of dead-zone complementary PWMS, and PWM4 and IPWM4 form a set of dead-zone complementary PWMS. PWM1 and IPWM1 are used for illustration, and the same is true for PWM4 and IPWM4.

IPWM1 is the output of PWM2 and PWM3 after XOR. When IPWM1EN is enabled, MCU will automatically enable PWM2 and PWM3, and the waveforms of PWM2 and PWM3 are logically XOR. If PWM2EN is enabled, IPWM1 will output through PWM2 port, and PWM2S will select P51/P61. If PWM3EN is enabled, IPWM1 will output through PWM3 port, and PWM3S will

select P50/P60. At the same time, enable to support IPWM1 waveform output from two ports at the same time.

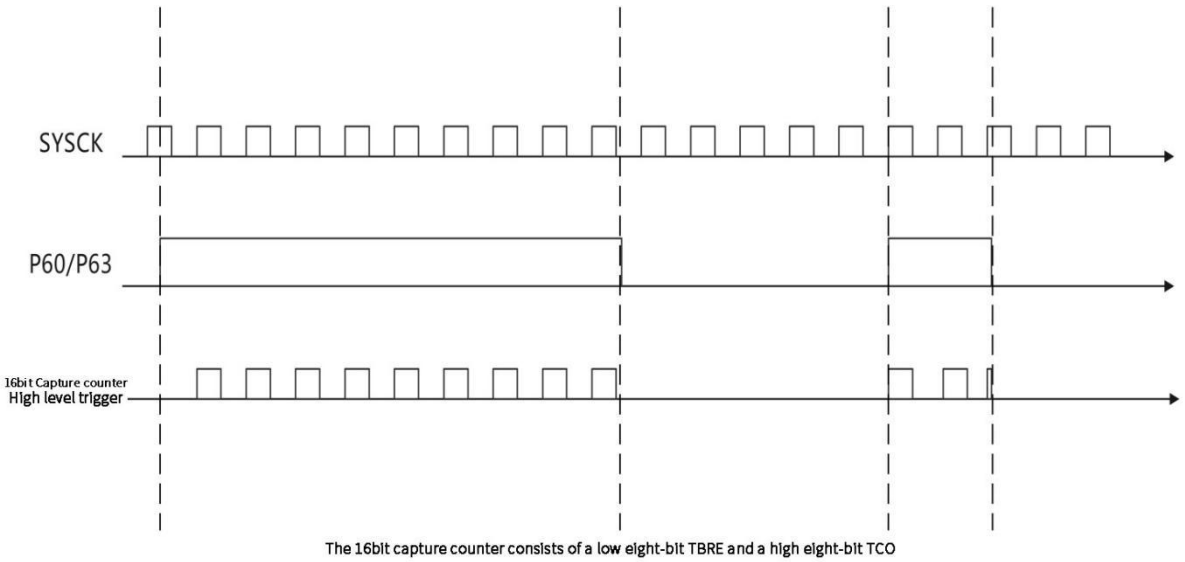
3.9.5 PWM pulse width modulation setup instructions

- Set CPUCON register, select TC1/TC2 wake-up function;
- Set the TC1CON /TC2CON registers, and select the corresponding PWM mode, PWM gate, PWM clock source and PWM frequency division ratio.
- Set PWMCON0/PWMCON1 register, select the corresponding PWM enable, IPWM take the inverse output, PWM output channel;
- Set the value of PWM cycle and duty cycle register;
- Enable PWM cycle overflow interrupt and execute "EI" or "DI" instruction (if necessary);

3.10 Port level capture

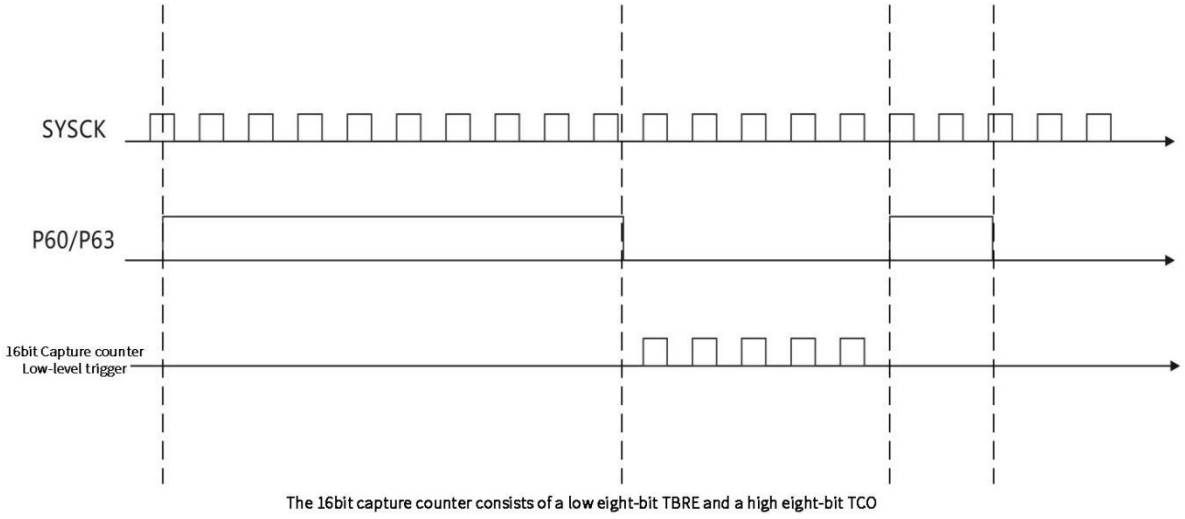
The JZ8P2521 provide s P60/P63 port level capture. By multiplexing the TC0 8Bit predivider TPRE (as the level capture counter low 8 bits) and the 8Bit counter TC0C (as the level capture counter high 8 bits) combination of 16Bit level capture counter, while with the external interrupt to achieve the level change trigger interrupt, in the interrupt program to determine the acquisition time of the last level. The external interrupt can be triggered by IOCE/WDTCON register INTEDG<1:0> to select the trigger edge, and INTS to select the external interrupt input port.

Description of the P60/P63 port high level capture function. First, set IOCE/WDTCON register **TC0GATE<2>=1** to select the TC0 counter controlled by the external interrupt level, while enabling **INTEDG<0>=1 external interrupt falling edge trigger function, enabling external interrupt, TC0CON register to select the TC0 clock source as the system clock, and finally enable TC0EN=1**. When the P60/P63 port is high, the TC0 predivider and counter start counting, the counting clock is the system clock, and the P60/P63 port is low, the TC0 predivider and counter stop counting, and the falling edge of the port trigger the external interrupt. The user can calculate the level time by reading the counts of R1/TC0C and IOC9/TPRE registers in the interrupt program.



The P60/P63 port low level capture is similar to the high level. First set the IOCE/WDTCON register **TC0GATE<2>=1** to select the TC0 counter controlled by the external interrupt level, while enabling **INTEDG<1>**=1 **external interrupt rising edge trigger function, enable external**

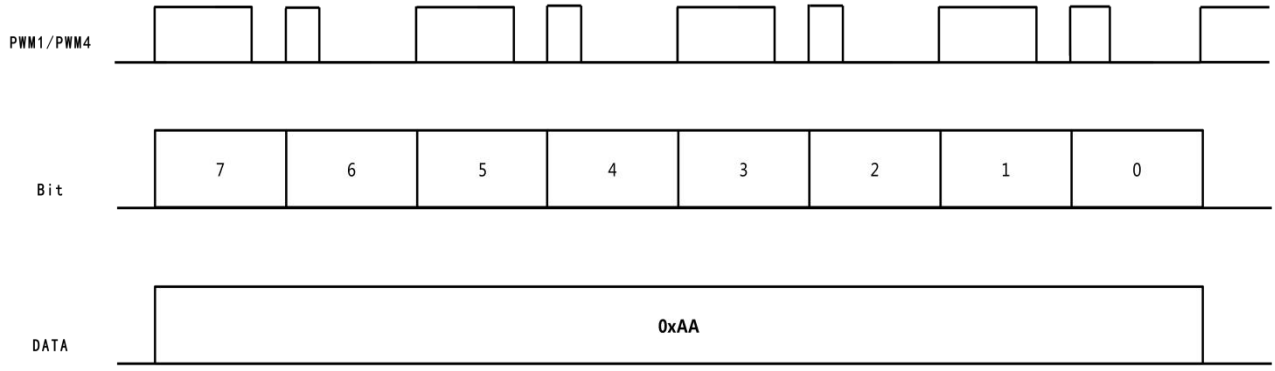
interrupt, TC0CON register selects the TC0 clock source as the system clock, and finally enable TC0EN=1. When the P60/P63 port is low, the TC0 pre-divider and counter start counting, the counting clock is the system clock, and the P60/P63 port is high, the TC0 pre-divider and counter stop counting, and the rising edge of the port trigger external interrupt. The user can calculate the level time by reading the counts of R1/TC0C and IOC9/TPRE registers in the interrupt program.



The 16bit capture counter consists of a low eight-bit TBRE and a high eight-bit TCO

3.11 LED single wire cascade

JZ8P2521 supports 2 single-wire cascaded LED driver, PWM1, PWM4 port output cascade control timing. Cascaded LED driver timing illustration diagram is as follows:



Single-wire cascaded LED timing illustration

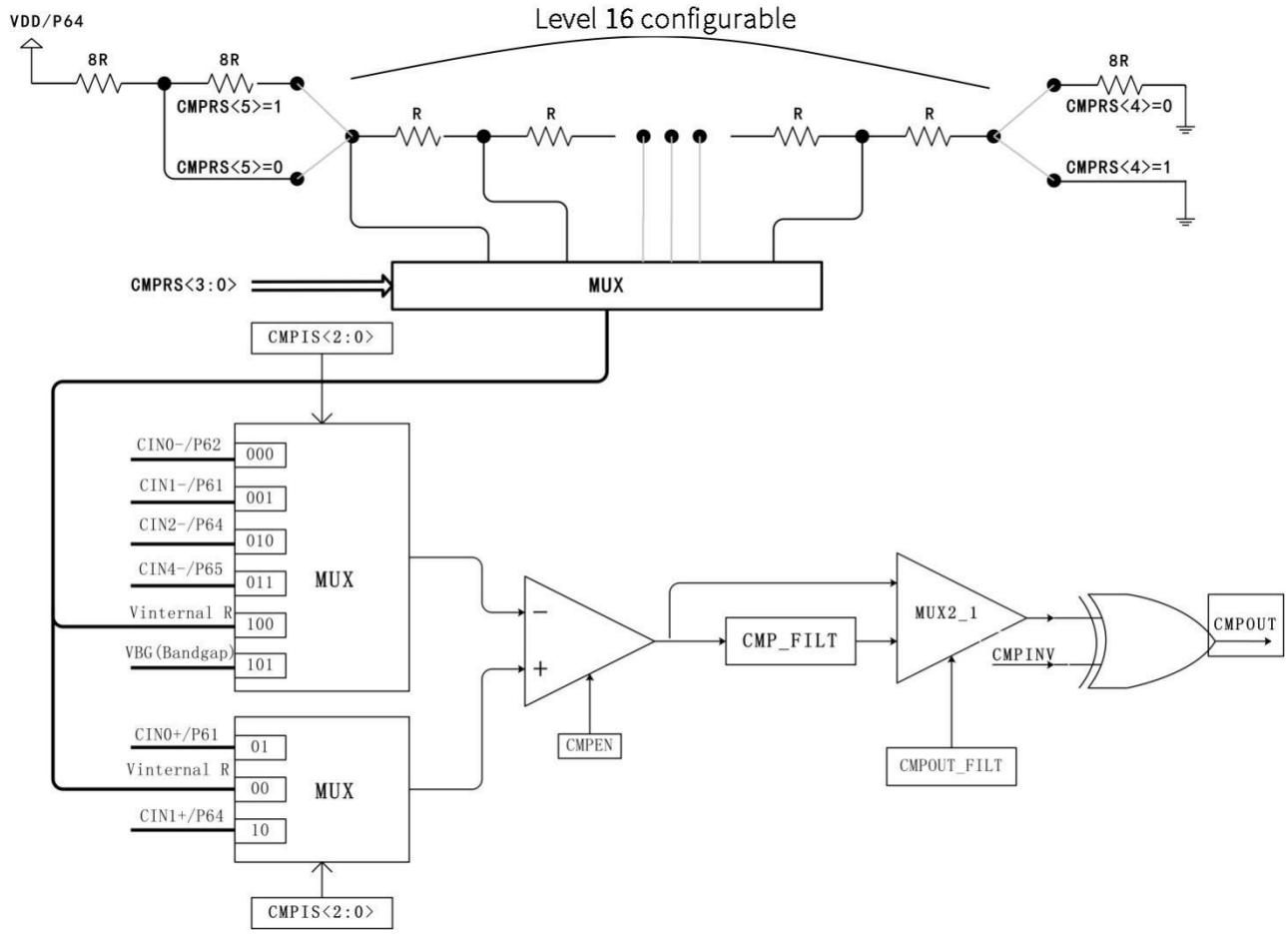


PWM1 and PWM4 are two independent single-wire cascaded LED drive controls. When PWM1 is used as the LED driver control, the high level time of code 0 is set by the duty cycle register of PWM1, code 1 is set by the duty cycle register of PWM2, and the period of code data is set by the TC1PRD cycle register. After enabling PWM1_LEDEN+TC1EN, the 8-bit cascade data is sent, and the data is output by the PWM1 port. TC1EN automatically reset and reset after the end of the 8-bit cascade data transmission, reset TC1EN to start the next 8-bit cascade data transmission.

When PWM4 is used as the LED driver control, the high level time of code 0 is set by the duty cycle register of PWM4, the high level time of code 1 is set by the duty cycle register of PWM5, and the period of code data is set by the cycle register of TC2PRD. After PWM4_LEDEN+TC2EN is enabled, 8-bit cascade data is sent, and the data is output by the PWM4 port. TC2EN automatically reset and reset after the end of the 8-bit cascade data transmission, reset TC2EN to start the next 8-bit cascade data transmission.

3.12 CMP comparator

The JZ8P2521 has a built-in hardware comparator that can compare any two of the input pin, the internal reference voltage $V_{internal\ R}$, and the built-in Bandgap (1.26v), selecting one as a positive input and the other as a negative input. The negative input of the comparator can be P61, P62, P64, P65, divider resistor (selected by CMPRS<5:0>), built-in Bandgap (1.26v). The positive input to the comparator can be P61, P64, divider resistor (selected by CMPRS<5:0>). (The same port cannot be used as both positive and negative inputs, nor can the voltage divider input source be used as both positive and negative.)



Comparator schematic illustration

The divider resistor can be configured via CMPCON control register to select the input voltage source as P64 port input or VDD.

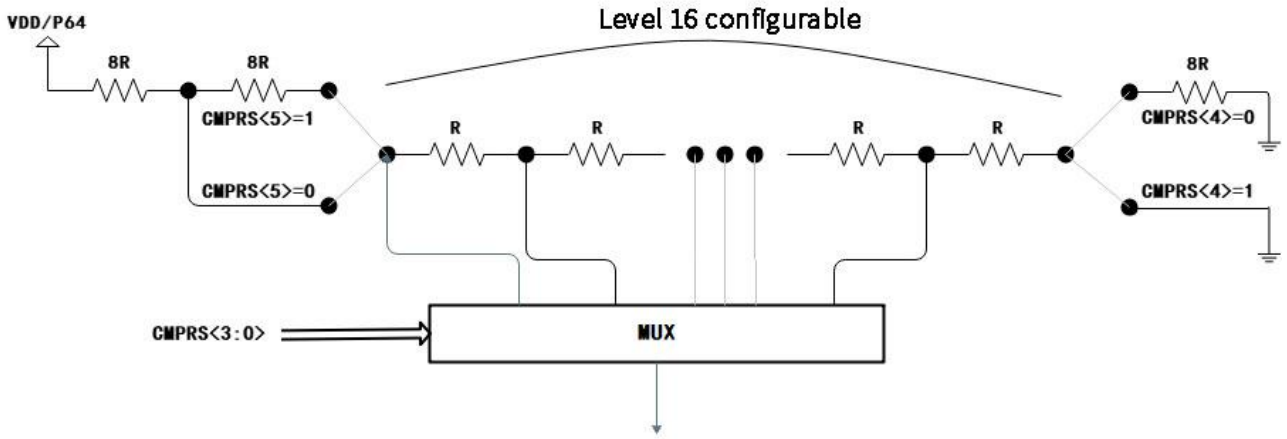
The output result of the comparator can be selected as P60 port output, and the output is supported to be negative. The chip supports digital filtering of output results, which can be selected in OPTION.

Comparator support output result change trigger interrupt, enable CMPIE can generate interrupt signal.

Comparator supports output result change wake-up, enable CMPWE can wake up the idle mode and sleep mode. In idle mode and sleep mode, if CMPEN is enabled, the low-speed oscillator will be enabled, and the sleep power consumption will become high.

3.12.1 Divider resistor output voltage Vinternal R

The output voltage $V_{internal\ R}$ of the divider resistor is composed of a series of resistors that can generate different levels of reference voltage. CMPRS<5:0> jointly determines the size of $V_{internal\ R}$, CMPRS<5> and CMPRS<4> select the highest and lowest value of $V_{internal\ R}$, CMPRS<3:0> is used to select the desired voltage level, is from the highest and lowest value of $V_{internal\ R}$ evenly divided into 16 equal parts, selected by CMPRS<3:0>.



Schematic diagram of comparator adjustment

例 1：CMPRS<5>=0，CMPRS<4>=0

Range of values:$V_{internal\ R} = (3/4) * VDD \sim (1/4) * VDD + (1/32) * VDD$

Formula:$V_{internal\ R} = (1/4) * VDD + \frac{(n+1)}{32} * VDD$

例 2：CMPRS<5>=0，CMPRS<4>=1

Range:$V_{\mathbf{internal\ R}} = (2/3) * VDD \sim (1/24) * VDD$

Formula:$V_{\mathbf{internal\ R}} = \frac{(n+1)}{24} * VDD$

例 3：CMPRS<5>=1，CMPRS<4>=0

Range of values:$V_{\mathbf{internal\ R}} = (3/5) * VDD \sim (1/5) * VDD + (1/40) * VDD$

Formula:$V_{\textbf{internal R}} = (1/5) * VDD + \frac{(n+1)}{40} * VDD$

例 4：CMPRS<5>=1，CMPRS<4>=1

Range of values:$V_{\textbf{internal R}} = (1/2) * VDD \sim (1/32) * VDD$

Formula:$V_{\textbf{internal R}} = \frac{(n+1)}{32} * VDD$

n=CMPRS<3:0>

3.12.2 Comparator configuration

Enable CMPEN when using the comparator, set CMPIS<5:0> to select positive and negative input sources, and set the ports of positive and negative electrodes as input. The same port cannot be used as positive and negative inputs at the same time, and the voltage divider input source cannot be used as positive and negative electrodes at the same time.

If the resistor voltage divider is selected as the input source, set the register CMPRS<5:0> according to the need, and select the required voltage divider resistor output voltage $V_{\textbf{internal R}}$ for comparison.

Example 1:

Choose P62 as the negative end input and the voltage of $V_{\textbf{internal R}}$ as (18/32)*VDD as the positive input, $V_{\textbf{internal R}}$ choose the configuration mode of CMPRS<5>=0, CMPRS<4>=0, CMPRS<3:0>=4b '1001 (n=9) to obtain

Vinternal R = (1/4)*VDD + [(9+1)/32]*VDD = (18/32)*VDD

When the configuration is completed, enable CMPCON0(R7) control register of Bit7 bit CMPEN, the comparator starts to compare, and can configure CMPCON1 (R8) control register of Bit7 bit CMPOE to select P60 port to output the comparison results (P60 port needs to be set as output), The output result can also be negated by the Bit6 bit CMPINV configured to control the register

3.12.3 Bandgap Usage

The built-in Bandgap reference voltage can provide a voltage of 1.26V, which measures the external supply voltage level. This can be achieved by selecting the Bandgap reference voltage for negative input to compare with the positive input Vinternal R. The power supply of Vinternal R is set to VDD, and the voltage of VDD can be known by comparing the Vinternal R voltage level

with the Bandgap reference voltage. If n (CMPRS[3:0] decimal) is set so that Vinternal R is closest to 1.26V, using the four cases in 3.10.1 as an example, the voltage of VDD can be calculated using the following formula:

For using Case 1: VDD = [32/(n+9)] * 1.26V;

For using Case 2: VDD = [24/(n+1)] * 1.26V;

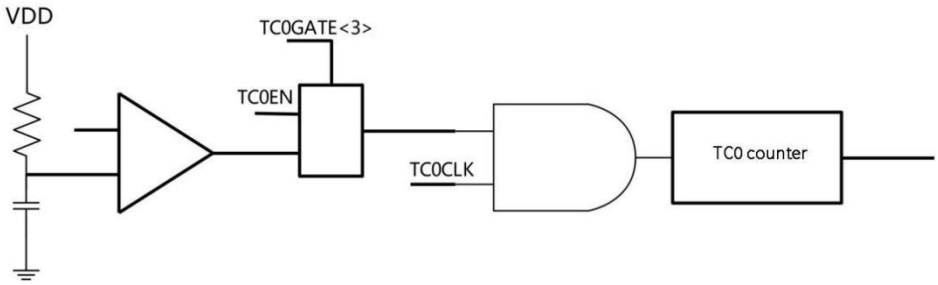
For using Case 3: VDD = [40/(n+9)] * 1.26V;

For using Case 4: VDD = [32/(n+1)] * 1.26V;

3.13 RFC resistor frequency conversion

JZ8P2521 built-in RFC resistance frequency conversion function, by selecting the TC0 counting gate source as the comparator output result, to achieve the time count of external voltage change.

The specific implementation is: enable the TC0GATE<3> of the **WDTCON** register, select the TC0 count controlled by CMPOUT, when CMPOUT=1, TC0 start counting, CMPOUT=0, TC0 stop counting. Configure the comparator function through **CMPCON0**, **CMPCON1**, P6AE registers, first enable the required analog port, set the positive input source of the comparator as a fixed level, and select the negative input source of the comparator as an external port. As shown in the figure, first set the port of the negative input source to the output high level, then the comparator result output bit CMPOUT=0, the TC0 timer does not count, set the initial value of the TC0 timer. When the port of the positive input source is set as the input port, the RC circuit on the port starts charging, when the port voltage is lower than the level of the positive input source, TC0 starts counting, when the port voltage is higher than the level of the positive input source, TC0 stops counting, TC0 is equivalent to recording the charging time of RC.



RFC structure illustration diagram

4.OPTION configuration sheet

CODE OPTION	Options	Feature Description
Watchdog	Enable	Watchdog WDT enabled
	Forbidden	Watchdog WDT prohibited
Clocks split frequency	2 Clocks	Choose 2 Clocks for the instruction cycle
	4 Clocks	Choose 4 Clocks for the instruction cycle
	8 Clocks	Choose 8 Clocks for the instruction cycle
	16 Clocks	Choose 16 Clocks for the instruction cycle
	32 Clocks	Select 32 Clocks for instruction cycles
IRC oscillator voltage source selection	Choose VDD voltage for IRC	The VDD voltage is chosen as the IRC oscillator voltage source
	Choose LDO voltage for IRC	IRC oscillator voltage source Select LDO voltage
IRC frequency	8M	Choose 8M for IRC frequency
	1M	Choose 1M for IRC frequency
	910KHz	Choose 910KHz for IRC frequency
System clock frequency multiplier selection	Forbidden	No doubling of the system clock is selected
	Enable	Select frequency doubling of system clock (system clock is the basic clock running inside the chip, CPUCON register can configure the system clock to low speed or high speed mode, pay attention to the difference with oscillator frequency doubling)
Low-voltage reset option	Enable: Software control	Enable the LVR function, the specific control is controlled **by the STATUS** register LVREN bit
	Forbid: Force forbid	The LVR function is forbidden by the hardware, the LVREN bit of the **STATUS** register is invalid, and the risk of entering the dead zone should be noted
Low voltage reset point selection	As = 1.2 V	Choose 1.2V for the low voltage reset point
	As = 1.6 V	Choose 1.6V as the low voltage reset point
	As = 1.8 V	Choose 1.8V as the low voltage reset point
	As = 2.4 V	Choose 2.4V as the low voltage reset point
	As = 2.7 V	The low voltage reset point is selected as 2.7V
	As = 3.3 V	Choose 3.3V as the low voltage reset point
	As = 3.6 V	Choose 3.6V for the low voltage reset point
	As = 3.9 V	Choose 3.9V as the low pressure reset point
OTP paging	Use 2K	Select 2K for the ROM area

	Use the first 1K	Select the first 1K for the ROM area
	Use the last 1K	The ROM area is selected after 1K
Code encryption	Encryption	Burn mode data encryption
	No encryption	Burn mode data is not encrypted
Reset port pull up	Enable	Enable P63 port pull-up
	Disable	Disallow P63 port pull-up
P63 port	GPIO	P63 serves as a general purpose I/O port
	RST	P63 serves as an external reset port
Reset time	PWRT = WDT = 4.5 ms	Reset setup time =WDT overflow time (regardless of frequency) = 4.5ms
	PWRT=WDT=18ms	Reset setup time =WDT overflow time (regardless of frequency) = 18ms
	PWRT=WDT=72ms	Reset setup time =WDT overflow time (regardless of frequency) = 72ms
	PWRT=WDT=288ms	Reset setup time =WDT overflow time (regardless of frequency) = 288ms
	PWRT = 140 us, WDT = 4.5 ms	Reset setup time =140us,WDT overflow time (regardless of frequency)
	PWRT=140us,WDT=18ms	Reset setup time =140us,WDT overflow time (regardless of frequency)
	PWRT=140us,WDT=72ms	Reset setup time =140us,WDT overflow time (regardless of frequency)
	PWRT=140us,WDT=288ms	Reset setup time =140us,WDT overflow time (regardless of frequency)
Drive enhancement	Forbidden	P5 Mouth - pull - fill drive ability enhanced forbidden
	Enable	P5 Mouth pull irrigation drive ability enhancement enable
CMP_FILT	Comparator results digital filter forbidden	When disabled, comparator results are output in real time
	Comparator result digital filtering enabled	When enabled, the comparator result is output after digital filtering

5. Instruction set

Instructions	Command action	Flag impact
ADD A,R	A+R→A	Z,C,DC
ADD R,A	A+R→R	Z,C,DC
AND A,R	A&R→A	Z
AND R,A	A&R→R	Z
CLRA	0→A	Z
CLR R	0→R	Z
INVA R	/R→A	Z
INV R	/R→R	Z
DA	A register adjusts to BCD value	C
DECA R	R-1→A	Z
DEC R	R-1→R	Z
DJA R	R-1→A, skip if zero	-
DJ R	R-1→R, skip if zero	-
INCA R	R+1→A	Z
INC R	R+1→R	Z
IJA R	R+1→A, skip if zero	-
IJ R	R+1→R, skip if zero	-
MOV R,A	A→R	-
MOV A,R	R→A	Z
MOV R,R	R→R	Z
OR A,R	A∨VR→A	Z
OR R,A	A∨VR→R	Z
SUB A,R	R-A→A	Z,C,DC
SUB R,A	R-A→R	Z,C,DC
XOR A,R	A⊕R→A	Z
XOR R,A	A⊕R→R	Z
IR R	IOCR→A	-
IW R	A→IOCR	-
CTR	CONT→A	-
CTW	A→CONT	-
BTC R,b	0→R(b)	-

BTS R,b	1→R(b)	-
JBTC R,b	if R(b)=0, skip	-
JBTS R,b	if R(b)=1, skip	-
LCR R	R(n)→R(n+1),R(7)→C, C→R(0)	C
LCA R	R(n)→A(n+1),R(7)→C, C→A(0)	C
RCR R	R(n)→R(n-1),R(0)→C, C→R(7)	C
RCA R	R(n)→A(n-1),R(0)→C, C→A(7)	C
SWAP R	R(0-3) ↔ R(4-7)	-
SWAPA R	R(0-3)→A(4-7),R(4-7)→A(0-3)	-
ADD A,k	A+k→A	Z,C,DC
AND A,k	A&k→A	Z
MOV A,k	k→A	-
OR A,k	A∨k→A	Z
SUB A,k	k-A→A	Z,C,DC
XOR A,k	A⊕k→A	Z
CALL k	PC+1→[SP], (Page,k)→PC	-
DI	Disallow interruption	-
EI	Enable Interrupt	-
JMP k	K (Page,k)→PC	-
NOP	Empty instruction	-
RET	[top of stack]→PC	-
RETI	[top of stack]→PC, enable interrupt	-
RETL k	k→A,[top of stack]→PC	-
SLEEP	0→WDT, the oscillator stops oscillating (sleep mode)	T,P
CWDT	0→WDT	T,P

6. Electrical characteristics

6.1 Limit parameters

Working temperature... -40℃ ~ 85℃
Storage temperature... -65℃ to 150℃
The input voltage... Vss-0.3V ~ Vdd+0.5V
The output voltage... Vss-0.3V ~ Vdd+0.5V
Working voltage... 1.2 V to 5.5 V

6.2 DC electrical characteristics

(VDD =5V, operating temperature =25 ° C, unless otherwise stated)

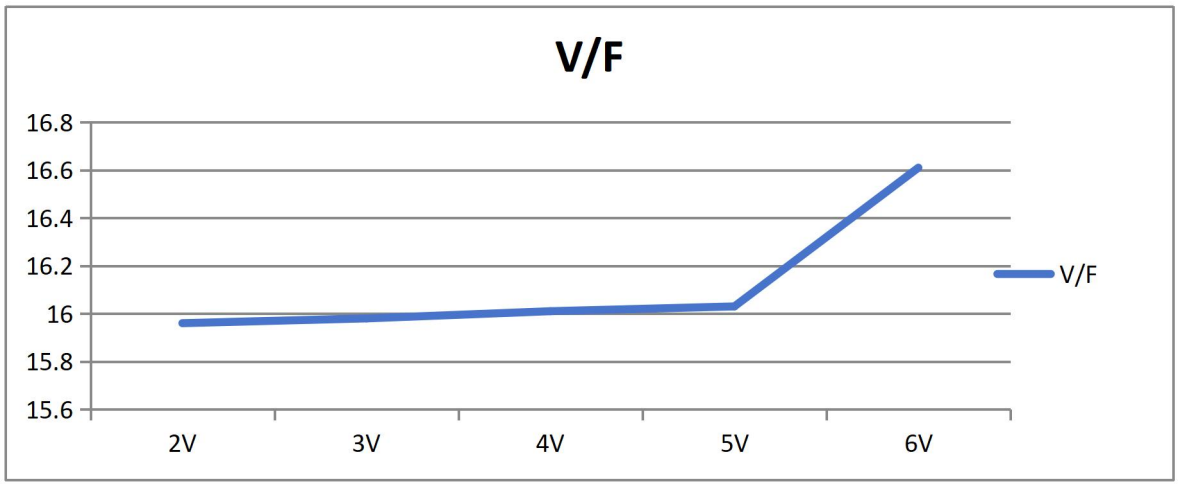
Symbols	Parameter description	Conditions	minimum	Typical	Largest	Units
IRC1	IRC1 (after correction)	OPTION select 8MHz	-	8	-	MHz
IRC2	IRC2 (after correction)	OPTION select 1MHz	-	1	-	MHz
IOH1	Output High Level driver	Ioh = 4.4 V	4	6	8	mA
IOH2	Output High level driver	Ioh = 4.4 V	15	17	19	mA
IOH3	Output High Level Drive Enhancement (P5)	Ioh = 4.4 V	15	17	19	mA
IOL1	Output Low Level driver	Iol = 0.6 V	8	10	12	mA
IOL2	Output Low Level driver	Iol = 0.6 V	20	22	24	mA
IOL3	Output Low Level Drive Enhancement (P5)	Iol = 0.6 V	20	22	24	mA
VIH1	Enter High level (P63)	-	0.5 * VDD	-	VDD	V
VIH2	Input high level (except P63)	-	0.48 * VDD	-	VDD	V
VIL1	Input low (P63)	-	GND	-	0.5 * VDD	V
VIL2	Input low (except P63)	-	GND	-	0.26 * VDD	V
RPH	Pull-up resistor	Pull up enable, input ground	53	55	57	K Ω
RPD	Pull-down resistance	Pull-down enabled, input to VDD	53	55	57	K Ω
Isb1	Power off current 1	The input is connected to VDD, the output is suspended, and the WDT is disabled	-	-	1	μA
Isb2	Power off current 2	The input is connected to VDD, the output is suspended, and WDT is enabled	-	-	12	μA
Iop2	Operating current 1	IRC=8MHz 2clock	-	1.2	1.5	mA
Iop2	Operating current 2	IRC=1MHz 2clock	-	0.2	0.3	mA
LVR	Low voltage reset voltage	Select the LVR reset point	Vlvr - 0.2	Vlvr	Vlvr + 0.2	V
Note: The above parameters are for reference only, please refer to the measured data of the target prototype.						

6.3 Characteristic curve diagram

The curves listed in this chapter are for design reference only, and part of the data given may exceed the specified working range of the chip. In order to ensure the normal operation of the chip, please strictly refer to the electrical characteristics.

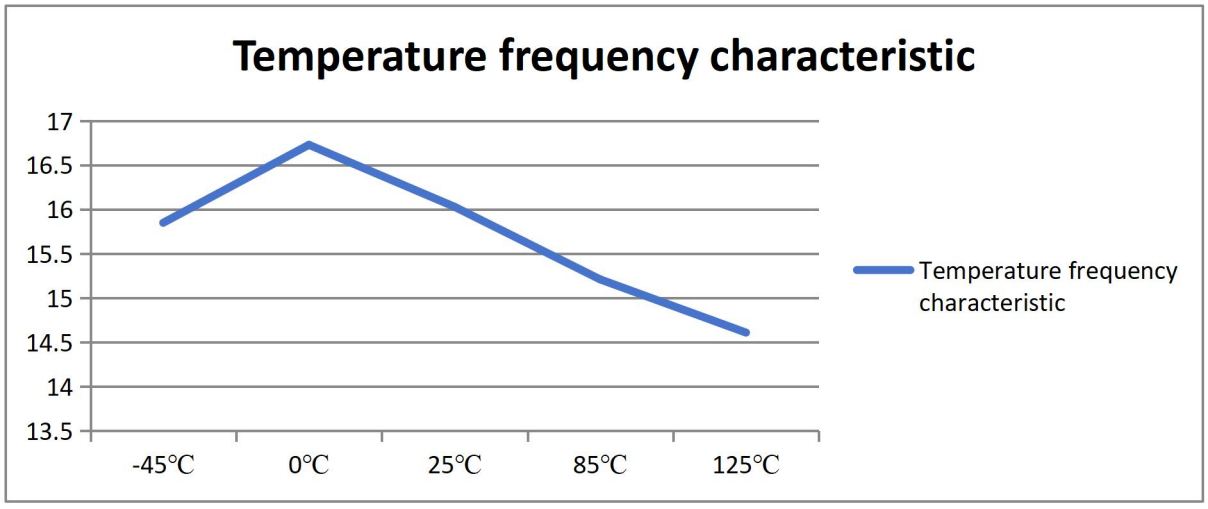
6.3.1 Internal low-speed RC Oscillator - voltage-frequency characteristic curve

Operating temperature at 25℃ : (in KHz)



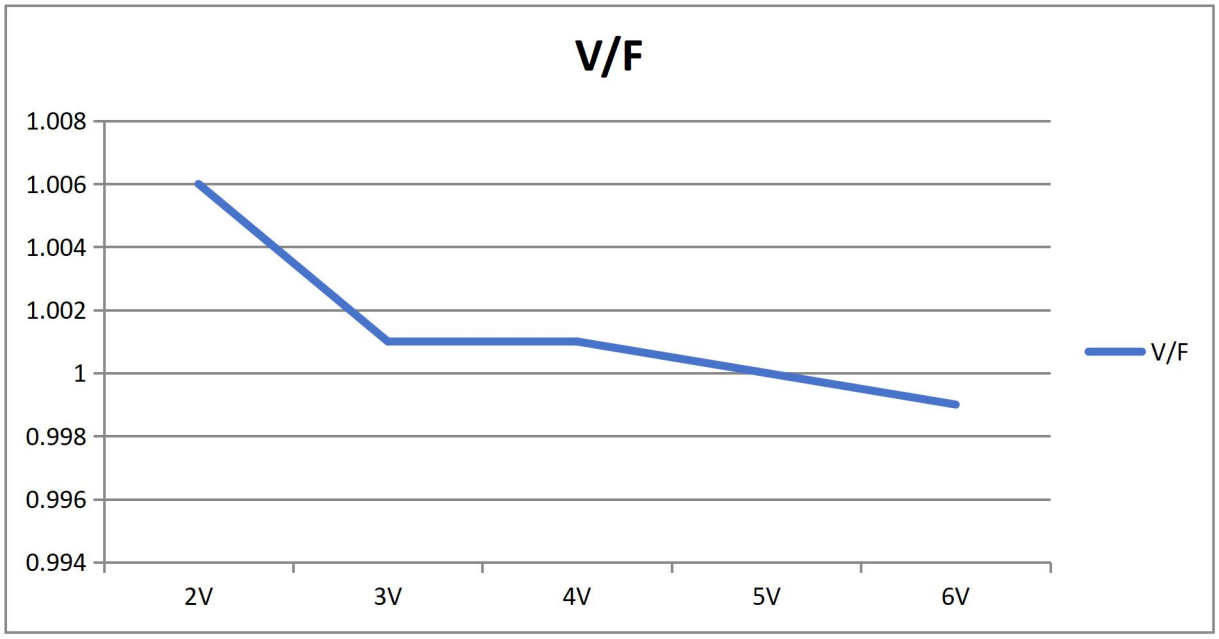
6.3.2 Internal low-speed RC oscillator - Temperature-frequency characteristic curve

Operating voltage at 5V: (in KHz)



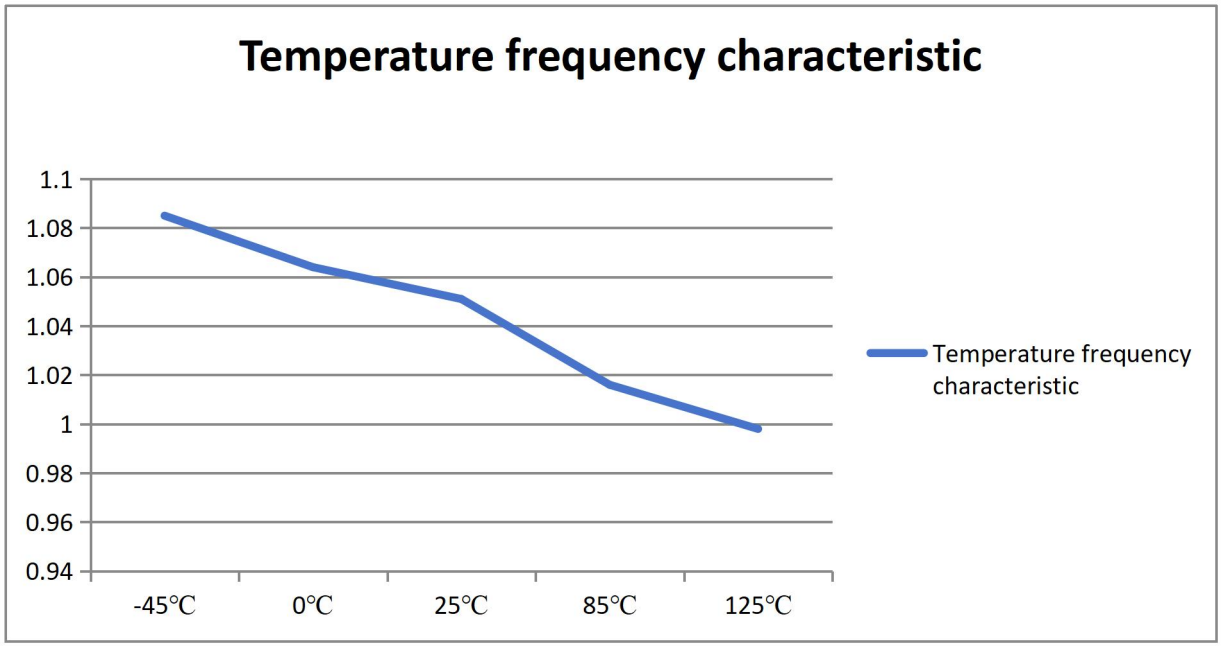
6.3.3 Internal 1MHz RC oscillator - voltage-frequency characteristic curve

Operating temperature at 25℃ : (in MHz)



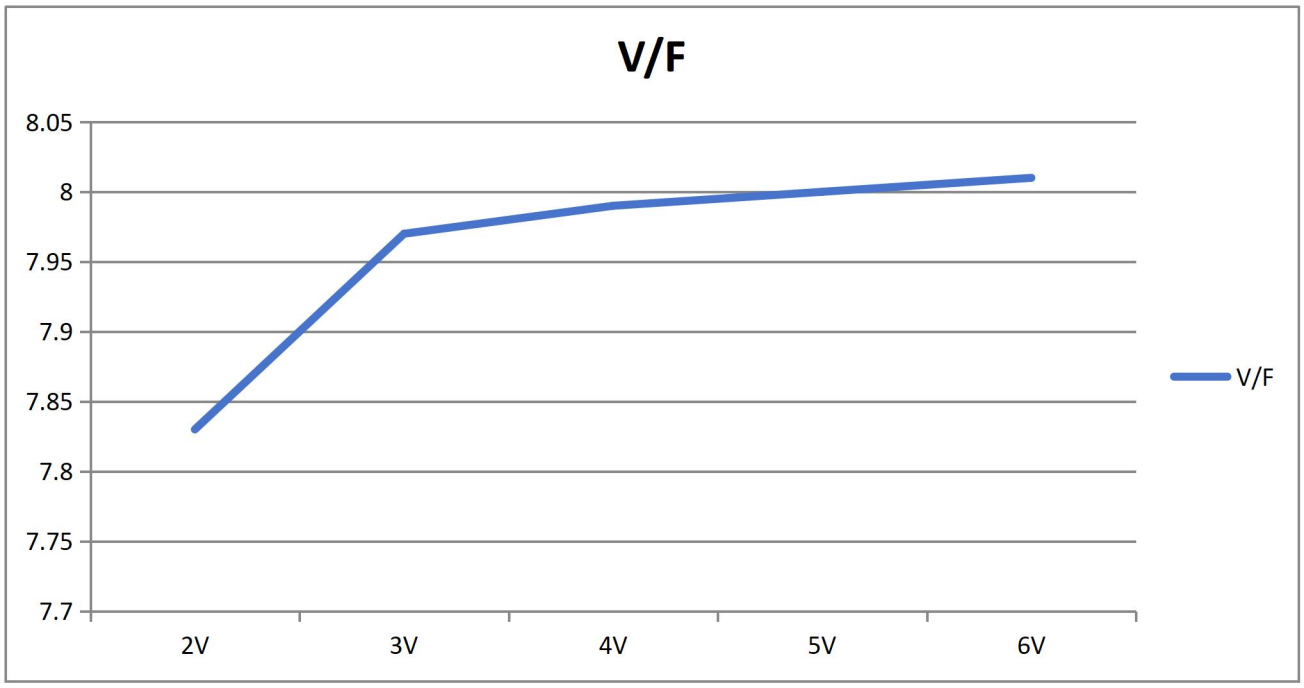
6.3.4 Internal 1MHz RC oscillator - Temperature-frequency characteristic curve

Operating voltage at 5V: (in MHz)



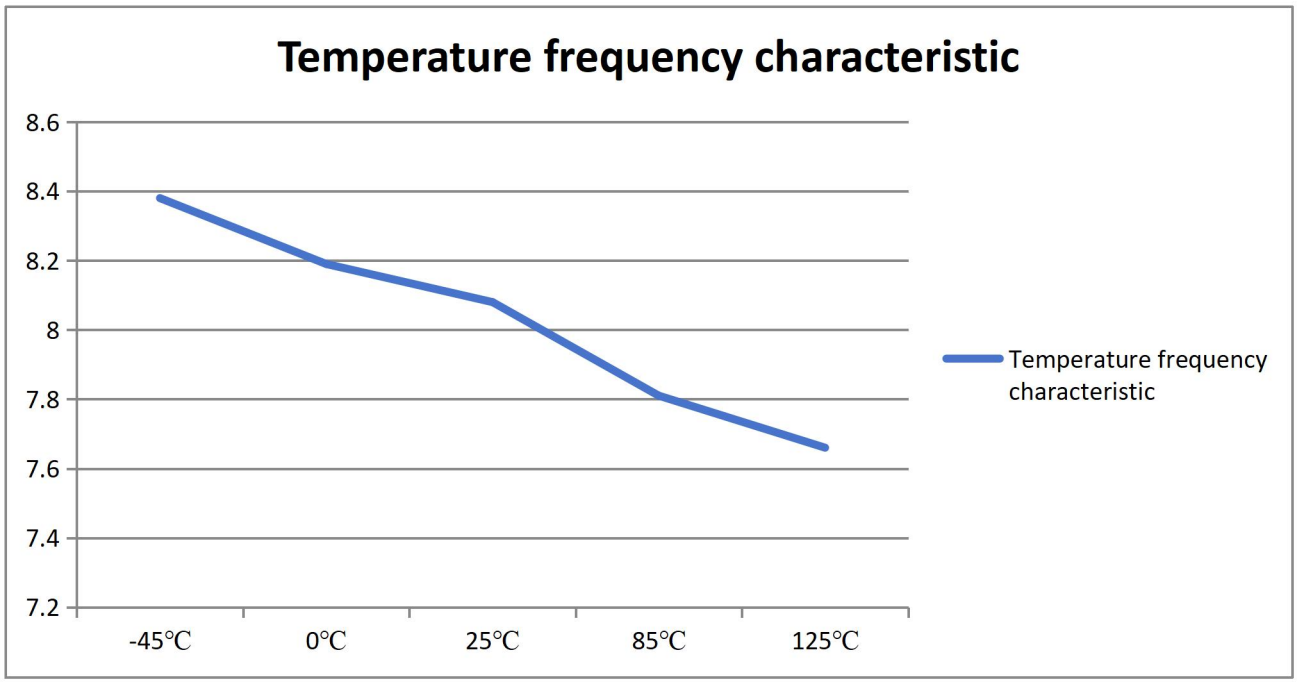
6.3.5 Internal 8MHz RC oscillator - voltage-frequency characteristic curve

Operating temperature at 25 ° C: (in MHz)



6.3.6 Internal 8MHz RC oscillator - Temperature-frequency characteristic curve

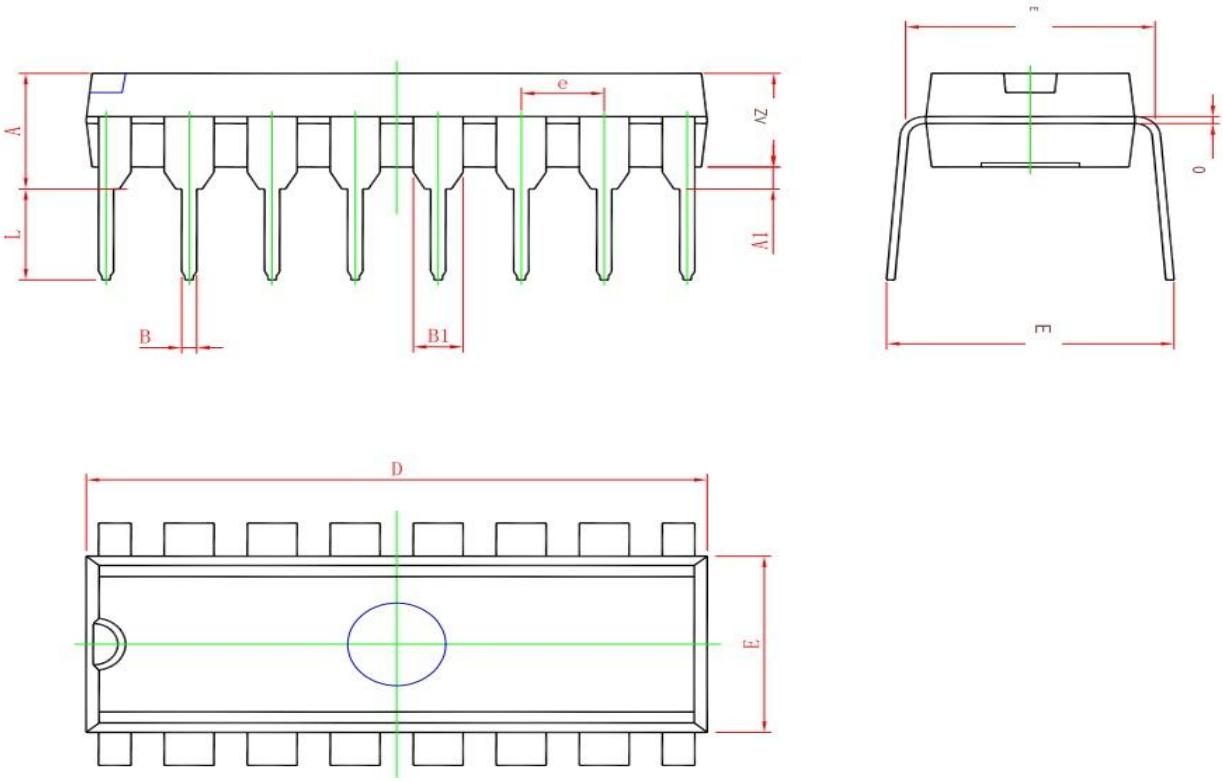
Operating voltage at 5V: (in MHz)



7 Package size

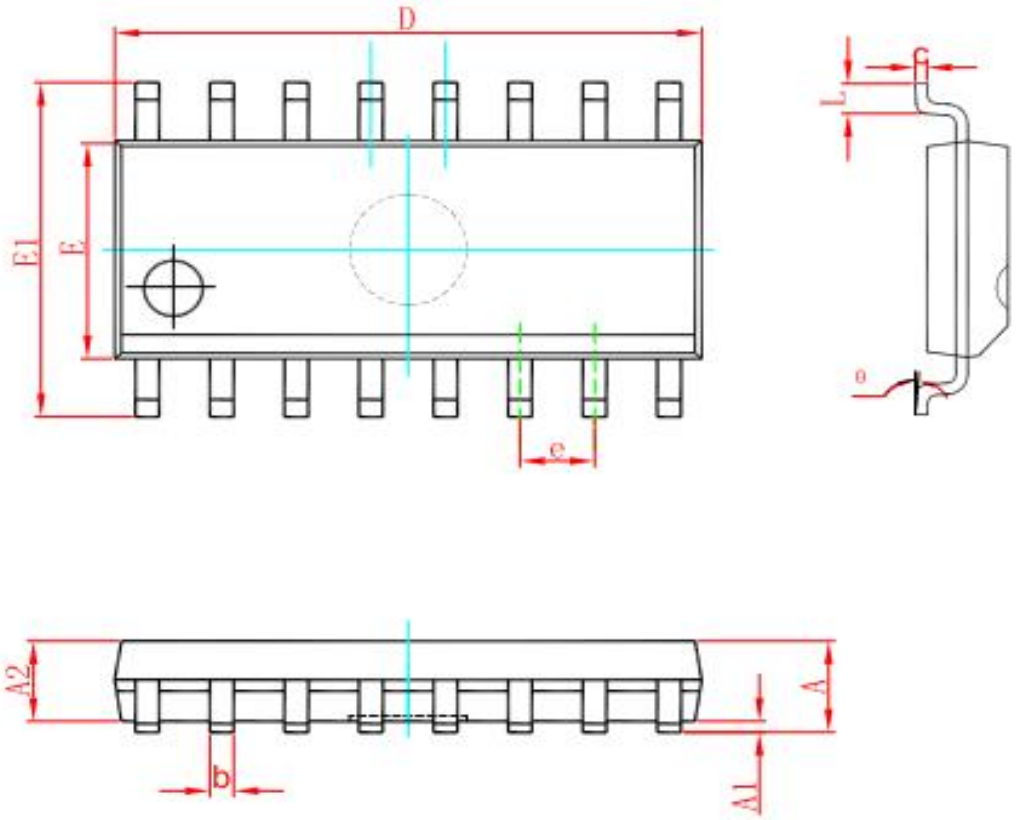
7.1 16PIN package size

DIP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.974	0.288	0.314
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

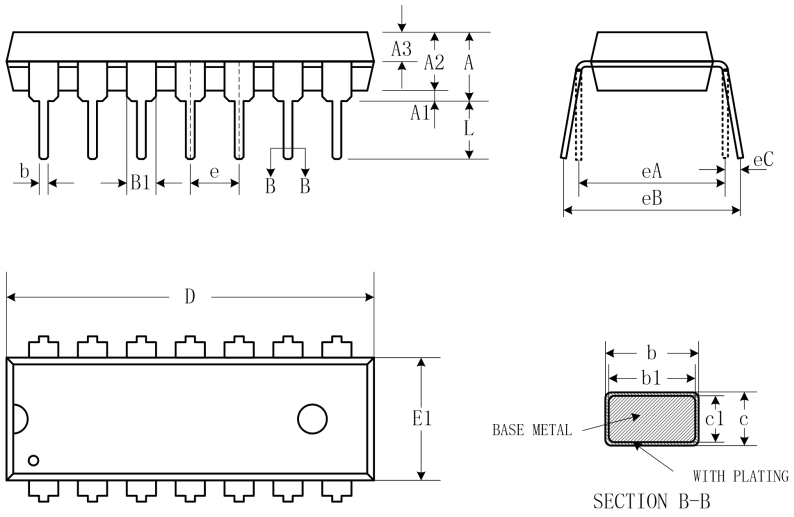
SOP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

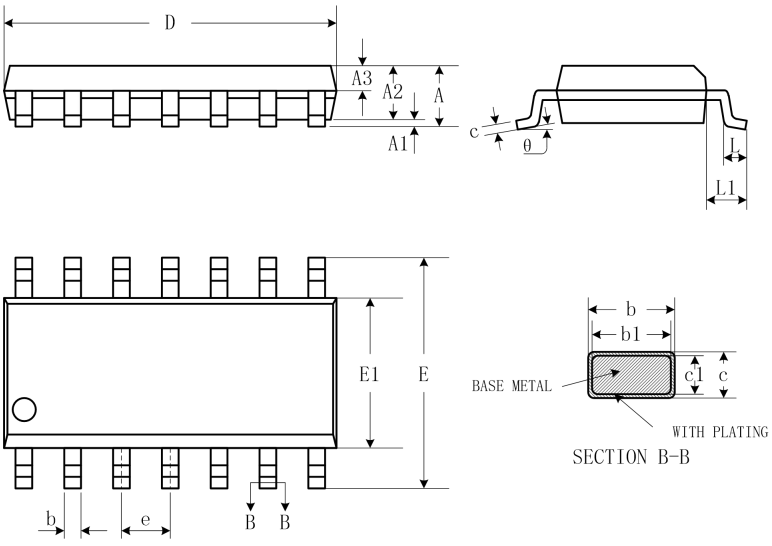
7.2 14PIN package size

DIP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	–	–
A2	3.10	3.30	3.50
A3	1.42	1.52	1.62
b	0.44	–	0.53
b1	0.43	0.46	0.48
B1	1.52 BSC		
c	0.25	–	0.31
c1	0.24	0.25	0.26
D	18.90	19.10	19.30
E1	6.15	6.35	6.55
e	2.54 BSC		
eA	7.62 BSC		
eB	7.62	–	9.50
eC	0	–	0.94
L	3.00	–	–

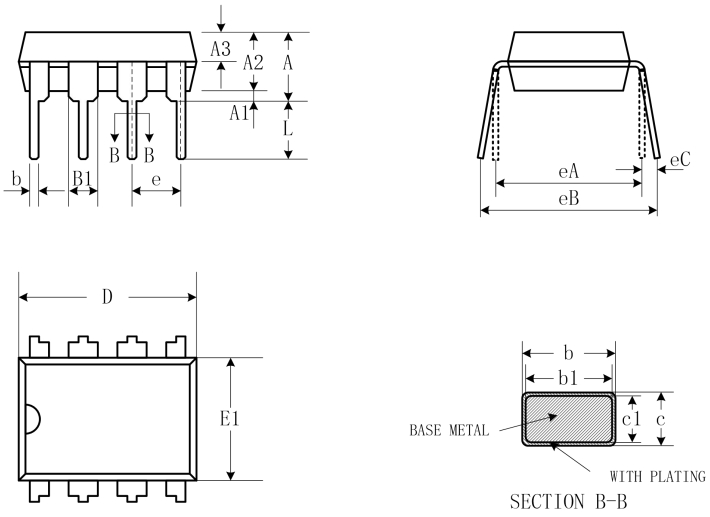
SOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	–	0.48
b1	0.38	0.41	0.43
c	0.21	–	0.26
c1	0.19	0.20	0.21
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
L	0.50	0.65	0.80
L1	1.05 BSC		
Theta.	0	–	8 °

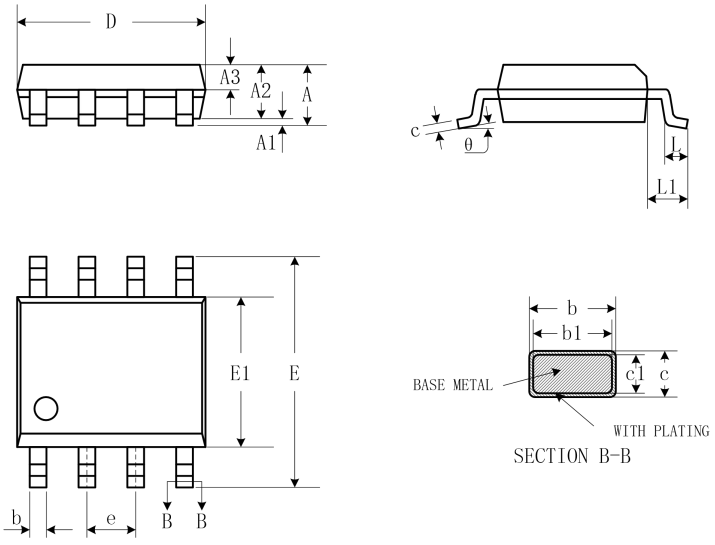
7.3 8PIN package size

DIP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	-	-
A2	3.10	3.30	3.50
A3	1.50	1.60	1.70
b	0.44	-	0.53
b1	0.43	0.46	0.48
B1	1.52 BSC		
c	0.25	-	0.31
c1	0.24	0.25	0.26
D	9.05	9.25	9.45
E1	6.15	6.35	6.55
e	2.54 BSC		
eA	7.62 BSC		
eB	7.62	-	9.50
eC	0	-	0.94
L	3.00	-	-

SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
L	0.50	0.65	0.80
L1	1.05 BSC		
Theta.	0	-	8 °