JZ8P2600C

8-BIT Microcontroller with OTP ROM

Product Specification

Version 1.1

Revision History

Version	Revision Description	Remake
V1.0	Initial version	
V1.1	Modifying the Content Format	

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1 General Description

1.1 Features

CPU configuration

- 2K×14-Bit OTP ROM
- 64×8-Bit SRAM
- 7-level stacks for subroutine nesting
- Less than 2 mA at 4MHz/5V
- Less than 30 μA at 32KHz/3V
- Less than 1 μA during Sleep mode

I/O port configuration

- 1 bidirectional I/O ports:P6
- 6 I/O pins
- Wake-up port:P6
- 6 programmable pull-high pins
- 5 programmable pull-down pins
- 6 programmable drive enhancement I/O pins
- External interrupt: P60

Operating voltage range

- Operating voltage range:
  1.8V～5.5V (0℃-70℃)
  2.3V～5.5V (-40℃-85℃)

Operating frequency range

- build-in RC oscillator:
  910KHz/8MHz
- Choice of Clock Period Frequency Division:
  2Clock,4Clock,8Clock,16Clock
  32Clock

Low voltage reset

- 1.2V±0.3V、1.6V±0.3V
- 1.8V±0.3V、2.4V±0.2V
- 2.7V±0.2V、3.3V±0.2V
- 3.6V±0.2V、3.9V±0.2V

Interrupt sources

- TCC overflow interrupt
- External interrupt
- Input-port status changed interrupt
- PWM period match interrupt
- ADC completes the transition interrupt

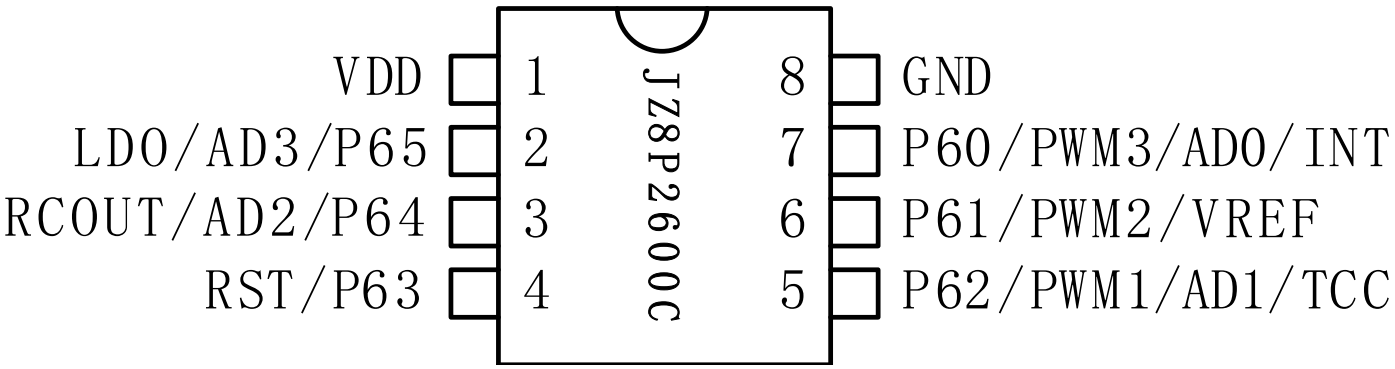
Special Features

- Programmable free running Watchdog Timer
- Four working modes switch
- External ADC reference voltage
- Reset /VPP port can output high level
- Can burn 1K twice, configuration bit can be modified
- LDO port can output the built-in reference voltage

Package Type

- JZ8P2600C-DIP8;
- JZ8P2600C-SOP8;

1.2 Pin Assignment



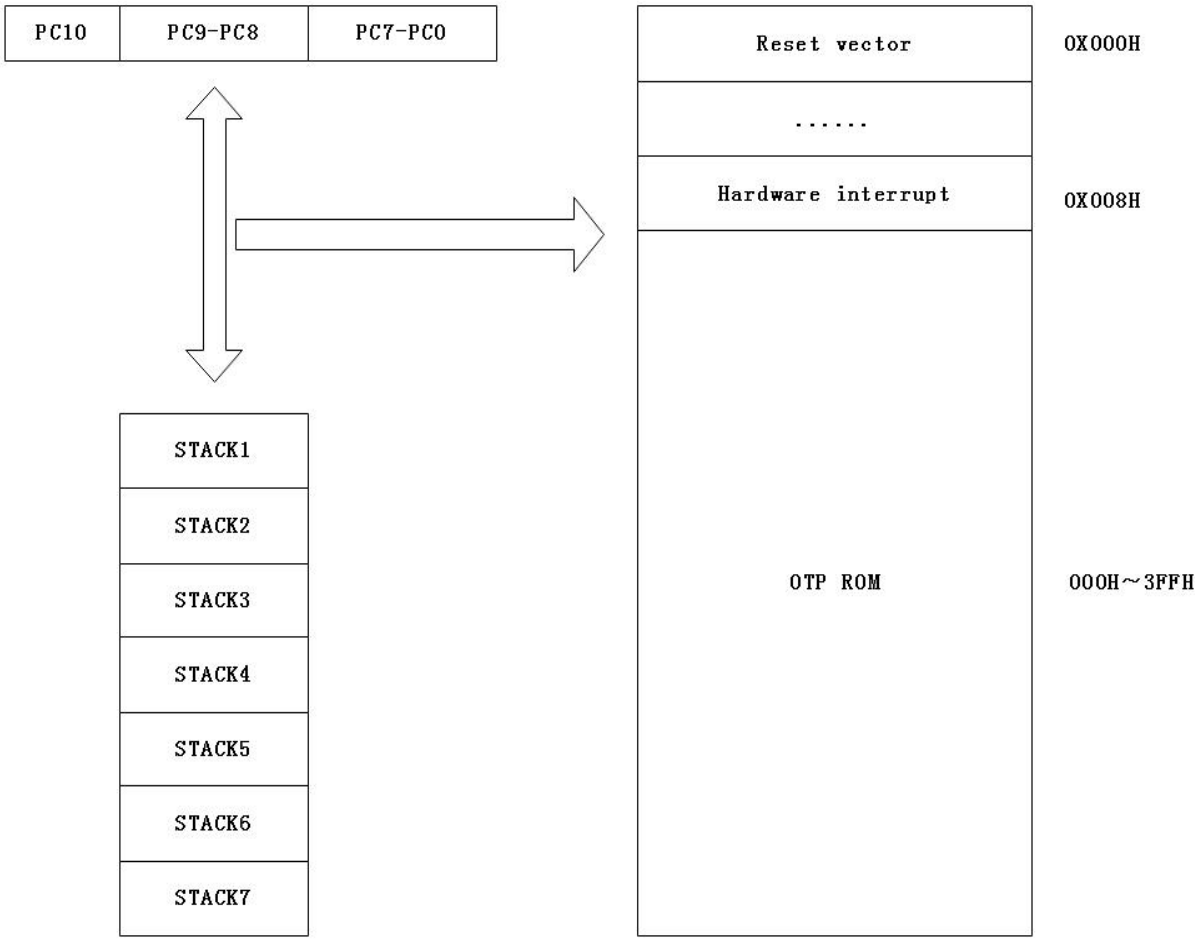
JZ8P2600C-8PIN map

1.3 Pin Description

NUM.	Name	I/O	Description
P60	P60	I/O	GPIO, programmable pull-up, pull-down, high drive, port wake-up
	INT0	I	External interrupt input port
	PWM3	O	PWM3 output
	AD0	I	ADC input channel 0
P61	P61	I/O	GPIO, programmable pull-up, pull-down, high drive, port wake-up
	PWM2	O	PWM2 output
	EXVREF	I	External reference voltage input port
P62	P62	I/O	GPIO, programmable pull-up, pull-down, high drive, port wake-up
	TCC	I	External TCC signal source input pin
	PWM1	O	PWM1 output
	AD1	I	ADC input channel 1
P63	P63	I/O	GPI, programmable pull-up, pull-down, high drive, port wake-up
	RST	I	Reset pin
P64	P64	I/O	GPIO, programmable pull-up, pull-down, high drive, port wake-up
	RCOUT	O	Internal system clock output
	AD2	AN	ADC input channel 2
P65	P65	I/O	GPIO, programmable pull-up, pull-down, high drive, port wake-up
	VFOUT	O	Built-in reference voltage can be output
	AD3	AN	ADC input channel 3
	VDD	--	VDD
	VSS	--	GND

2 Memory structure

2.1 Program memory area



Program memory area structure

2.2 Data memory area

2.2.1 RPAGE\IOPAGE\Bank Data register area

Address	RPAGE Page register	IOPAGE Page register
0x00	R0/IAR Indirect Addressing Register	Reserved
0x01	R1/TCC Timer Clock Counter	CONT Control Register
0x02	R2/PC Program Counter	Reserved
0x03	R3/STATUS Status Register	Reserved
0x04	R4/RSR RAM Select Register	Reserved
0x05	Reserved	Reserved
0x06	R6/PORT6 P6 Data Register	IOC6/P6CR P6 Direction Control Register
0x07	R7/ADCON ADC control register	IOC7/ADCVS AD channel, voltage, frequency division selection
0x08	R8/PWMCON PWM Control Register	IOC8/ADATH AD converts the high 8 bits of the value
0x09	R9/PRD PWM Cycle Register	IOC9/PHDCR Port Pull-up Or Pull-down Control Register
0x0A	RA/PDC1 PWM1Duty Register	IOCA/ADPS AD sampling port enable and AD high 4 bit register
0x0B	RB/PDC2 PWM2 Duty Register	IOCB/PDCR Port Pull-down Control Register
0x0C	RC PDC3 PWM3 Duty Register	IOCC/ADATL AD converts the low 8 bits of the value
0x0D	RD/ICIECR P6 Port Interrupt Wake-up Enable Register	IOCD/PHCR Port6 Pull-up Control Register
0x0E	RE/CPUCON CPU Mode Controls Registers	IOCE/WDTCR WDT Enable Control Register
0x0F	RF/ISR Interrupt Flag Register	IOCF/IMR Interrupt Enable Control Register
0x10-0x4F	General register	

3 Functional Description

3.1 Operational Registers

3.1.1 RPAGE～R0/IAR(Indirect Address Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RIND<7:0>							

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the low 6-bit RAMS<5:0> of RAM Select Register (R4).

3.1.2 RPAGE～R1/TCC(TCC Time Clock/Counter)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC<7:0>							

TCC is an 8Bit Count-Up counter. An internal clock/external clock can be selected as the clock source. Count overflow can form an interrupt, and TCC can be read and written.

3.1.3 RPAGE～R2/PCL(PC Program Counter)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCL<7:0>							

The program counter (PC) is a pointer for recording instructions to be processed by the CPU in each instruction cycle. During the CPU run cycle, the PC advances the instruction pointer to the program memory and then increments the pointer by one to advance to the next cycle.

3.1.4 RPAGE～R3/STATUS(STATUS Status Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	GB1	GB0	T	P	Z	DC	C

Bit<7>: RST: Bit of reset type:

0: if wake-up from other reset types.

1: if wake-up from sleep on pin change.

Bit<6:5>:GB1-GB0: Universal read-Write bit

Bit<4>:T- Time-out bit

0: WDT time-out

1: execute the "SLEP" and "WDTC" commands or during Low voltage reset

The events affecting T/P are shown in the following table:

Type	RST	T	P
Power on	0	1	1
/RESET during Operating mode	0	Hold	Hold
/RESET wake-up during Sleep mode	0	1	0
WDT time-out in working mode	0	0	Hold
Wakes up for WDT time-out	0	0	0

Wake-up on pin change during Sleep mode	1	1	0
WDTC instruction	Hold	1	1
SLEEP instruction	Hold	1	0

Bit<3>: P: Power-down bit:
0: execute "SLEP" command.
1: during power-on or by a "WDTC" command.
Bit<2>: Z: Zero flag:
0: if the result of an arithmetic or logic operation is zero.
1: if the result of an arithmetic or logic operation is not zero.
Bit<1>: DC: Auxiliary carry flag:
0: When the addition operation is performed, the lower four bits do not generate a carry or when the subtraction operation is performed, the lower four bits do not generate a borrow.
1: When the addition operation is performed, the lower four bits do not generate a carry or when the subtraction operation is performed, the lower four bits do not generate a borrow.
Bit<0>: C: Carry flag:
0: When the addition operation is performed, the upper four bits do not generate a carry or when the subtraction operation is performed, the upper four bits do not generate a borrow.
1: When the addition operation is performed, the upper four bits do not generate a carry or when the subtraction operation is performed, the upper four bits do not generate a borrow.

3.1.5 RPAGE～R4/RSR(FSR RAM Select Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	FSR<6:0>						

FSR<6:0> Used to select a register (Address: 0X00~0X4F) in indirect addressing mode. The user can place the address corresponding to a register into the FSR. And then through accessing indirect addressing Register R0, the address will point to the register of the corresponding address in the FSR.

3.1.6 RPAGE～R6/PORT6(PORT6 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P65	P64	P63	P62	P61	P60

Port input/output register, P6 port is 6 bits, R6 is a readable and writable register

3.1.7 RPAGE～R7/ADCON(ADC Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADRUN	ADPD	VREFS	CALI	SIGN	VOF<2>	VOF<1>	VOF<0>

Bit<7>:ADRUN
1: ADC starts sampling
0: ADC no sampling or sampling ended
Bit<6>:ADPD
1:ADC Enable

0:ADC Disable（Turn off ADC in sleep mode, otherwise there will be power consumption）

Bit<5>:VREFS

1: ADC uses external reference voltage (P61 port)

0: ADC uses internal reference voltage

Bit<4>:CALI

1: ADC zero drift calibration enables

0: ADC zero drift calibration disables

Bit<3>:SIGN

1: ADC zero drift calibrates positive polarity

0: ADC zero drift calibrates negative polarity

Bit<2:0>:VOF<2:0> ADC zero drift calibration bits

VOF<2>	VOF<1>	VOF<0>	The calibration range
0	0	0	0 LSB
0	0	0	2 LSB
0	0	1	4 LSB
0	1	0	6 LSB
0	1	1	8 LSB
1	0	0	10 LSB
1	0	1	12 LSB
1	1	0	14 LSB

3.1.8 RPAGE～R8/PWMCON(PWM Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1EN	PWM3EN	PWM2EN	PWM1EN	T1PTEN	T1P<2:0>		

Bit<7>:T1EN-T1/PWM counter enable

1: Enable

0: Disable

Bit<6>:PWM3EN-PWM3 output enables control bits

1: Enable（P60 output PWM3）

0: Disable

Bit<5>:PWM2EN-PWM2 output enables control bits

1: Enable（P61 output PWM2）

0: Disable

Bit<4>:PWM1EN-PWM1 output enables control bits

1: Enable（P62 output PWM1）

0: Disable

Bit<3:0>:T1PTEN PT1P<2:0>-T1 frequency division selects the control bit

T1PTEN	PT1P<2>	PT1P<1>	PT1P<0>	T1 Frequency division ratio
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8

1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.9 RPAGE～R9/PRD(PWM Cycle Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD<7:0>							

T1/PWM Cycle Register

3.1.10 RPAGE～RA/PDC1(PWM1 Duty Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC1<7:0>							

Bit<7:0>:PDC1<7:0>-PWM1 Duty Register

3.1.11 RPAGE～RB/PDC2(PWM2 Duty Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC2<7:0>							

Bit<7:0>:PDC2<7:0>-PWM2 Duty Register

3.1.12 RPAGE～RC/PDC3(PWM3 Duty Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC3<7:0>							

Bit<7:0>:PDC3<7:0>-PWM3 Duty Register

3.1.13 RPAGE～RD/ICIECR(P6 Port Interrupt Wake-up Enable Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	P6WK<5>	P6WK<4>	P6WK<3>	P6WK<2>	P6WK<1>	P6WK<0>

Bit<5:0>:P6WK<5:0>-P6 Port Interrupt Wake-up Enable

1: Enable

0: Disable(default)

Note: In OPTION for port wake-up setting, if P6 port is not independently controlled, port wake-up is not controlled by RD register; otherwise, the RD register needs to be processed, or the port cannot be woken up.

3.1.14 RPAGE～RE/CPUCON(CPU Mode Controls Registers)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPWM1	PWMCKS	TCCCKS	PWMWE	TCCWE	STPHX	CLKMD	IDLE

Bit<7>:IPWM1-PWMcomplementary output

1:PWM1 reverse phase output

0:PWM1 normal output

Bit<6>:PWMCKS-PWM clock source

1: Select system clock

0: Select the instruction cycle clock

Bit<5>:TCCCKS-TCC clock source
1: Select system clock
0: Select the instruction cycle clock
Bit<4>:PWMWE-PWM wake up
1:PWM wake up enable, can wake up IDLE mode
0:PWM wake up disable
Bit<3>:TCCWE-TCC wake up
1:TCC wake up enable, can wake up IDLE mode , RTC mode can wake up SLEEP and IDLE mode
0:TCC wake up disable
（Set TCCWE=1&RTCS=1 in RTC mode and LXT will continue to work when in SLEEP mode, otherwise LXT will stop when in SLEEP mode）
Bit<2>:STPHX- High-speed clock
1: Stop high speed clock, including IRC and crystal oscillator clock (excluding RTC clock)
0: The high speed clock is working properly
Bit<1>:CLKMD- System clock
1: The system clock uses a low speed RC oscillator clock
0: The system clock uses a high speed IRC or crystal oscillator clock
（When the system enters low speed mode from normal mode, set CLKMD=1 first, then set STPHX=1;When the system enters normal mode from low speed mode, STPHX=0 is set first, and CLKMD=0 is set later）
Bit<0>:IDLE-IDLE mode
1: When the system executes SLEEP instruction, it enters idle mode, and the system clock works normally
（TCC and PWM in idle mode, select the system clock can continue to work, and can wake up the system）
0: The system goes into SLEEP mode when it executes the SLEEP instruction

3.1.15 RPAGE～RF/ISR(Interrupt Flag Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	ADIF	T1IF	EXIF	ICIF	TCIF

Bit<4>:ADIF- ADC conversion completes the interrupt flag bit, software clear 0
Bit<3>:T1IF-T1/PWM cycle interrupt flag bit, software clear 0
Bit<2>:EXIF-External interrupt flag bit (set 1 by drop edge of EXINT pin, software clear 0)
Bit<1>:ICIF-P6 Port state change interrupt flag bit, software clear 0
Bit<0>:TCIF-TCC interrupt flag bit, software clear 0
1: interrupt request
0: no interrupt occurs
Note: "MOV RF, A" should be used to clear the interrupt flag. BTC/AND RF, A instructions should not be used.

3.2 Control Register

3.2.1 CONT (Control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit<6>:INT- Interrupt enable flag
0: Disable interrupts by instruction or hardware
1: Enable interrupts by instruction
Bit<5>:TS-TCC signal source selection bit
0: Internal instruction cycle clock
1: External input signal (P62 needs to be set as input)
Bit<4>:TE-TCC signal edge selection bit
0: TCC pin signal changes from low to high plus 1
1: TCC pin signal changes from high to low plus 1
Bit<3>:PAB- Prescaler allocation bit
0: Prescaler is assigned to TCC
1: Prescaler is assigned to WDT
Bit<2:0>PSR2～PSR0: TCC/WDT Prescaler selection control bit:

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

CONT is a readable and writable register

3.2.2 IOPAGE～IOC6/P6CR(P6 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6CR<5>	P6CR<4>	P6CR<3>	P6CR<2>	P6CR<1>	P6CR<0>

Port6 direction control bit
1: input (default)
0: output

3.2.3 IOPAGE～IOC7/ADCVS(AD channel/voltage/frequency division selection register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCKS<1>	ADCKS<0>	ADICS<2>	ADICS<1>	ADICS<0>	VREF<2>	VREF<1>	VREF<0>

Bit<7:6>:ADCKS<1:0>

CLKMD	ADCKS<1>	ADCKS<0>	ADC clocks
0	0	0	Fosc/16
0	0	1	Fosc/4

0	1	0	Fosc/64
0	1	1	Fosc/1
1	X	X	Fosc/1

Bit<5:3>:ADICS<2:0>

ADICS<2>	ADICS<1>	ADICS<0>	ADC channel selection
0	0	0	AD0（P60）
0	0	1	AD1（P62）
0	1	0	AD2（P64）
0	1	1	AD3（P65）
1	0	0	AD4（Internal reference）

AD value is calculated as follows: AD value = (reference voltage /VDD) *4096

Bit<2:0>:VREF<2:0>

VREF<2>	VREF<1>	VREF<0>	Internal reference voltage
0	0	0	VDD
0	0	1	4V
0	1	0	3V
0	1	1	2V
1	0	0	1.5V

3.2.4 IOPAGE～IOC8/ADATH(AD converts the high 8 bits of the value)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADAT<11>	ADAT<10>	ADAT<9>	ADAT<8>	ADAT<7>	ADAT<6>	ADAT<5>	ADAT<4>

Save the high 8 bits of the AD conversion result.

3.2.5 IOPAGE～IOC9/PHDCR(Port Pull-up Or Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6PD<5>	P6PD<4>	-	-	-	-

Bit<5:4>:P6<5:4> Pull-down enable control

0: Enable

1: Disable (default)

Note: When setting option in burn mode, it is necessary to enable P5, P6 pull up and down; otherwise, all of them are read as 1.

3.2.6 IOPAGE～IOCA/ADPS(AD sampling port enable and AD high 4 bit register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADEN<3>	ADEN<2>	ADEN<1>	ADEN<0>	ADAT<11>	ADAT<10>	ADAT<9>	ADAT<8>

Bit<7>:ADEN<3>

1: AD3 port as analog input port

0: AD3 port as GPIO

Bit<6>:ADEN<2>

1: AD2 port as analog input port
0: AD2 port as GPIO

Bit<5>:ADEN<1>
1: AD1 port as analog input port
0: AD1 port as GPIO

Bit<4>:ADEN<0>
1: AD0 port as analog input port
0: AD0 port as GPIO

Bit<3:0> ADAT<11:8> read-only

Note: Being an analog input port will disable other IO port functions including input, output, pull-up, pull-down, and other reuse functions

3.2.7 IOPAGE～IOCB/PDCR(Port Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	P6PD<2>	P6PD<1>	P6PD<0>	-	-	-	-

Bit7: undefined

Bit<6:4>:P6<2:0> Pull-down enable control
0: Enable
1: Disable (default)

Bit<3:0>: undefined

3.2.8 IOPAGE～IOCC/ADATL(AD converts the low 8 bits of the value)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADAT<7>	ADAT<6>	ADAT<5>	ADAT<4>	ADAT<3>	ADAT<2>	ADAT<1>	ADAT<0>

Save the low 8 bits of the AD conversion result.

3.2.9 IOPAGE～IOCD/PHCR(Port6 Pull-up Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>

P6 port pull-up control
0: Enable
1: Disable (default)

Note: The P6PH<3> software pull-up function is valid only when the function enhancement and wake-up independent control are all enabled in OPTION.

3.2.10 IOPAGE～IOCE/WDTCR(WDT Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTEN	EIS	ADWE	VFOE	1	1	1	1

Bit<7>:WDTEN-WDT enable control
0: Disable (default)
1: Enable

Bit<6>:EIS-P60 external interrupt enable bit
0: Disable, P60 is GPIO.
1: Enable, The I/O control bit for P60 must be set as input.

Bit<5>:ADWE-ADC wake-up control

0: Disable (default)
1: Enable

Bit<4>:VFOE-Internal reference voltage output
0: Internal reference voltage output is prohibited, P65 as GPIO (default)
1: The internal reference voltage output is enabled, with P65 as the analog port, and the output voltage is based on VREF<2: 0> choose.

3.2.11 IOPAGF～IOCF/IMR(Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	ADIE	T1IE	EXIE	ICIE	TCIE

Bit<4>:ADIE-AD interrupt enable control
1: Enable
0: Disable (default)
Bit<3>:T1IE-T1 interrupt enable control
1: Enable
0: Disable (default)
Bit<2>:EXIE- External interrupt enable control
1: Enable
0: Disable (default)
Bit<1>:ICIE- P6 port status change interrupt enable control
1: Enable
0: Disable (default)
Bit<0>:TCIE- TCC overflow interrupt enable control
1: Enable
0: Disable (default)

3.3 GPIO Function Module

JZ8P2600C has a set of bidirectional I/O ports, a total of 6 inputs and 6 outputs, most of which can be reused for other functions.

6 programmable pull-high I/O pins: P6.0～P6.5;

5 programmable pull-down I/O pins: P6.0～P6.2,P6.4～P6.5;

6 programmable driver enhanced I/O pins: P6.0～P6.5; （Port driven enhancements need to be set in OPTION）

The port input characteristics table is as follows:

Pins	SMT	HSMT	EMT	INV
P6.3	0.56*VDD	0.15*VDD/0.8*VDD	0.2*VDD/0.35*VDD	0.54*VDD
P6.0～P6.2	0.2*VDD/0.6*VDD	0.2*VDD/0.8*VDD	0.2*VDD/0.35*VDD	0.54*VDD
P6.4～P6.5	0.2*VDD/0.6*VDD	0.2*VDD/0.8*VDD	0.36*VDD	0.54*VDD

The above data are for reference , please refer to the actual prototype test.

3.3.1 GPIO Register Description

RPAGE～R6/PORT6(PORT6 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P65	P64	P63	P62	P61	P60

Port input/output register, 6 bits.

R6 is a readable and writable register.

IOPAGE～IOC6/P6CR(P6 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6CR<5>	P6CR<4>	P6CR<3>	P6CR<2>	P6CR<1>	P6CR<0>

Port6 direction control bit

1: input (default)

0: output

IOPAGE～IOC9/PHDCR(Port Pull-up Or Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6PD<5>	P6PD<4>	-	-	-	-

Bit<5:4>:P6<5:4> Pull-down enable control

0: Enable

1: Disable (default)

IOPAGE～IOCB/PDCR(Port Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	P6PD<2>	P6PD<1>	P6PD<0>	-	-	-	-

Bit7: undefined

Bit<6:4>:P6<2:0> Pull-down enable control

0: Enable

1: Disable (default)

Bit<3:0>: undefined

IOPAGE～IOCD/PHCR(Port6 Pull-up Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>

P6 port pull-up control

0: Enable

1: Disable (default)

Note: The P6PH<3> software pull-up function is valid only when the function enhancement and wake-up independent control are all enabled in OPTION.

3.4 TCC Timer Function Module

There is an 8-bit counter available as prescalers for the TCC and WDT respectively. Clock source can be either internal system clock (rising edge triggering), or external clock (input by TCC pin, triggering edge optional). If there is no frequency division control, each clock (Fm/Fs) cycle (select internal clock) or each external clock cycle (external clock) can be added to the counter by 1.

The system provides an 8-Bit counter as the prescaler of TCC. TCC prescaler, trigger edge and clock can be set by CONT register.

Note: "MOV RF, A" should be used to clear the interrupt flag. BTC/AND RF, A instructions should not be used.

3.4.1 TCC Timer Register Description

CONT (Control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit<7>: undefined

Bit<6>:INT- Interrupt enable flag

0: Disable interrupts by instruction or hardware

1: Enable interrupts by instruction

Bit<5>:TS-TCC signal source selection bit

0: Internal instruction cycle clock

1: External input signal (P62 needs to be set as input)

Bit<4>:TE-TCC signal edge selection bit

0: TCC pin signal changes from low to high plus 1

1: TCC pin signal changes from high to low plus 1

Bit<3>:PAB- Prescaler allocation bit

0: Prescaler is assigned to TCC

1: Prescaler is assigned to WDT

Bit<2:0>PSR2～PSR0: TCC/WDT Prescaler selection control bit:

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

RPAGE～R1/TCC(TCC Time Clock/Counter)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC<7:0>							

TCC is an 8Bit Count-Up counter. An internal clock/external clock can be selected as the clock source. Count overflow can form an interrupt, and TCC can be read and written.

RPAGE～RE/CPUCON(CPU Mode Controls Registers)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPWM1	PWMCKS	TCCCKS	PWMWE	TCCWE	STPHX	CLKMD	IDLE

Bit<5>:TCCCKS-TCC clock source

1: Select system clock

0: Select the instruction cycle clock

Bit<3>:TCCWE-TCC wake up

1:TCC wake up enable, can wake up IDLE mode , RTC mode can wake up SLEEP and IDLE mode

0:TCC wake up disable

（Set TCCWE=1&RTCS=1 in RTC mode and LXT will continue to work when in SLEEP mode, otherwise LXT will stop when in SLEEP mode）

Bit<2>:STPHX- High-speed clock

1: Stop high speed clock, including IRC and crystal oscillator clock (excluding RTC clock)

0: The high speed clock is working properly

Bit<1>:CLKMD- System clock

1: The system clock uses a low speed RC oscillator clock

0: The system clock uses a high speed IRC or crystal oscillator clock

（When the system enters low speed mode from normal mode, set CLKMD=1 first, then set STPHX=1;When the system enters normal mode from low speed mode, STPHX=0 is set first, and CLKMD=0 is set later）

Bit<0>:IDLE-IDLE mode

1: When the system executes SLEEP instruction, it enters idle mode, and the system clock works normally

（TCC and PWM in idle mode, select the system clock can continue to work, and can wake up the system）

0: The system goes into SLEEP mode when it executes the SLEEP instruction

RPAGE～RF/ISR(Interrupt Flag Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	ADIF	T1IF	EXIF	ICIF	TCIF

Bit<0>:TCIF-TCC interrupt flag bit, software clear 0

1: interrupt request

0: no interrupt occurs

Note: "MOV RF, A" should be used to clear the interrupt flag. "BTC/AND RF, A" instructions should not be used.

IOPAGF～IOCF/IMR(Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	ADIE	T1IE	EXIE	ICIE	TCIE

Bit<0>:TCIE- TCC overflow interrupt enable control

1: Enable
0: Disable (default)

3.4.2 TCC Timing Setup Instructions

- Assign initial values to TCC registers.
- Set the value of the CONT register (select as a timer or counter and pre-divider ratio).
- As a counter, it is necessary to select positive or negative edge plus 1 for TCC external irrigation signal in CONT register.
- If interrupt function is needed, TCIE (Bit0) in IOCF register should be set to 1, and ENI instruction should be executed.
- The interrupt program will manually save ACC, STATUS and R4 in the stack. After executing RETI instructions, the interrupt program will be poped from the stack. Before exiting the interrupt, the TCC interrupt flag should be clear.

3.5 WDT Watchdog Function Module

WDT is a 12-Bit count-up counter with two enabling control signals (WDTEN in OPTION and WDTEN control bit in IOCE register). The counting clock is provided by a separate oscillator, so the WDT can still run (if enabled) after the system enters the sleep mode. In normal mode or sleep mode, the overflow of WDT can reset the system, and the reset time is selected by the control bit WDTPS in OPTION for 4.5ms、18ms、72ms or 288ms.

The system provides an 8-Bit counter as a prescaler for WDT, which is set by CONT registers.

Whether in simulation or in burning, in order to enable WDT function, it is necessary to select Enable at the WDT bit of Code Option register, and then select "1" at the WDTE bit of WDT control register. Two conditions are indispensable. The counting frequency of watchdog timer (WDT) comes from the internal RC oscillator. The counting frequency is about 15 kHz (+30%). When MCU enters Sleep mode, because the power supply to RC oscillator is not turned off, WDT is still counting. When WDT overflows, MCU will be awakened and reset.

3.5.1 WDT Watchdog Register Description

IOPAGE～IOCE/WDTCR(WDT Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTEN	EIS	ADWE	VFOE	1	1	1	1

Bit7:WDTEN-WDT enable control

1: Enable

0: Disable (default)

3.5.2 WDT Watchdog Setting Instructions

1. Set Bit7 (WDTEN) bit in IOCE register and choose whether to use WDT or not.
2. Setting prescaler rate by setting Bit2-Bit0 bits of CONT register;
3. If WDT wake-up is enabled, it is recommended that customers prohibit other wake-up. Reasons: WDT wake-up and other wake-up enablers, when the application of WDT function wakes up at the same time, IC will give priority to reset, not to implement other wake-up procedures, so if enabling WDT wake-up, it is recommended that customers prohibit other wake-up.

3.6 Port State Change Wake-up Function Module

3.6.1 Description of sleep wake-up mode

The chip executes the "SLEEP" instruction to go to sleep mode (low power mode). When entering sleep mode, the system clock stops, all modules stop working, and the WDT (if enabled) is cleared to 0, but continues to run.

The microcontroller can be awakened as follows:

1、WDT reset wakes up;

2、TCC wake up;

3、The port status changes wake up;

The latter two methods maintain the continuity of the program, and can continue the original process (DISI before SLEEP) or perform the corresponding jump (ENI before SLEEP), and open the corresponding enabling control bit, jump to the position of the interrupt vector. Mainly describes the port change wake-up, other wake-up methods will be explained in the corresponding module.

Note: "MOV RF, A" should be used to clear the interrupt flag. BTC/AND RF, A instructions should not be used.

3.6.2 Port status change wake-up register description

RPAGE～RD/ICIECR(P6 Port Interrupt Wake-up Enable Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	P6WK<5>	P6WK<4>	P6WK<3>	P6WK<2>	P6WK<1>	P6WK<0>

Bit<5:0>:P6WK<5:0>-P6 Port Interrupt Wake-up Enable

1: Enable

0: Disable(default)

Note: In OPTION for port wake-up setting, if P6 port is not independently controlled, port wake-up is not controlled by RD register; otherwise, the RD register needs to be processed, or the port cannot be woken up.

RPAGE～RE/CPUCON(CPU Mode Controls Registers)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPWM1	PWMCKS	TCCCKS	PWMWE	TCCWE	STPHX	CLKMD	IDLE

Bit<6>:PWMCKS-PWM clock source

1: Select system clock

0: Select the instruction cycle clock

Bit<5>:TCCCKS-TCC clock source

1: Select system clock

0: Select the instruction cycle clock

Bit<4>:PWMWE-PWM wake up

1:PWM wake up enable, can wake up IDLE mode

0:PWM wake up disable

Bit<3>:TCCWE-TCC wake up

1:TCC wake up enable, can wake up IDLE mode , RTC mode can wake up SLEEP and IDLE mode

0:TCC wake up disable

（Set TCCWE=1&RTCS=1 in RTC mode and LXT will continue to work when in SLEEP mode, otherwise LXT will stop when in SLEEP mode）

Bit<2>:STPHX- High-speed clock

1: Stop high speed clock, including IRC and crystal oscillator clock (excluding RTC clock)

0: The high speed clock is working properly

Bit<1>:CLKMD- System clock

1: The system clock uses a low speed RC oscillator clock

0: The system clock uses a high speed IRC or crystal oscillator clock

（When the system enters low speed mode from normal mode, set CLKMD=1 first, then set STPHX=1;When the system enters normal mode from low speed mode, STPHX=0 is set first, and CLKMD=0 is set later）

Bit<0>:IDLE-IDLE mode

1: When the system executes SLEEP instruction, it enters idle mode, and the system clock works normally

（TCC and PWM in idle mode, select the system clock can continue to work, and can wake up the system）

0: The system goes into SLEEP mode when it executes the SLEEP instruction

RPAGE～RF/ISR(Interrupt Flag Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	ADIF	T1IF	EXIF	ICIF	TCIF

Bit<1>:ICIF-P6 Port state change interrupt flag bit, software clear 0

1: interrupt request

0: no interrupt occurs

IOPAGF～IOCF/IMR(Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	ADIE	T1IE	EXIE	ICIE	TCIE

Bit<1>:ICIE- P6 port status change interrupt enable control

1: Enable

0: Disable (default)

3.6.3 Port status change query mode wake-up setting

1、PORT6 port wake-up port is set as input;

2、The internal pull-up or pull-down of the wake-up port can be selected according to the need;

3、Enable PORT6 port status change interrupt;

4、Enabling port state change independent interrupt and wake-up control;

5、Execute DISI instructions and do not enter the interrupt address port;

6、Execute the "SLEP" instruction and enter the sleep mode;

7、After waking up, execute the next instruction of SLEP.

3.6.4 Port status change interrupt wake-up settings

1、PORT6 port wake-up port is set as input;

2、The internal pull-up or pull-down of the wake-up port can be selected according to the need;
3、Enable PORT6 port status change interrupt;
4、Enabling port state change independent interrupt and wake-up control;
5、Execute "ENI" instructions and wait to enter the interrupt address port;
6、Instruct "SLEP" and enter the sleep mode;
7、After waking up, it will enter the interrupt address port. After exiting the interrupt, it will execute the next instruction of SLEP;

3.7 ADC Analog-to-digital Conversion Function Module

JZ8P2600C has 4 input channels and 12 bit accuracy. The completion of AD conversion can be interrupted, or it can be determined by querying the ADRUN bits.

The completion of the AD conversion can be awakened from idle mode if the AD wake-up function is enabled.

Calculation method of AD sampling time:

From ADRUN=1, the time to complete an AD sampling =ADC sampling retention period +AD conversion time.

AD conversion time:

It takes one TAD time for AD to convert 1 bit. We have a total of 12 bits of AD, so the conversion time is 12 TAD.

3.7.1 ADC analog-to-digital conversion register description

RPAGE～R7/ADCON(ADC control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADRUN	ADPD	VREFS	CALI	SIGN	VOF<2>	VOF<1>	VOF<0>

Bit<7>:ADRUN

1: ADC starts sampling

0: ADC no sampling or sampling ended

Bit<6>:ADPD

1:ADC Enable

0:ADC Disable (Turn off ADC in sleep mode, otherwise there will be power consumption)

Bit<5>:VREFS

1: ADC uses external reference voltage (P61 port)

0: ADC uses internal reference voltage

Bit<4>:CALI

1: ADC zero drift calibration enables

0: ADC zero drift calibration disables

Bit<3>:SIGN

1: ADC zero drift calibrates positive polarity

0: ADC zero drift calibrates negative polarity

Bit<2:0>:VOF<2:0> ADC zero drift calibration bits

VOF<2>	VOF<1>	VOF<0>	The calibration range
0	0	0	0 LSB
0	0	0	2 LSB
0	0	1	4 LSB
0	1	0	6 LSB
0	1	1	8 LSB
1	0	0	10 LSB
1	0	1	12 LSB

1	1	0	14 LSB

RPAGE～RF/ISR (Interrupt Flag Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	ADIF	T1IF	EXIF	ICIF	TCIF

Bit<4>:ADIF- ADC conversion completes the interrupt flag bit, software clear 0
1: interrupt request
0: no interrupt occurs

IOPAGE～IOC7 /ADCVS(AD channel/voltage/frequency division selection register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCKS<1>	ADCKS<0>	ADICS<2>	ADICS<1>	ADICS<0>	VREF<2>	VREF<1>	VREF<0>

Bit<7:6>:ADCKS<1:0>

CLKMD	ADCKS<1>	ADCKS<0>	ADC clocks
0	0	0	Fosc/16
0	0	1	Fosc/4
0	1	0	Fosc/64
0	1	1	Fosc/1
1	X	X	Fosc/1

Bit<5:3>:ADICS<2:0>

ADICS<2>	ADICS<1>	ADICS<0>	ADC channel selection
0	0	0	AD0（P60）
0	0	1	AD1（P62）
0	1	0	AD2（P64）
0	1	1	AD3（P65）
1	0	0	AD4（Internal reference）

AD value is calculated as follows: AD value = (reference voltage /VDD) *4096

Bit<2:0>:VREF<2:0>

VREF<2>	VREF<1>	VREF<0>	Internal reference voltage
0	0	0	VDD
0	0	1	4V
0	1	0	3V
0	1	1	2V
1	0	0	1.5V

IOPAGE～IOC8/ADATH(AD converts the high 8 bits of the value)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADAT<11>	ADAT<10>	ADAT<9>	ADAT<8>	ADAT<7>	ADAT<6>	ADAT<5>	ADAT<4>

Save the high 8 bits of the AD conversion result.

IOPAGE～IOCA/ADPS(AD sampling port enable and AD high 4 bit register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADEN<3>	ADEN<2>	ADEN<1>	ADEN<0>	ADAT<11>	ADAT<10>	ADAT<9>	ADAT<8>

Bit<7>:ADEN<3>
1: AD3 port as analog input port
0: AD3 port as GPIO
Bit<6>:ADEN<2>
1: AD2 port as analog input port
0: AD2 port as GPIO
Bit<5>:ADEN<1>
1: AD1 port as analog input port
0: AD1 port as GPIO
Bit<4>:ADEN<0>
1: AD0 port as analog input port
0: AD0 port as GPIO
Bit<3:0> ADAT<11:8> read-only
Note: Being an analog input port will disable other IO port functions including input, output, pull-up, pull-down, and other reuse functions

IOPAGE～IOCC/ADATL(AD converts the low 8 bits of the value)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADAT<7>	ADAT<6>	ADAT<5>	ADAT<4>	ADAT<3>	ADAT<2>	ADAT<1>	ADAT<0>

Save the low 8 bits of the AD conversion result.

IOPAGE～IOCE/WDTCR(WDT Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTEN	EIS	ADWE	VFOE	1	1	1	1

Bit<5>:ADWE-ADC wake-up control
0: Disable (default)
1: Enable
Bit<4>:VFOE-Internal reference voltage output
0: Internal reference voltage output is prohibited, P65 as GPIO (default)
1: The internal reference voltage output is enabled, with P65 as the analog port, and the output voltage is based on VREF<2：0> choose.

IOPAGF～IOCF/IMR(Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	ADIE	T1IE	EXIE	ICIE	TCIE

Bit<4>:ADIE-AD interrupt enable control
1: Enable
0: Disable (default)

3.7.2 ADC analog-to-digital conversion setup instructions

1、Configure the ADEN3:ADIS0 bit of register IOPAGE ~ IOCA/ADPS, Enables analog input channels.
2、Set register IOPAGE ~ IOC7/ADCVS, select AD input channel, select ADC clock pre-division frequency and select ADC reference voltage; Set "ADPD=1" to start AD power supply voltage;
3、If interrupts are needed, set ADIE=1 and execute "ENI";

4、You can enable AD wake-up function as required, and set ADWE=1;
5、Set "ADRUN=1" to start AD conversion;
6、Idle/Sleep mode can be selected as needed;
7、Wait for interrupt or ADRUN to be cleared 0;If AD interrupt occurs, ADIF should be cleared to "0" when leaving the interrupt program.
8、Save the results of the transformation. If you need to do multiple AD conversions, skip to Step 4.

3.8 PWM Pulse width modulation function module

JZ8P2600C provides a PWM signal of the same period, where the accuracy of PWM1, PWM2 and PWM3 is 8 bits. The PWM output waveform is determined by the period and duty cycle, and the transmission rate is the reciprocal of the period.

3.8.1 PWM Pulse Width Modulation Register Description

RPAGE～R8/PWMCON(PWM Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1EN	PWM3EN	PWM2EN	PWM1EN	T1PTEN	T1P<2:0>		

Bit<7>:T1EN-T1/PWM counter enable
1: Enable
0: Disable
Bit<6>:PWM3EN-PWM3 output enables control bits
1: Enable（P60 output PWM3）
0: Disable
Bit<5>:PWM2EN-PWM2 output enables control bits
1: Enable（P61 output PWM2）
0: Disable
Bit<4>:PWM1EN-PWM1 output enables control bits
1: Enable（P62 output PWM1）
0: Disable
Bit<3:0>:T1PTEN PT1P<2:0>-T1 frequency division selects the control bit

T1PTEN	PT1P<2>	PT1P<1>	PT1P<0>	T1 Frequency division ratio
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

RPAGE～R9/PRD(PWM Cycle Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD<7:0>							

T1/PWM Cycle Register

RPAGE～RA/PDC1(PWM1 Duty Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC1<7:0>							

Bit<7:0>:PDC1<7:0>-PWM1 Duty Register

RPAGE～RB/PDC2(PWM2 Duty Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

PDC2<7:0>

Bit<7:0>:PDC2<7:0>-PWM2 Duty Register

RPAGE～RC/PDC3(PWM3 Duty Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDC3<7:0>							

Bit<7:0>:PDC3<7:0>-PWM3 Duty Register

RPAGE～RE/CPUCON(CPU Mode Controls Registers)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPWM1	PWMCKS	TCCCKS	PWMWE	TCCWE	STPHX	CLKMD	IDLE

Bit<7>:IPWM1-PWMcomplementary output
1:PWM1 reverse phase output
0:PWM1 normal output
Bit<6>:PWMCKS-PWM clock source
1: Select system clock
0: Select the instruction cycle clock
Bit<4>:PWMWE-PWM wake up
1:PWM wake up enable, can wake up IDLE mode
0:PWM wake up disable

RPAGE～RF/ISR(Interrupt Flag Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	ADIF	T1IF	EXIF	ICIF	TCIF

Bit<3>:T1IF-T1/PWM cycle interrupt flag bit, software clear 0
Note: "MOV RF, A" should be used to clear the interrupt flag. BTC/AND RF, A instructions should not be used.

IOPAGF～IOCF/IMR(Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	ADIE	T1IE	EXIE	ICIE	TCIE

Bit<3>:T1IE-T1 interrupt enable control
1: Enable
0: Disable (default)

3.8.2 PWM Pulse width modulation setting instructions

1、 Set the PWMCON register, select the corresponding timer as the PWM mode, the timer division ratio, the timer interrupt type (if the PWM interrupt is enabled), the clock source of the timer, etc.
2、Write the value of the RPAGE-R9 register to determine the Period of the PWM channel;
3、Write the value of the PDCX register to determine the Duty of the PWM channel;
4、Enable the corresponding timer;
5、Enable or disable the timer interrupt corresponding to PWM and execute the "ENI" or "DISI" instruction (if needed).

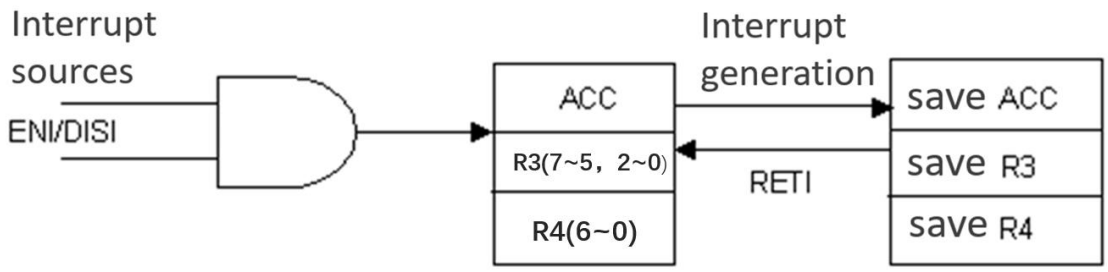
3.9 Interrupt Function Module

JZ8P2600C has 4 interrupt sources. Regardless of which interrupt is used, the total interrupt must be enabled, that is, the "ENI" instruction is executed. The following are the characteristics of each interrupt, the interrupt address and the priority level:

	Interrupt Sources	Enable Condition	Interrupt Flag	Interrupt vector
External	External Interrupt	ENI + EXIE = 1	EXIF	008H
External	Port input status change	ENI + ICIE = 1	ICIF	008H
Internal	TCC overflow interrupt	ENI + TCIE = 1	TCIF	008H
Internal	T1/PWM cycle interrupt	ENI + T1IE = 1	T1IF	008H
Internal	AD conversion interrupted	ENI + ADIE = 1	ADIF	008H

RPAGE~RF are interrupt status flag registers that record the value of the interrupt flag bit when an interrupt generates an interrupt request. IOPAGF～IOCF are interrupt setting registers. The enable and disable of interrupts are set in these two registers. The total interrupt is enabled by executing the "ENI" instruction. Conversely, the total interrupt is disabled by the "DISI" instruction. When an interrupt is generated, its next instruction will be executed from their specific address. The corresponding interrupt flag must be cleared before leaving the interrupt service routine to avoid interrupted malfunctions.

When the interrupt subroutine is executed, the contents of ACC, R3, and R4 need to be kept manually. After the subroutine is completed, we need to load the saved values into ACC, R3, R4 manually. This is to avoid changing the values of ACC, R3, and R4 when the interrupt subroutine is executed, resulting in an error when returning to the main program. As shown below:



3.9.1 Interrupt register description

RPAGE～RF/ISR(Interrupt Flag Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	ADIF	T1IF	EXIF	ICIF	TCIF

Bit<4>:ADIF- ADC conversion completes the interrupt flag bit, software clear 0

Bit<3>:T1IF-T1/PWM cycle interrupt flag bit, software clear 0

Bit<2>:EXIF-External interrupt flag bit (set 1 by drop edge of EXINT pin, software clear 0)
Bit<1>:ICIF-P6 Port state change interrupt flag bit, software clear 0
Bit<0>:TCIF-TCC interrupt flag bit, software clear 0
1: interrupt request
0: no interrupt occurs
Note: "MOV RF, A" should be used to clear the interrupt flag. BTC/AND RF, A instructions should not be used.

IOPAGF～IOCF/IMR(Interrupt Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	ADIE	T1IE	EXIE	ICIE	TCIE

Bit<4>:ADIE-AD interrupt enable control
1: Enable
0: Disable (default)
Bit<3>:T1IE-T1 interrupt enable control
1: Enable
0: Disable (default)
Bit<2>:EXIE- External interrupt enable control
1: Enable
0: Disable (default)
Bit<1>:ICIE- P6 port status change interrupt enable control
1: Enable
0: Disable (default)
Bit<0>:TCIE- TCC overflow interrupt enable control
1: Enable
0: Disable (default)

3.10 Reset function module

3.10.1 Reset function overview

JZ8P2600C chip provides 3 reset modes:

1、Power-on reset and Low voltage reset;

2、RESET pin input low level reset;

3、WDT overflow reset;

The first reset time is determined by the SUT in OPTION, as shown in the following table:

Power-on reset setup time:

SUT	Reset setup time
PWRT=WDT=18ms	Reset setup time = 18ms
PWRT=WDT=4.5ms	Reset setup time = 4.5ms
PWRT=WDT=72ms	Reset setup time = 72ms
PWRT=WDT=288ms	Reset setup time = 288ms
PWRT=140us WDT=18ms	Reset setup time =140us
PWRT=140us WDT=4.5ms	Reset setup time =140us
PWRT=140us WDT=72ms	Reset setup time =140us
PWRT=140us WDT=288ms	Reset setup time =140us

When any of the above resets occur, all system registers are restored to their default state, the program stops running, and the program counter PC is cleared. After the reset is complete, the system restarts from vector 0000H.

Any kind of reset situation requires a certain response time, and the system provides a complete reset process to ensure the smooth operation of the reset action. For different types of oscillators, the time required to complete the reset is different. Therefore, the rising speed of VDD and the start-up time of different crystals are not fixed. The RC oscillator has the shortest start-up time and the crystal oscillator has a longer start-up time. In the process of using the user terminal, the requirements of the host for the power-on reset time should be considered.

3.10.2 Power-on reset

Power-on reset is closely related to LVR operation. The process of powering on the system is in the form of a gradually rising curve, which takes a certain amount of time to reach the normal level.

Power-on: The system detects that the power supply voltage has risen and waits for it to stabilize;

External Reset (External Reset Pin Enable Only): The system detects the status of the external reset pin. If not high level, the system remains in reset until the external reset pin is released;

System initialization: all system registers are set to initial values;

The oscillator starts working: the oscillator starts to provide the system clock;

Execution procedure: At the end of power-on, the program starts running.

3.10.3 WDT reset

The watchdog reset is a protection setting for the system. In the normal state, the watchdog timer is cleared by the program. If an error occurs, the system is in an unknown state and the watchdog timer overflows and the system is reset. After the WTD reset, the system restarts to the normal state.

Watchdog timer status: The system detects if the watchdog timer overflows. If it overflows, the system resets.

System initialization: all system registers are set to the default state;

The oscillator starts working: the oscillator starts to provide the system clock;

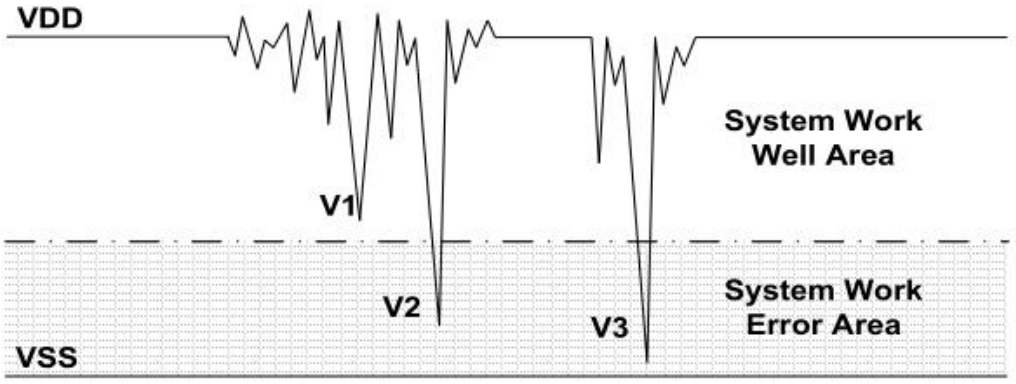
Execution procedure: At the end of power-on, the program starts running.

Watchdog Timer Application Notes:

- Checking the status of the I/O port and the contents of the RAM before the watchdog is cleared which can improve the reliability of the program before the watchdog is cleared.
- The watchdog cannot be cleared in the interrupt; otherwise the main program cannot be detected.
- The program should only have the action of clearing the watchdog in the main program. This architecture can maximize the protection function of the watchdog.

3.10.4 LVR low voltage reset

Power-down reset, system voltage dip caused by external factors (for example, interference or changes in external load). A brown-out may cause the system to malfunction or program execution errors.



Voltage drops can enter the system dead zone. The system dead zone means that the power supply does not meet the minimum operating voltage requirements of the system. The figure above is a typical power-down reset diagram. In the figure, VDD is severely disturbed and the voltage drop is very low. The system above the dotted line works normally. In the area below the dotted line, the system enters an unknown working state. This area is called the dead zone. When VDD falls to V1, the system is still in a normal state; when VDD falls to V2 and V3, the system enters the dead zone, which is easy to cause an error. The system may enter the dead zone in the following cases:

DC application:

In DC applications, battery power is generally used. When the battery voltage is too low or the microcontroller drives the load, the system voltage may drop and enter the dead zone. At this time, the power supply does not fall further to the LVD detection voltage, so the system remains in the dead zone.

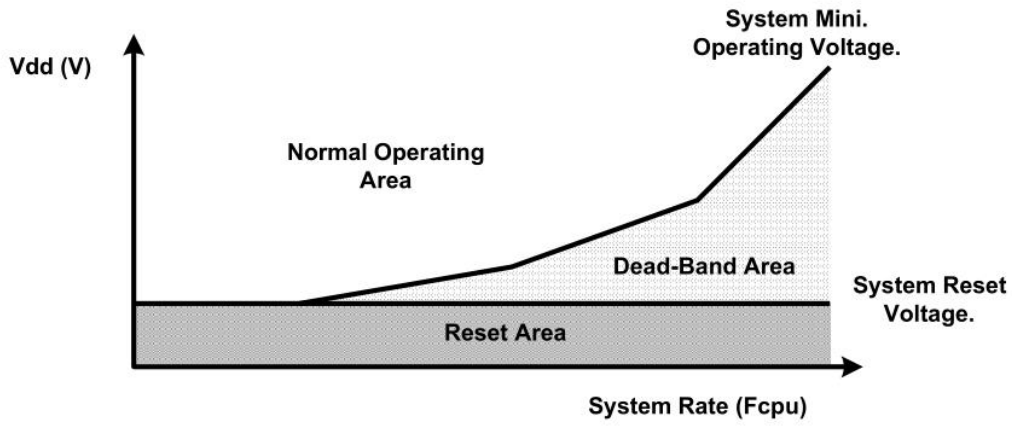
AC application:

When the system is powered by AC, the DC voltage value is affected by noise in the AC power supply. When the external load is too high, such as driving the motor, the interference caused by the load action also affects the DC power supply. If VDD falls below the minimum operating voltage due to interference, the system may enter unstable operation.

In the AC application, the system has a long time to power on and off. Among them, the power-on sequence protection makes the system power on normally, but the power-off process is similar to that in the DC operation. After the AC power is turned off, the VDD voltage is easy to enter the dead zone during the slow decline.

3.10.5 Relationship between working frequency and LVR low voltage detection

In order to improve the performance of the system power-down reset, it is necessary to clarify that the system has the minimum operating voltage value. The minimum operating voltage of the system is related to the system execution speed, and the minimum operating voltage value is different at different execution speeds.



As shown in the figure above, the normal operating voltage range of the system is generally higher than the system reset voltage, and the reset voltage is determined by the low voltage detection (LVR) level. When the system execution speed is increased, the minimum operating voltage of the system is also increased accordingly. However, since the system reset voltage is fixed, a voltage region will appear between the system minimum operating voltage and the system reset voltage, and the system will not work normally or reset, this area is the dead zone.

To avoid dead band voltage, select the appropriate LVR reset voltage point when selecting the operating frequency. The following table:

Operating Frequency	LVR Reset Voltage Point
IRC-8M, 2Clock	LVR=2.7V
IRC-8M, 4Clock	LVR=1.8V

IRC-8M,8Clock	LVR=1.8V
IRC-910KHz,2Clock	LVR=1.8V

Note: The corresponding value of this operating frequency and LVR reset voltage point is only the recommended value. During the use, the reset voltage point can be adjusted appropriately according to the specific application.

3.10.6 Register power reset value

Address	Register	Reset Value	Addres	Registe	Reset Value
0x0	R0	-	0x0	-	-
0x1	R1(TCC)	0000 0000	0x1	-	-
0x2	R2(PC)	0000 0000	0x2	CONT	0000 1111
0x3	R3(STATUS)	0001 1uuu	0x3	-	-
0x4	RSR	1uuu uuuu	0x4	-	-
0x5	-	-	0x5	-	-
0x6	PORT6	0011 1111	0x6	P6CR	1111 1111
0x7	ADCON	0000 0000	0x7	ADCVS	0000 0000
0x8	PWMCON	0000 0000	0x8	ADATH	uuuu uuuu
0x9	PRD	0000 0000	0x9	PHDCR	1111 1111
0xA	PDC1	0000 0000	0xA	ADPS	0000 uuuu
0xB	PDC2	0000 0000	0xB	PDCR	1111 1111
0xC	PDC3	0000 0000	0xC	ADATL	uuuu uuuu
0xD	ICIECR	0000 0000	0xD	PHCR	1111 1111
0xE	CPUCON	0000 0000	0xE	WDE	1000 1111
0xF	ISR	0000 0000	0xF	IMR	0000 1111
0x10~0x3f	General purpose register	uuuu uuuu			

U= Unknown state;

3.11 System clock function module

JZ8P2600C provides internal RC mode with frequency options of 910KHz and 8MHz.

IRC working frequency can be selected by setting the configuration bit of OPTION, and the corresponding relationship is as follows:

Firc	IRC Frequency
8 M	IRC frequency is 8MHz
910 KHz	IRC frequency is 910KHz

JZ8P2600C provides a variety of frequency division options, which can be selected in OPTION, suitable for more occasions. The following table:

Clocks	Clocks Frequency Division
2clock	Frequency division is 2clock
4clock	Frequency division is 4clock
8clock	Frequency division is 8clock
16clock	Frequency division is 16clock
32clock	Frequency division is 32clock

4 CODE OPTION Register

CODE OPTION	Option	Description of function
WTD	Enable	WDT is enabled
	Disable	WDT is disabled(default)
Clocks Frequency Division	2 Clocks	Instruction cycle selects 2 clock
	4 Clocks	Instruction cycle selects 4 clock
	8 Clocks	Instruction cycle selects 8 clock
	16 Clocks	Instruction cycle selects16 clock
	32 Clocks	Instruction cycle selects 32 clock
IRC Frequency	8M	IRC frequency selects 8M
	910KHz	IRC frequency selects 910KHz
Low Voltage Reset	Disable	Low voltage reset is disabled
	LVR=1.2V	Low voltage reset point selects 1.2V
	LVR=1.6V	Low voltage reset point selects 1.6V
	LVR=1.8V	Low voltage reset point selects 1.8V
	LVR=2.4V	Low voltage reset point selects 2.4V
	LVR=2.7V	Low voltage reset point selects 2.7V
	LVR=3.3V	Low voltage reset point selects 3.3V
	LVR=3.6V	Low voltage reset point selects 3.6V
	LVR=3.9V	Low voltage reset point selects 3.9V
OTP paging selection	Use 2 k	Program uses 2K capacity
	Use the front 1K	The program uses the first half of the OTP with 1K capacity
	Use the back 1K	The program uses the second half of the OTP with 1K capacity
2K code encryption	2k encryption	Data encryption
	2k without encryption	Data unencrypted
Reset Port Pull-up	Enable	Enable P63 port pull up
	Disable	Disable P63 port pull up
P63 Port	GPIO	P63 is a general purpose input/output port
	GPI	P63 is a general purpose input port
	RST	P63 is an external reset port

Reset Time	PWRT=WDT=4.5ms	Wake-up setup time =WDT overflow time (no prescale)= 4.5ms
	PWRT=WDT=18ms	Wake-up setup time = WDT overflow time (no prescale)= 18ms
	PWRT=WDT=72ms	Wake-up setup time = WDT overflow time (no prescale)= 72ms
	PWRT=WDT=288ms	Wake-up setup time = WDT overflow time (no prescale)= 288ms
	PWRT=140us,WDT=4.5ms	Wake-up setup time =140us, WDT overflow time (no prescale)=4.5ms
	PWRT=140us,WDT=18ms	Wake-up setup time =140us, WDT overflow time (no prescale)=18ms
	PWRT=140us,WDT=72ms	Wake-up setup time =140us, WDT overflow time (no prescale)=72ms
	PWRT=140us,WDT=288ms	Wake-up setup time =140us, WDT overflow time (no prescale)=288ms
Port Characteristics	EMC	The port input characteristic is Schmidt EMT characteristic (see 3.3 for details)
	SMT	The port input characteristic is Schmidt SMT characteristics (see 3.3 for details)
	HSMT	The port input characteristic is Schmidt HSMT characteristics (see 3.3 for details)
	INV	The port input characteristic is the inverter INV characteristic (see 3.3 for details)
P6 Port Wake up	Independent control	P6 port independent control wake-up (0x0D register needs to be set)
	No Independent control	P6 port is not independently control wake-up
Drive Enhancement	Disable	Port drive capability enhancement disable
	Enable	Port drive capability enhanced enable
ADC sampling retention time	12TAD	ADC sampling retention time is 12TAD
	8TAD	ADC sampling retention time is 8TAD
	4TAD	ADC sampling retention time is 4TAD
	2TAD	ADC sampling retention time is 2TAD
The ADC sample value is forced up by 14 least-significant bits	Enable	Enable the ADC sampling value to force up by 14 least-significant bits
	Disable	Disallow the ADC sampling value to force up to 14 least-significant bits
IRC	LDO	IRC oscillator voltage source select LDO

oscillator		
voltage source	VDD	IRC oscillator voltage source select VDD
Power	HIGH	VDD Voltage Select HIGH
	LOW	VDD Voltage Select LOW

5 Electrical Characteristics

5.1 Chip limit parameter

Operating temperature	(√) E:-40-85;
Storage temperature (℃):	(√) -65～+150;
Limit voltage (V)	(√) other -0.3～6;
Limit input voltage (V)	(√) other GND-0.3～VDD+0.5;
Limit output voltage (V)	(√) other GND-0.3～VDD+0.5;

5.2 Chip DC parameters

(T=25℃, VDD=5V)

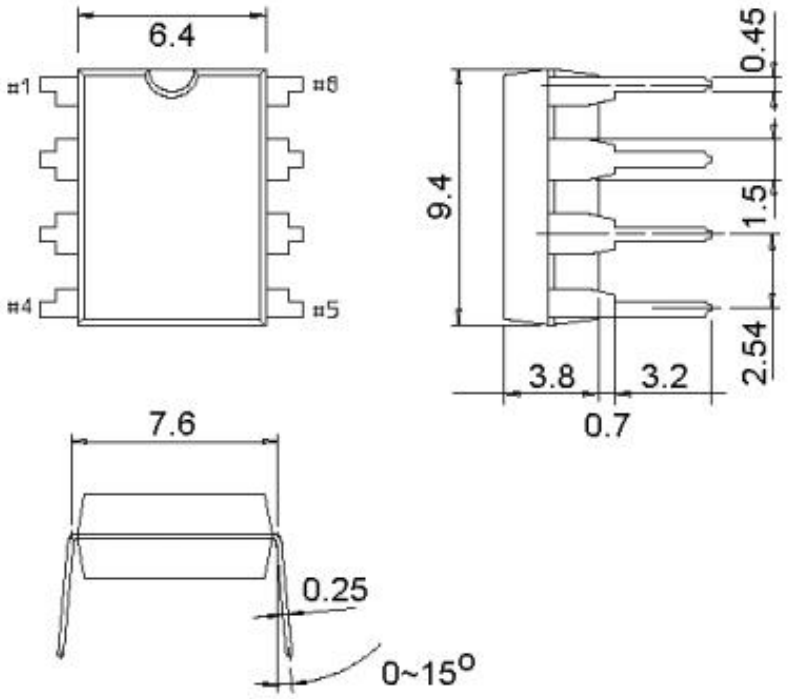
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
IRC1	IRC1 (after correction)	OPTION select 8MHz	-	8	-	MHz
IRC3	IRC3 (after correction)	OPTION select 910KHz	-	910	-	KHz
IOH1	Output high level drive (except P63)	Ioh=4.4V	4.5	5	5.5	mA
IOH2	Output high level drive enhancement (P63)	Ioh=4.4V	11	12	-	mA
IOH3	Output high level drive enhancement (except P63)	Ioh=4.4V	12	13	14	mA
IOL1	IO output low level drive (except P63)	Iol=0.6V	16	17	18	mA
IOL2	IO output low level drive (P63)	Iol=0.6V	13	14	15	mA
IOL3	IO output low level drive enhancement (except P63)	Iol=0.6V	25	26	28	mA
IOL4	IO output low level drive enhancement (P63)	Iol=0.6V	19	20	21	mA
IOL5	Secondary drive enhancement (P60,P61,P62)	Iol=0.6V	32	33	34	mA
IPH1	Pull-up current (except P63)	Pull-up enable, input is connected to	80	118	130	μA
IPH2	Pull-up current (P63)	Pull-up enable, input is connected to	80	100	130	μA
IPD	Pull-down current (except P63)	Pull-down enable, input is connected to	45	55	80	μA
Isb1	Shutdown current 1	All inputs are connected to VDD, the output is left floating, WDT, LVD	-	-	1	μA

		disabled				
Isb2	Shutdown current 2	All inputs are connected to VDD, the output is left floating, WDT, LVD disabled	-	-	12	μA
Isb3	Shutdown current 3	RTC mode, internal capacitance 12.5 PF	-	-	15	μA
Iop2	Working current 1（VDD=5V）	IRC=8MHz 2clock	-	1.2	1.5	mA
Iop2	Working current 2（VDD=5V）	IRC=1MHz 2clock	-	0.2	0.3	mA
LVR	Low voltage reset voltage	Select Vlvr reset point	Vlvr-0.2	Vlvr	Vlvr+0.2	V
Note: LVD is affected by power supply, the above parameters are for reference only, please refer to the measured data of target prototype.						

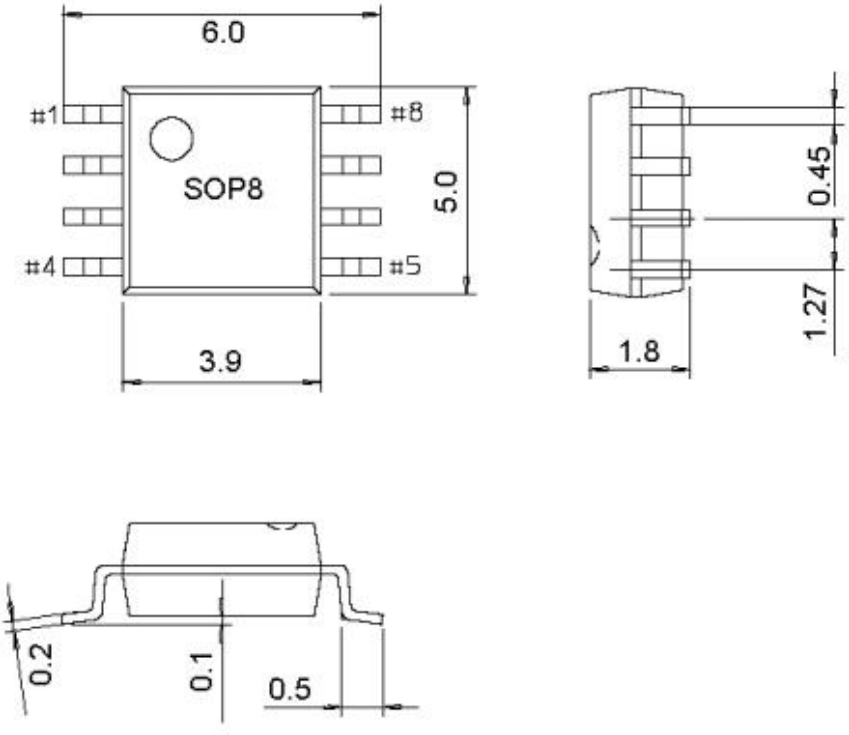
6 Package size information

6.1 8PIN Package Size

unit: mm



DIP8 Package Size



SOP8 Package Size