JZ8P2603

8-BIT Microcontroller

Product Specification

Version 2.3

Revision History

Version	Revision Description	Remake
V1.0	Initial version	
V1.1	Modify the RPAGE operation instructions	
V1.2	Modify ADC Description	
V1.3	Modify the programming configuration instructions	
V1.4	Added description	
V1.5	Modify the flip level electrical parameters	
V1.6	Modify internal reference voltage	
V2.0	Revised	
V2.2	Modify the pin map	
V2.3	Modifying the Content Format	

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- The test data are for reference only. The actual data are subject to the target prototype test.

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1 General Description

1.1 Features

CPU configuration

- 2×16Bit OTP ROM
- 80-Bit SRAM
- 8-level stacks for subroutine nesting
- 4-level programmable voltage detection (LVD)
  4.5V, 4.0V, 3.3V, 2.2V
- 5-level programmable voltage reset (LVR) 4.0V, 3.5V, 2.7V, 1.8V, 1.6V
- Operating current is less than 2 mA (4MHz/5V)
- Operating current 30 μA (32kHz/3V)
- Sleep current is less than 1 μA (sleep mode)

I/O port configuration

- 3 bidirectional I/O ports: P5, P6, P7
- 18 I/O pins
- Wake-up port:P5
- 16 programmable pull-high pins
- 8 programmable pull-down pins
- 8 programmable open-drain I/O pins
- 14 programmable drive enhanced I/O pins
- External interrupt: P60

Operating voltage range

- Operating voltage range:
  1.8V～5.5V (0℃-70℃)
  2.3V～5.5V (-40℃-85℃)

Operating frequency range

(based on 2Clock)

- build-in IRC oscillator:
  16MHz, 8MHz, 4MHz, 1MHz
- External ERC oscillation circuit:
- External XT oscillator circuit:
  DC～16MHz (Above 4.5V)
  DC～8MHz (Above 3V)
  DC～4MHz (Above 2.5V)
- Choice of Clock Period Frequency Division:
  2Clock, 4Clock, 8Clock, 16Clock

Peripheral configuration

- 8Bit real time clock / counter
- 8-channel 12Bit ADC analog-to-digital converter
- A pair of comparator (CMP) or Operational amplifier o (OP)
- Two Pulse Width Modulation (PWM) with 8-bit resolution

Interrupt sources

- TCC overflow interrupt
- External interrupt
- Input-port status changed interrupt
- ADC completion interrupt
- Comparator status change interrupt
- Low voltage detect (LVD) interrupt
- PWM1 period/ duty match interrupt
- PWM2 period/ duty match interrupt

Special Features:

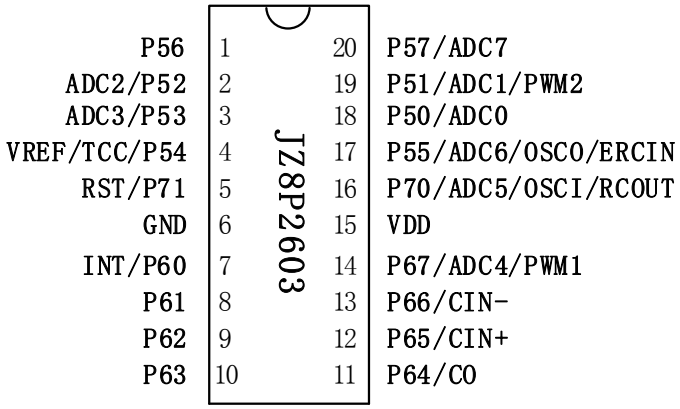
- Programmable free running Watchdog Timer
- Four working mode switching

Package Type:

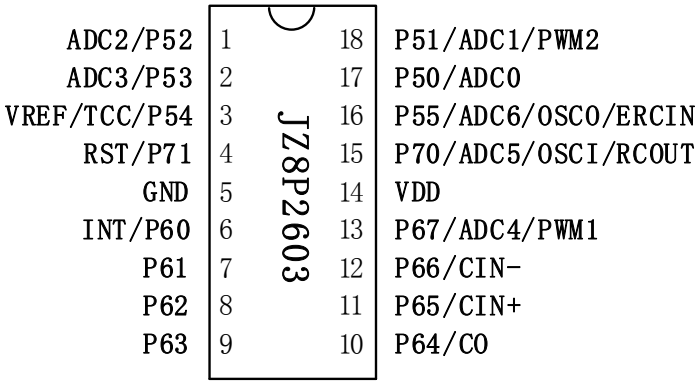
- JZ8P2603-DIP20;

- JZ8P2603-SOP20;
- JZ8P2603-DIP18;
- JZ8P2603-SOP18;
- JZ8P2603-DIP16;
- JZ8P2603-SOP16;
- JZ8P2603-DIP14;
- JZ8P2603-SOP14;
- JZ8P2603-DIP8;
- JZ8P2603-SOP8;
- JZ8P2603-MSOP10;

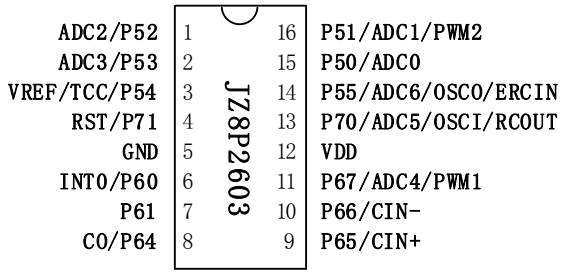
1.2 Pin Assignment



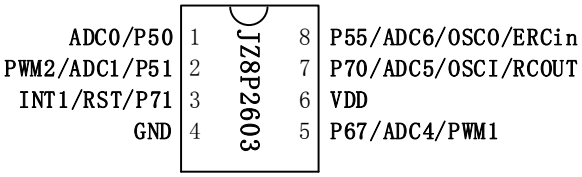
JZ8P2603-20 PIN map



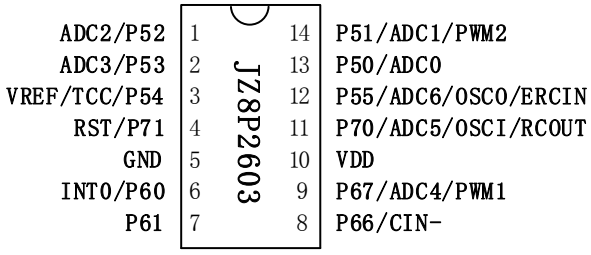
JZ8P2603-18 PIN map



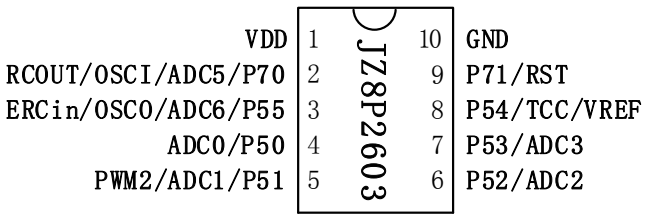
JZ8P2603-16 PIN map



JZ8P2603-8 PIN map



JZ8P2603-14 PIN map



JZ8P2603-10 PIN map

1.3 Pin Description

NUM.	Name	I/O	Description
P50	P50	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up
	ADC0	AN	ADC Input 0
P51	P51	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up
	ADC1	AN	ADC Input 1
	PWM2	CMOSoutput	PWM2 output
P52	P52	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up
	ADC2	AN	ADC Input 2
P53	P53	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up
	ADC3	AN	ADC Input 3
P54	P54	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up
	TCC	SMT	Real Time Clock/Counter clock input
	VREF	AN	ADC external voltage reference
P55	P55	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up
	ADC6	AN	ADC Input 6
	OSC0	XTAL	Clock output of crystal/ resonator oscillator
	ERCin	AN	External RC input pin
P56	P56	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up
P57	P57	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable pull-down, pull-high and pin change wake-up
	ADC7	AN	ADC Input 7
P60	P60	I/O (pull-high)	Bidirectional I/O pin with programmable open-drain, pull-high
	INT0	I (SMT)	External interrupt input pin

P61	P61	I/O (pull-high)	Bidirectional I/O pin with programmable open-drain, pull-high
P62	P62	I/O (pull-high)	Bidirectional I/O pin with programmable open-drain, pull-high
P63	P63	I/O (pull-high)	Bidirectional I/O pin with programmable open-drain, pull-high
P64	P64	I/O (pull-high)	Bidirectional I/O pin with programmable open-drain, pull-high
	CO	O	Comparator output
P65	P65	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable open-drain, pull-high
	CIN+	I	Non-inverting end of Amplifier
P66	P66	I/O (pull-high or pull-down)	Bidirectional I/O pin with programmable open-drain, pull-high
	CIN-	I	Inverting end of Amplifier
P67	P67	I/O (pull_high)	Bidirectional I/O pin with programmable open-drain, pull-high
	ADC4	AN	ADC Input 4
	PWM1	CMOSoutput	PWM1 output
P70	P70	I/O	Bidirectional I/O pin with programmable pull-down, pull-high
	ADC5	AN	ADC Input 5
	OSCI	I (XTAL)	Clock input of crystal/ resonator oscillator
	RCOUT	O	Clock output of RC oscillator
P71	P71	I/O	Bidirectional I/O pin
	RESET	I (SMT)	System reset pin
	VDD	--	Power
	VSS	--	Ground

2 Memory structure

2.1 Data memory Configuration

2.1.1 RPAGE and Bank data register configuration

0x00	R0 Indirect Addressing Register	Reserved
0x01	R1 Timer Clock Counter	Reserved
0x02	R2 Program Counter	Reserved
0x03	R3 STATUS Status Register	Reserved
0x04	R4 FSR RAM Select register	Reserved
0x05	R5 PORT5 Data register	R5 TBHP：Table Point Register
0x06	R6 PORT6 Data register	R6 TBLP：Table Point Register
0x07	R7 PORT7 Data register	R7 PWM Control Registe
0x08	R8 ADC Input Select Register	R8 TMR Control Registe

0x09	R9 ADC Control Register	R9 PWM1 Time Period
0x0A	RA ADC Offset Calibration Register	RA PWM2 Time Period
0x0B	RB Converted value AD11~AD4 of ADC	RB PWM1 Duty Cycle
0x0C	RC Converted value AD11~AD8 of ADC	RC PWM2 Duty Cycle
0x0D	RD Converted value AD7~AD0 of ADC	Reserved
0x0E	RE Interrupt Status 2 and Wake-up Control Register 1	RE LVD and external interrupt control registers
0x0F	RF Interrupt Flag 1 Register	RF System clock and status control register
0x10 ～ 0x1F	16-Byte Common Register	
	Bank0	Bank1
0x20 ～ 0x3F	Common Register 32*8Bit	Common Register 32*8Bit

2.1.2 IOPAGE data register configuration

address	IOPAGE0 page register	IOPAGE1 page register
0x00	Reserved	Reserved
0x01	Reserved	Reserved
0x02	Reserved	Reserved
0x03	Reserved	Reserved
0x04	Reserved	Reserved
0x05	IOC50 P5 Direction control register	IOC51 P5 High Sink Control Register
0x06	IOC60 P6 Direction control register	IOC61 P6High Sink Control Register
0x07	IOC70 P7 Direction control register	IOC71 P5 High Driver Control Register
0x08	IOC80 Comparator Control Register	IOC81 P6 High Driver Control Register
0x09	IOC90 TMR1 Register	Reserved

0x0A	IOCA0 TMR2 Register	Reserved
0x0B	IOCB0 P5 Pull-down Control Register	Reserved
0x0C	IOCC0 P6 Open-drain Control Register	Reserved
0x0D	IOCD0 P5 Pull-high Control Register	Reserved
0x0E	IOCE0 WDT Control Register and Interrupt Enable Register 2	Reserved
0x0F	IOCF0 Interrupt Enable Register 1	IOCF1 P6 Pull-high Control Register

3 Functional Description

3.1 Operational Registers

3.1.1 RPAGE0～R0 (Indirect Address Register)

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the low 6-bit RAMS<5:0> of RAM Select Register (R4).

3.1.2 RPAGE0～R1 (TCC Time Clock/Counter)

TMR is an 8Bit Count-Up counter. An internal clock/external clock can be selected as the clock source. Count overflow can form an interrupt, and TMR can be read and written.

TCC can be triggered by a signal edge or an instruction cycle on the EXINT pin to generate an add 1 operation (defined by the CONT.4 bit). If the PAB bit (CONT.3) is cleared, a prescaler is assigned to the TCC. When the TCC register is written to a value, the value of the prescaler is cleared.

3.1.3 RPAGE0～R2 (PC Program Counter)

The program counter (PC) is a pointer for recording instructions to be processed by the CPU in each instruction cycle. During the CPU run cycle, the PC advances the instruction pointer to the program memory, and then increments the pointer by one to advance to the next cycle. The JZ8P2603 has a 13-bit wide program counter (PC) with low bytes from a readable and writable PCL.

The JZ8P2603 stack is used to record the instruction pointer returned by the program. When a subroutine is called, the PC pushes the instruction pointer onto the stack. When the return instruction is to be executed, the stack sends the instruction pointer back to the PC to continue the original process. The JZ8P2603 has an 8-level stack that does not occupy program memory space or data memory space, and the stack pointer cannot be read or written.

(1) Register PC and built-in 8-level stack are 13-bit wide for 2K×16Bit ROM addressing, JZ8P2603 program memory area mapping.

(2) In general, the PC is incremented by one; when reset, all bits of the PC are cleared.

(3) The instruction "JMP" allows direct loading of the lower 10-bit address, so the JMP instruction can implement any position jump within the current page (within 1K range). The instruction "JMP" directly loads the lower 10-bit address and pushes the PC +1 onto the stack. The subroutine entry address can be accurately located within the same page.

(4) The top-of-stack data is sent to the PC when the "RET" (RETL K, RETI) instruction is executed.

(5) The work of the stack is like a circular buffer. That is to say, after the stack is pushed 8 times, the data pushed on the stack at the 9th time will cover the data pushed on the stack at the 1st time, and the data pushed on the stack at the 10th time will cover the data pushed on the stack at the 2nd time, and so on.

3.1.4 RPAGE0～R3 (STATUS Status Register))

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	IOCS	-	T	P	Z	DC	C

Bit<7>: RST: Bit of reset type:
0: if wake-up from other reset types.
1: if wake-up from sleep on pin change, comparator status change, or AD conversion completed.

Bit<6>: IOCS: IOCPAGE Select the Segment
0: Segment IOCPAGE0 selected
1: Segment IOCPAGE1 selected

Bit<4>: T: Time-out bit
0: WDT time-out
1: execute the "SLEP" and "WDTC" commands or during Low voltage reset

The events affecting T/P are shown in the following table:

Type	RST	T	P
power on	0	1	1
/RESET during Operating mode	0	hold	hold
/RESET wake-up during Sleep mode	0	1	0
WDT time-out in working mode	0	0	hold
wakes up for WDT time-out	0	0	0
Wake-up on pin change during Sleep mode	1	1	0
WDTC instruction	hold	1	1
SLEEP instruction	hold	1	0

Bit<3>: P: Power-down bit:
0: execute "SLEP" command

1: during power-on or by a "WDTC" command

Bit<2>: Z: Zero flag:

0: if the result of an arithmetic or logic operation is zero.

1: if the result of an arithmetic or logic operation is not zero.

Bit<1>: DC: Auxiliary carry flag:

0: When the addition operation is performed, the lower four bits do not generate a carry or when the subtraction operation is performed, the lower four bits do not generate generated a borrow

1: When the addition operation is performed, the lower four bits do not generate a carry or when the subtraction operation is performed, the lower four bits do not generate generated a borrow

Bit<0>: C: Carry flag:

0: When the addition operation is performed, the upper four bits do not generate a carry or when the subtraction operation is performed, the upper four bits do not generate generated a borrow

1: When the addition operation is performed, the upper four bits do not generate a carry or when the subtraction operation is performed, the upper four bits do not generate generated a borrow

3.1.5 RPAGE0～R4 (FSR RAM Select Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBANK	BANK	FSR<5:0>					

FSR<7>: SBANK

Special Register 0x05~0x0F bank selection bit.

FSR<6>: BANK Used to select Bank 0 or Bank 1 of the register (0x20-0x3F)

0: Bank0

1: Bank1

FSR<5:0> Used to select a register (Address: 00~0F, 10~3F) in indirect addressing mode. (Address::0X00～0X3F)

The user can place the address corresponding to a register into the FSR. And then through accessing indirect addressing Register R0, the address will point to the register of the corresponding address in the FSR.

3.1.6 RPAGE0 R5～R7(Port 5 ~ Port 7))

I/O registers.

3.1.7 RPAGE0～R8(AD Channel enable register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE<7>	ADE<6>	ADE<5>	ADE<4>	ADE<3>	ADE<2>	ADE<1>	ADE<0>

Bit<7:0>:ADE<7:0>- AD channel enable control bit

1: Enable

0: Disable

Channel number	Enable control	pin
AD0	ADE<0>	P50
AD1	ADE<1>	P51

AD2	ADE<2>	P52
AD3	ADE<3>	P53
AD4	ADE<4>	P67
AD5	ADE<5>	P70
AD6	ADE<6>	P55
AD7	ADE<7>	P57

AD channel enable register is readable and writable

3.1.8 RPAGE0～R9(ADC Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR<1:0>		ADRUN	ADPD	ADIS<2:0>		

Bit<7>: VREFS-ADC the input source of Vref of the ADC

1: External reference (from P54 input voltage as ADC reference voltage)

0: Internal reference

Bit<6:5>:CKR<1:0>（**ADC Clock Rate Select**, Set the value of the minimum time of unit TAD）

CPUS	CKR<1>	CKR<0>	ADC Clock
1	0	0	Fosc/16
1	0	1	Fosc/4
1	1	0	Fosc/64
1	1	1	Fosc/1
0	x	x	Fosc/1

Note: Fosc represents the oscillator clock. For example, if IRC is selected for 4M, Fosc=4M.

For example: Fosc=4M, TAD is set to Fosc/4, then TAD=1uS

Bit<4>: ADRUN-ADC ADC starts to RUN

1: An A/D conversion is started. This bit can be set by software

0: on completion of the conversion Reset by hardware. This bit cannot be reset through software (default))

Bit<3>: ADPD-ADC ADC Power

1: Enable

0: Disable

Bit<2:0>: ADIS<2:0>-ADC Analog Input Select

ADICS	ADIS<2>	ADIS<1>	ADIS<0>	Analog Input Select
0	0	0	0	P50
0	0	0	1	P51
0	0	1	0	P52
0	0	1	1	P53
0	1	0	0	P67
0	1	0	1	P70
0	1	1	0	P55

0	1	1	1	P57
1	0	0	0	OPOUT
1	1	0	0	0.25*VDD

3.1.9 RPAGE0～RA(ADC Offset Calibration Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF<2:0>			VREF<1:0>		ADICS

Bit<7>: CALI-ADC Calibration enable bit for ADC offset

1: Enable Calibration

0: Disable Calibration

Bit<6>: SIGN-ADC Polarity bit of the offset voltage

1: Positive voltage

0: Negative voltage

Bit<5:3>: VOF<2:0>-ADC Offset voltage bits

VOF<2>	VOF<1>	VOF<0>	Range of Calibration
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bit<2:1>: VREF<1:0>- ADC internal reference voltage source

VREF<1>	VREF<0>	
0	0	VDD
0	1	4V
1	0	3V
1	1	2V

Bit<0>: ADICS-ADC input channel selection, see description on RPAGE0-R9.

3.1.10 RPAGE0～RB(Converted Value of ADC Register AD11-AD4)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD<11>	AD<10>	AD<9>	AD<8>	AD<7>	AD<6>	AD<5>	AD<4>

The upper 8 bits of the AD conversion result, when the AD conversion ends, it is automatically loaded, read only

3.1.11 RPAGE0～RC(Converted Value of ADC Register AD11-AD8)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	AD<11>	AD<10>	AD<9>	AD<8>

The upper 4 bits of the AD conversion result, when the AD conversion ends, it is automatically loaded, read-only, where bit<7:4> is fixed to read 0.

3.1.12 RPAGE0～RD(Converted Value of ADC Register AD7-AD0)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD<7>	AD<6>	AD<5>	AD<4>	AD<3>	AD<2>	AD<1>	AD<0>

The lower 8 bits of the AD conversion result, when the AD conversion ends, it is automatically loaded, read only

3.1.13 RPAGE0～RE(Interrupt Status Register 2 and Wake-up Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<7>: LVD_FG- Low voltage Detector state
0: The power supply voltage is lower than the preset voltage detection point
1: The power supply voltage is higher than the preset voltage detection point or the low voltage detection module is not enabled.
Bit<6>: LVDIF- Low voltage detection interrupt flag
1: Low voltage detection interrupt
0: No low voltage detection interrupt
Bit<5>: ADIF-AD Conversion end interrupt flag
1: There is an AD interrupt
0: no AD interrupt
Bit<4>: CMPIF- Comparator Interrupt flag.
1: interrupt request
0: no interrupt occurs
Bit<3>: ADWE-ADC wake-up enable bit
1: Enable ADC wake-up
0: Disable ADC wake-up
When AD Conversion enters sleep/idle mode, this bit must be set to “Enable“.
Bit<2>: CMPWE- Comparator wake-up enable bit
1: Enable Comparator wake-up
0: Disable Comparator wake-up
When the Comparator enters sleep/idle mode, this bit must be set to “Enable”.
Bit<1>: P5ICWE- Port 5 input change to wake-up status enable bit
1: Enable Port 5 input change to wake-up status
0: Disable Port 5 input change to wake-up status
When Port 5 change enters sleep/idle mode, this bit must be set to “Enable”.
Bit<0>: LVDWE-LVD Low Voltage Detect wake-up enable bit
1: Enable Low Voltage Detect wake-up
0: Disable Low Voltage Detect wake-up

3.1.14 RPAGE0～RF(Interrupt Status Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	EXIF	P5ICIF	TCIF

Bit<6>: DT2IF-PWM2 Duty Match Interrupt flag
1: Set when PWM2 Duty Match
0: Reset by software or When the PWM2 duty cycle does not match
Bit<5>: DT1IF-PWM1 Duty Interrupt flag

1: Set when PWM1 Duty Match
0: When the PWM1 duty cycle does not match

Bit<4>: PWM2IF-PWM2 Period Interrupt flag
1: Set when PWM2 period match
0: When the PWM2 period does not match

Bit<3>: PWM1IF-PWM1 Period Interrupt flag
1: Set when PWM1 period match
0: When the PWM1 period does not match

Bit<2>: EXIF External interrupt flag
1: Set by falling edge on /INT pin
0: no interrupt occurs

Bit<1>: P5ICIF-P5 input status change interrupt flag
1: Set when Port 5 input changes
0: no interrupt occurs

Bit<0>: TCIF-TCC overflow interrupt flag
1: when TCC overflows.
0: no interrupt occurs

3.1.15 RPAGE1～R5(Table Point High Register for Instruction)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	0	0	0	TAD<11>	TAD<10>	TAD<9>	TAD<8>

Bit<7>: MLB- Lookup table data selection
1: High eight bits
0: Low eight bits

Bit<6:4>: Readable only, Set to “0” at all time.

Bit<3:0>: TAD<11:8>- The upper four bits of the table lookup instruction address

3.1.16 RPAGE1～R6(Table Point Low Register for Instruction)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAD<7>	TAD<6>	TAD<5>	TAD<4>	TAD<3>	TAD<2>	TAD<1>	TAD<0>

The lower eight bits of the table lookup instruction address

3.1.17 RPAGE1～R7(PWM Enable Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PWMCAS	PWM2E	PWM1E

Bit<7:3>: Not used bits. Read as “0” all the time

Bit<2>: PWMCAS-PWM1 Cascade Mode
1:16-Bit PWM (PWM2 as a high bit)
0:8-Bit PWM

Bit<1>: PWM2E-PWM2 Function control
1: Enable (P51 output)
0: Disable

Bit<0>: PWM1E-PWM1 Function control
1:Enable (P67 output)
0: Disable

3.1.18 RPAGE1～R8(TMR Timer Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2EN	T1EN	T2P<2:0>			T1P<2:0>		

Bit<7>: T2EN-TMR2 function control
1: Enable
0: Disable
Bit<6>: T1EN-TMR1 function control
1: Enable
0: Disable
Bit<5:3>: T2P<2:0>-TMR2 TMR2 clock prescaler option bits

T2P<2>	T2P<1>	T2P<0>	Prescale
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit<2:0>: T1P<2:0>-TMR1 TMR1 clock prescale option bits

T1P<2>	T1P<1>	T1P<0>	Prescale
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.19 RPAGE1～R9(PWM1 Time Period)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1<7>	PRD1<6>	PRD1<5>	PRD1<4>	PRD1<3>	PRD1<2>	PRD1<1>	PRD1<0>

PWM1 Cycle setting register, readable and writable

3.1.20 RPAGE1～RA(PWM2 Time Period)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2<7>	PRD2<6>	PRD2<5>	PRD2<4>	PRD2<3>	PRD2<2>	PRD2<1>	PRD2<0>

PWM2 Cycle setting register, readable and writable

3.1.21 RPAGE1～RB(PWM1 Duty Cycle Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT1<7>	DT1<6>	DT1<5>	DT1<4>	DT1<3>	DT1<2>	DT1<1>	DT1<0>

PWM1 Duty cycle setting register, readable and writable

3.1.22 RPAGE1～RC(PWM2 Duty Cycle Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT2<7>	DT2<6>	DT2<5>	DT2<4>	DT2<3>	DT2<2>	DT2<1>	DT2<0>

PWM2 Duty cycle setting register, readable and writable

3.1.23 RPAGE1～RE(LVD and External Interrupt Control Registers)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD<1:0>		-	-	-	EXWE

Bit<7>: LVDIE-LVD interrupt enable control
1: Enable
0: Disable
Bit<6>: LVDEN-LVD function control
1: Enable
0: Disable
Bit<5:4>: LVD<1:0>-LVD Detection point selection

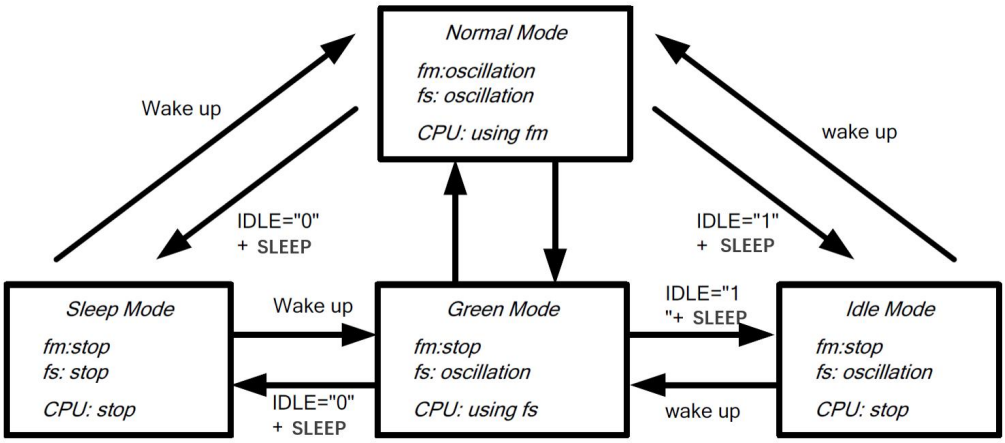
LVD<1>	LVD<0>	LVD Detection point selection
0	0	4.5V
0	1	4.0V
1	0	3.3V
1	1	2.2V

Bit<3:1>: Not used. Set to “0” at all time.
Bit<0>: EXWE-External /INT wake-up enable bit
1: Enable External /INT pin wake-up
0: Disable External /INT pin wake-up (default)

3.1.24 RPAGE1～RF(System Clock and Status Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TIMERSC	CPUS	IDLE	SHS<1:0>		RCM<1:0>	

Bit<6>: TIMERSC-TCC/PWM clock source select.
1: main oscillator
0: sub-oscillator
Bit<5>: CPUS-CPU Oscillator Source Select
1: main oscillator
0: sub-oscillator
Bit<4>: IDLE- System status selection
1: Enter sleep mode after executing SLEEP (CPU+ peripherals are stopped)
0: Wait for mode after executing SLEEP (CPU stops, peripherals do not stop)
is bit will determine as to which mode to activate.
1: IDLE = ‘1’ + SLEP instruction → idle mode
0: IDLE = ‘0’ + SLEP instruction → sleep mode (default)



Bit<3:2>: SHS<1:0>-ADC Sample and hold period selection bit

SHS<1>	SHS<0>	AD Sample and hold cycle
0	0	2TAD
0	1	4TAD
1	0	8TAD
1	1	12TAD

Note: The accuracy, linearity, and speed of successive approximation AD conversion are determined by the characteristics of the ADC and comparator. The sampling resistor directly affects the time required to charge the sample-and-hold capacitor. The application process controls the length of the sampling time to meet the needs of a particular precision.

In general, for every 1K increase in impedance of the sampling resistor, the sampling time is increased by at least 2μs. It is recommended that the maximum resistance of the sampling resistor be 10K.

Bit<1:0>: RCM<1:0>:IRC Frequency selection bit

RCM<1>	RCM<0>	IRC Frequency selection
0	0	1M
0	1	8M
1	0	16M
1	1	4M

3.2 Control Register

3.2.1 CONT (Control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit<7>: INTE: INT signal edge
1: Interrupt occurs at the falling edge of the INT pin
0: Interrupt occurs at the rising edge of the INT pin
Bit<6>:INT: Interrupt Enable flag
1: Enabled by the ENI/RETI instructions
0: Masked by DISI or hardware interrupt
This bit is readable only.
Bit<5>: TS: TCC TCC signal source
1: Select external clock, P54 as TCC signal input port
0: Select internal system clock, P54 as IO port
Bit<4>:TE: External clock trigger edge select control bit
1: Increment if the transition from high to low takes place on the TCC pin
0: Increment if the transition from low to high takes place on the TCC pin
Bit<3>: PSTE: Prescaler enable bit for TCC
1: Prescaler enable bit. TCC rate is set by Bit 2 ~ Bit 0.
0: TCC Prescaler disable bit. TCC rate is 1:1.
Bit<2:0>:PST2～PST0: Prescaler rate selection control bit

PST2	PST1	PST0	TCC Prescaler rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.2.2 IOPAGE0～IOC50～IOC70(I/O Port Control Register)

1:input (default)
0: defines the relative I/O pin as output

3.2.3 IOPAGE0～IOC80(Comparator/Operational Amplifier Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	CMPOUT	COS<1:0>		-	-	-

Bit<7:6>: Not used. Set to "0" all the time
Bit<5>: CMPOUT- Result of the comparator output. This bit is readable only.
1: Non-inverting input voltage > reverse input voltage
0: Non-inverting input voltage < reverse input voltage

Bit<4:3>: COS<1:0>

COS<1>	COS<0>	Function Description
0	0	Comparator and OP are not used. P64, P65, and P66 are normal I/O pin
0	1	CMP enable, P65 and P66 are Comparator input pins and P64 is normal I/O pin
1	0	CMP enable, P65 and P66 are Comparator input pins and P64 is Comparator output pin (CO)
1	1	Used as OP and P64 is OP output pin (CO)

Bit<2:0>: Not used. Set to "0" all the time.

Note: IOC80 register BIT<4:0> is readable and writable, BIT5 is read only.

3.2.4 IOPAGE0～IOC90(TMR1 Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR1<7:0>							

TMR1 register, read only

3.2.5 IOPAGE0～IOCA0(TMR2 Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR2<7:0>							

TMR2 register, read only

3.2.6 IOPAGE0～IOCB0(P5 Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5PD<7>	P5PD<6>	P5PD<5>	P5PD<4>	P5PD<3>	P5PD<2>	P5PD<1>	P5PD<0>

Port5 Pull-down Control

1: Disable(default)

0: Enable

3.2.7 IOPAGE0～IOCC0(P6 Open-drain Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6OD<7>	P6OD<6>	P6OD<5>	P6OD<4>	P6OD<3>	P6OD<2>	P6OD<1>	P6OD<0>

Port6 Open-drain Control

1: Disable(default)

0: Enable

3.2.8 IOPAGE0～IOCD0(P5 Pull-high Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5PH<7>	P5PH<6>	P5PH<5>	P5PH<4>	P5PH<3>	P5PH<2>	P5PH<1>	P5PH<0>

Port5 Pull-high Control

1: Disable(default)

0: Enable

3.2.9 IOPAGE0～IOCE0(WDT Control Register and Interrupt Enable Register 2)

Bit 7	Bit6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<7>: WDTE-WDT function control
1: Enable
0: Disable
Bit<6>: EIS-Control bit used to define the function of the INT pin
1: external interrupt pin
0: bidirectional I/O pin
Bit<5>: ADIE-ADC interrupt enable bit
1: Enable
0: Disable
Bit<4>: CMPIE- CMP interrupt enable bit
1: Enable
0: Disable
Bit<3>: PSWE- Prescaler enable bit for WDT
1: Enable
0: Disable
Bit<2:0>:PSW<2:0>-WDT prescaler select bits

PSW<2>	PSW<1>	PSW<0>	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.2.10 IOPAGE0～IOCF0 (Interrupt Enable Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	P5ICIE	TCIE

Bit<7>: Not used. Set to “0” at all time.
Bit<6>: DT2IE-PWM2 Duty interrupt enable control
1: Enable
0: Disable
Bit<5>: DT1IE-PWM1 Duty interrupt enable control
1: Enable
0: Disable
Bit<4>: PWM2IE-PWM2 Periodic interrupt enable control
1: Enable
0: Disable

Bit<3>: PWM1IE-PWM1 Periodic interrupt enable control
1: Enable
0: Disable
Bit<2>: EXIE- External interrupt enable control
1: Enable
0: Disable
Bit<1>: P5ICIE- P5 Keyboard interrupt enable control
1: Enable
0: Disable(default)
Bit<0>: TCIE-TCC overflow interrupt enable control
1: Enable
0: Disable

3.2.11 IOPAGE1～IOC51(P5 High Sink Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5HS<7>	P5HS<6>	-	P5HS<4>	P5HS<3>	P5HS<2>	P5HS<1>	-

Port5 Output low drive capability selection
1: Enhance (25mA in 0.1VDD)
0: Normal (10mA in 0.1VDD)

3.2.12 IOPAGE1～IOC61(P6 High Sink Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HS<7>	P6HS<6>	P6HS<5>	P6HS<4>	P6HS<3>	P6HS<2>	P6HS<1>	P6HS<0>

Port6 Output low drive capability selection
1: Enhance (25mA in 0.1VDD)
0: Normal (10mA in 0.1VDD)

3.2.13 IOPAGE1～IOC71(P5 High Driver Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5HD<7>	P5HD<6>	-	P5HD<4>	P5HD<3>	P5HD<2>	P5HD<1>	-

Port5 Output High drive capability selection
1: Enhance (10mA in 0.9VDD)
0: Normal (3.5mA in 0.9VDD)

3.2.14 IOPAGE1～IOC81(P6 High Driver Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HD<7>	P6HD<6>	P6HD<5>	P6HD<4>	P6HD<3>	P6HD<2>	P6HD<1>	P6HD<0>

Port6 Output High drive capability selection
1: Enhance (10mA in 0.9VDD)
0: Normal (3.5mA in 0.9VDD)

3.2.15 IOPAGE1～IOCF1(P6 Pull-high Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PH<7>	P6PH<6>	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>

Port6 Pull-high enable control bit
1: Disable (default)

0：Enable

3.3 GPIO Function Module

JZ8P2603 has three sets of bidirectional I/O ports, a total of 18 inputs and 18 outputs, most of which can be reused for other functions.

16 programmable pull-high I/O pins：P5.0-P5.7, P6.0-P6.7;

8 programmable pull-down I/O pins：P5.0-P5.7;

14 programmable driver enhanced I/O pins：P5.1-P5.4, P5.6-P5.7, P6.0-P6.7;

8 programmable open-drain I/O pins：P6.0-P6.7;

3.3.1 GPIO Register Description

RPAGE0～R5 (PORT5 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P57	P56	P55	P54	P53	P52	P51	P50

Port input/output register, P5 port 8 bits

P5 is a readable and writable register

RPAGE0～R6 (PORT6 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

Port input/output register, P5 port 8 bits

P6 is a readable and writable register

RPAGE0～R7 (PORT7 Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	P71	P70

Port input/output register, P7 port 2 bits

P7 is a readable and writable register

IOPAGE0～IOC50(P5 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5CR<7>	P5CR<6>	P5CR<5>	P5CR<4>	P5CR<3>	P5CR<2>	P5CR<1>	P5CR<0>

Port5 Direction Control bits

1：input（default）

0：output

IOPAGE0～IOC60(P6 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6CR<7>	P6CR<6>	P6CR<5>	P6CR<4>	P6CR<3>	P6CR<2>	P6CR<1>	P6CR<0>

Port6 Direction Control bits

1：input（default）

0：output

IOPAGE0～IOC70(P7 Direction Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	P7CR<1>	P7CR<0>

Bit<1:0>：Port7 Direction Control bits

1：input（default）

0：output

IOPAGE0～IOCB0(P5 Pull-down Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5PD<7>	P5PD<6>	P5PD<5>	P5PD<4>	P5PD<3>	P5PD<2>	P5PD<1>	P5PD<0>

Port5 pull-down control

1：Disable（default）

0：Enable

IOPAGE0～IOCC0(P6 Open-drain Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6OD<7>	P6OD<6>	P6OD<5>	P6OD<4>	P6OD<3>	P6OD<2>	P6OD<1>	P6OD<0>

Port6 Open-drain control

1：Disable（default）

0：Enable

IOPAGE0～IOCD0(P5 Pull-high Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5PH<7>	P5PH<6>	P5PH<5>	P5PH<4>	P5PH<3>	P5PH<2>	P5PH<1>	P5PH<0>

Port5 Pull-high control

1：Disable（default）

0：Enable

IOPAGE1～IOC51(P5 High Sink Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5HS<7>	P5HS<6>	P5HS<5>	P5HS<4>	P5HS<3>	P5HS<2>	P5HS<1>	P5HS<0>

Port5 Output low drive capability selection

1：Enhance（25mA in 0.1VDD）

0：Normal（10mA in 0.1VDD）

IOPAGE1～IOC61(P6 High Sink Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HS<7>	P6HS<6>	P6HS<5>	P6HS<4>	P6HS<3>	P6HS<2>	P6HS<1>	P6HS<0>

Port5 Output low drive capability selection

1：Enhance（25mA in 0.1VDD）

0：Normal（10mA in 0.1VDD）

IOPAGE1～IOC71(P5 High Driver Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P5HD<7>	P5HD<6>	P5HD<5>	P5HD<4>	P5HD<3>	P5HD<2>	P5HD<1>	P5HD<0>

Port5 Output High drive capability selection

1：Enhance（10mA in 0.9VDD）

0：Normal（3.5mA in 0.9VDD）

IOPAGE1～IOC81(P6 High Driver Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6HD<7>	P6HD<6>	P6HD<5>	P6HD<4>	P6HD<3>	P6HD<2>	P6HD<1>	P6HD<0>

Port6 Output High drive capability selection

1：Enhance（10mA in 0.9VDD）

0：Normal（3.5mA in 0.9VDD）

IOPAGE1～IOCF1(P6 Pull-high Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6PH<7>	P6PH<6>	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>

Port6 Pull-high enable control bita

1：Disable（default）

0：Enable

3.4 TCC Timer Function Module

TCC (R1) is an 8-Bit count-up counter that works as long as it has a clock. Clock source can be either internal system clock (rising edge triggering), or external clock (input by TCC pin, triggering edge optional). If there is no frequency division control, each clock (Fm/Fs) cycle (select internal clock) or each external clock cycle (external clock) can be added to the counter by 1.

The system provides an 8-Bit counter as the prescaler of TCC. TCC prescaler, trigger edge and clock can be set by CONT register.

TCC count overflow can form interrupt signal.

In IDLE mode, TCC interruption can wake up the circuit.

3.4.1 TCC Timer Register Description

RPAGE0～R1 (TCC Timing Counter)

TCC is an 8Bit count-up counter. Clock source can choose internal clock/external clock. Counting overflow can cause interruption and TCC can be read and written.

TCC can be triggered by signal edge or instruction cycle on EXINT pin to generate plus 1 operation (CONT.4-bit definition). If the PAB bit is cleared (CONT.3), a prescaler is assigned to the TCC. When the TCC register is written to a value, the value of the prescaler is cleared to zero.

CONT (Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit<6>:INT: Interrupt enable flag
1: Masked by DISI instructions or hardware interrupts
0: Enabled by ENI or RETI instructions

Bit<5>:TS: TCC Clock Source Selection Control Bit
1: Select external clock (P54 as TCC port at this time)
0: Select internal system clock

Bit<4>:TE: External clock triggers along selected control bits
1: Select the falling edge of the external clock as the trigger edge
0: Select the rising edge of the external clock as the trigger edge

Bit < 3>: PSTE: Predivider Selection Control Bit
1: TCC prescaler enable
0: TCC prescaler disable

Bit<2:0>: PST2-PST0: Selection Control Bit for prescaler rate

PST2	PST1	PST0	TCC prescaler rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128

1	1	1	1:256

RPAGE0～RF(Interrupt flag 1 register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	EXIF	P5ICIF	TCIF

Bit<0>: TCIF-TCCInterrupt flag bit

1: Interruption

0: No interruption

IOPAGE0～IOCF0(Interrupt enable 1 control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	P5ICIE	TCIE

Bit<0>: TCIE-TCC Overflow interrupt enabling control

1: Enable

0: Disable

RPAGE1～RF(System Clock and State Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB_EN	TIMERSC	CPUS	IDLE	SHS<1:0>		RCM<1:0>	

Bit<6>: TIMERSC-TCC/PWM Clock Source Selection

1: main oscillator

0: sub-oscillator

3.4.2 TCC Timing Setup Instructions

1. Assign initial values to TCC registers;
2. Set the value of the CONT register (select as a timer or counter and pre-divider ratio);
3. As a counter, it is necessary to select positive or negative edge plus 1 for TCC external irrigation signal in CONT register.;
4. If interrupt function is needed, TCIE (Bit0) in IOCF0 register should be set to 1, and ENI instruction should be executed.
5. The interrupt program will automatically save ACC, STATUS and R4 in the stack. After executing RETI instructions, the interrupt program will be poped from the stack. Before exiting the interrupt, the TCC interrupt flag should be clear.

3.5 WDT Watchdog Function Module

WDT is a 12-Bit count-up counter with two enabling control signals (ENWDT in OPTION and WDTE control bit in IOCE register). The counting clock is provided by a separate oscillator, so the WDT can still run (if enabled) after the system enters the sleep mode. In normal mode or sleep mode, the overflow of WDT can reset the system, and the reset time is selected by the control bit WDTPS in OPTION for 4.5ms or 18ms.

The system provides an 8-Bit counter as a prescaler for WDT, which is set by IOCE0 registers.

Whether in simulation or in burning, in order to enable WDT function, it is necessary to select Enable at the WDT bit of Code Option register, and then select "1" at the WDTE bit of WDT control register. Two conditions are indispensable. The counting frequency of watchdog timer (WDT) comes from the internal RC oscillator. The counting frequency is about 15 kHz (+30%). When MCU enters Sleep mode or Idle mode, because the power supply to RC oscillator is not turned off, WDT is still counting. When WDT overflows, MCU will be awakened and reset.

3.5.1 WDT Watchdog Register Description

IOPAGE0～IOCE0(WDT Control and interrupt enable 2 control registers)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<7>: WDTE-WDT function control.

1: Enable

0: Disable

Bit<3>: PSWE- Watchdog Clock prescaler Control

1: Enable

0: Disable

Bit<2:0>:PSW<2:0>- Watchdog Clock prescaler Control

PSW<2>	PSW<1>	PSW<0>	Prescaler rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.5.2 WDT Watchdog Setting Instructions

1. Set Bit7 (WDTE) bit in IOCE0 register and choose whether to use WDT or not.
2. Setting prescaler rate by setting Bit2-Bit0 bits of IOCE0 register;
3. If WDT wake-up is enabled, it is recommended that customers prohibit other wake-up. Reasons: WDT wake-up and other wake-up enablers, when the application of WDT function wakes up at the same time, IC will give priority to reset, not to implement other

wake-up procedures, so if enabling WDT wake-up, it is recommended that customers prohibit other wake-up.

3.6 Port State Change Wake-up Function Module

After executing SLEEP instructions, the system enters sleep mode (IDLE = 0), the system clock stops, all modules stop working, except WDT (if enabled). If SLEEP is executed during AD conversion, the system clock, TCC, TMR1, TMR2, TMR3, WDT (if enabled) will continue to run.

3.6.1 Description of sleep wake-up mode

RESET pin input low level;
WDT reset;
Port input status changes;
Change of comparator status;
AD conversion is completed.
LVD low voltage detection;
External interrupt pin wake-up;

The first two wakeups cause the system to reset once, thus terminating all programs executed before sleep.

The last five wake-up modes maintain the continuity of the program, and can continue the original process (DISI before SLEEP) or perform the corresponding jump (ENI before SLEEP), and open the corresponding enabling control bit, jump to the position of the interrupt vector. Mainly describes the port change wake-up, other wake-up methods will be explained in the corresponding module.

3.6.2 Port status change wake-up register description

RPAGE0～RE(Interrupt flag 2 and wake-up enable 1 register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<1>: P5ICWE-P5 Port status change wake-up enablement
1: Enable
0: Disable

RPAGE0～RF(Interrupt flag 1 register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	EXIF	P5ICIF	TCIF

Bit<1>: P5ICIF-P5 Port status change interrupt flag bit
1: interrupt request
0: no interrupt occurs

IOPAGE0～IOCF0(Interrupt enable 1 control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	P5ICIE	TCIE

Bit<1>: P5ICIE-P5 Port status change interrupt enablement
1: Enable
0: Disable (default)

3.6.3 Port State Change Query Mode Wake-up Settings

1. PORT port wake-up port is set as input;
2. The internal pull-up or pull-down of the wake-up port can be selected according to the need.
3. Enabling port state change independent interrupt and wake-up control;
4. Set the ICWE bit of register RE as 1 enable wake-up function.
5. Execute DISI instructions and do not enter the interrupt address port.
6. Read PORT ports (e.g. MOV 0X05, 0X05);
7. Execute the "SLEP" instruction and enter the sleep (IDLE = 0) / idle (IDLE = 1) mode.
8. After waking up, execute the next instruction of SLEP.

3.6.4 Port status change interrupt wake-up settings

1. PORT port wake-up port is set as input;
2. The internal pull-up and pull-down of the wake-up port can be selected according to the need.
3. The setting of WDT pre-frequency division must be greater than 1:1, prohibiting WDT;
4. Enabling port state change independent interrupt and wake-up control;
4. Set the ICWE bit of register RE to 1 to enable wake-up function.
5. Enabling PORT port status change interrupt;
6. Execute "ENI" instructions and wait to enter the interrupt address port.
7. Read PORT ports (e.g. MOV 0X05, 0X05);
8. Instruct "SLEP" and enter the sleep (IDLE = 0) / idle (IDLE = 1) mode.
9. After waking up, it will enter the interrupt address port. After exiting the interrupt, it will execute the next instruction of SLEP.

3.7 LVD Low Voltage Detection Function Module

JZ8P2603 has the function of low voltage detection (LVD). A total of four voltage values can be selected programmably. When the working voltage of CPU drops to a set value, the CPU interrupts immediately by setting the interrupt flag bit (if the LVD is enabled), and the Bit6 bit of BANK0-RE register is set at 1. When the working voltage of CPU rises from below the set value to above the set value, the MCU will reset the interrupt flag again (if enabled), and Bit7 bit of BANK1 RE register is set to 1.

3.7.1 LVD Voltage Detection Register Description

RPAGE0～RE(Interrupt flag 2 and wake-up enable 1 register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<7>: LVD_FG-Low Voltage Detection Flag bit

0: The power supply voltage is lower than the preset voltage detection point.

1: The power supply voltage is higher than the preset voltage detection point or the low voltage detection module is not enabled.

Bit < 6>: LVDIF-Low Voltage Detection Interruption Flag bit

1: Interruption of Low Voltage Detection

0: No Low Voltage Detection Interruption

Bit<0>: LVDWE-LVD Wake-up Enable bit

1: Enable

0: Disable

RPAGE1～RE(LVD and External Interrupt Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD<1:0>		-	-	-	EXWE

Bit<7>: LVDIE-LVD Interrupt control

1: Enable

0: Disable

Bit<6>: LVDEN-LVD Function control

1: Enable

0: Disable

Bit<5:4>: LVD<1:0>-LVD Detection Point Selection

LVD<1>	LVD<0>	LVD Detection Point Selection
0	0	4.5V
0	1	4.0V
1	0	3.3V
1	1	2.2V

3.7.2 LVD Description for Voltage Detection Settings

1. Set the voltage value of LVD (LVD 1 and LVD0 bits of BANK1 RE register);
2. Enabling LVD function (BANK1 RE register LVDEN bit);

3. Enabling LVD interrupt (LVDIE bit of BANK1 RE register) and executing "ENI" instruction (if LVD interrupt is needed);
4. After the interrupt subroutine or main program queries LVDIF bit 1, the LVD_FG bit of RPAGE0 RE register is judged and the corresponding action is performed.

3.8 ADC A/D Conversion Function Module

JZ8P2603 has 8 input channels (P50-P53, P55, P57, P67, P70) and 12-bit resolution. If the AD interrupt function is enabled, an interrupt will be generated when the AD conversion is completed. If the AD interrupt is not enabled, the user needs to query the ADRUN bit of RPAGE0~R9. If this bit has been cleared, the AD conversion is complete.

If the AD wake-up function is enabled, the completion of the AD conversion can wake the CPU from sleep mode.

AD sampling time calculation method:

Starting with setting ADRUN = 1, the time to complete one AD sampling = **ADC sampling and holding period + AD conversion time**

AD conversion time:

One bit of AD conversion takes a TAD time. We have a total of 12 bits of AD. So the conversion time is 12 TADs.

3.8.1 ADC A/D Conversion Register Description

RPAGE0～R8(AD Channel enable register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE<7>	ADE<6>	ADE<5>	ADE<4>	ADE<3>	ADE<2>	ADE<1>	ADE<0>

Bit<7:0>:ADE<7:0>-AD Channel enable control bit

1：Enable

0：Disable

Channel NUM	Enable control	Pin
AD0	ADE<0>	P50
AD1	ADE<1>	P51
AD2	ADE<2>	P52
AD3	ADE<3>	P53
AD4	ADE<4>	P67
AD5	ADE<5>	P70
AD6	ADE<6>	P55
AD7	ADE<7>	P57

AD Channel enable register is readable and writable

RPAGE0～R9(ADC Control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR<1:0>		ADRUN	ADPD	ADIS<2:0>		

Bit<7>：VREFS-ADC the input source of Vref of the ADC

1：External reference (from P54 input voltage as ADC reference voltage)

0：Internal reference

Bit<6:5>:CKR<1:0>（ADC Clock Rate Select，Set the value of the minimum time of unit TAD）

CPUS	CKR<1>	CKR<0>	ADC Clock
1	0	0	Fosc/16

1	0	1	Fosc/4
1	1	0	Fosc/64
1	1	1	Fosc/1
0	x	x	Fosc/1

Bit<4>: ADRUN-ADC ADC starts to RUN

1: an A/D conversion is started. This bit can be set by software

0: on completion of the conversion Reset by hardware. This bit cannot be reset through software (default))

Bit<3>: ADPD-ADC ADC Power

1: Enable

0: Disable

Bit<2:0>: ADIS<2:0>-ADC Analog Input Select

ADICS	ADIS<2>	ADIS<1>	ADIS<0>	Analog Input Select
0	0	0	0	P50
0	0	0	1	P51
0	0	1	0	P52
0	0	1	1	P53
0	1	0	0	P67
0	1	0	1	P70
0	1	1	0	P55
0	1	1	1	P57
1	0	0	0	OPOUT
1	1	0	0	0.25*VDD

Note: Fosc represents the oscillator clock. For example, if IRC is selected for 4M, Fosc=4M.

For example: Fosc=4M, TAD is set to Fosc/4, then TAD=1uS

RPAGE0～RA(ADC Offset Calibration Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF<2:0>			VREF<1:0>		ADICS

Bit<7>: CALI-ADC Calibration enable bit for ADC offset

1: Enable Calibration

0: Disable Calibration

Bit<6>: SIGN-ADC Polarity bit of the offset voltage

1: Positive voltage

0: Negative voltage

Bit<5:3>: VOF<2:0>-ADC Offset voltage bits

VOF<2>	VOF<1>	VOF<0>	Range of Calibration
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB

1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

Bit<2:1>: VREF<1:0>-ADC internal reference voltage source

VREF<1>	VREF<0>	
0	0	VDD
0	1	4V
1	0	3V
1	1	2V

Bit<0>: ADICS-ADC input channel selection, see description on RPAGE0-R9.

RPAGE0～RB(Converted Value of ADC Register AD11-AD4)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD<11>	AD<10>	AD<9>	AD<8>	AD<7>	AD<6>	AD<5>	AD<4>

The upper 8 bits of the AD conversion result, when the AD conversion ends, it is automatically loaded, read only

RPAGE0～RC(Converted Value of ADC Register AD11-AD8)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

The upper 4 bits of the AD conversion result, when the AD conversion ends, it is automatically loaded, read-only, where bit<7:4> is fixed to read 0.

RPAGE0～RD(Converted Value of ADC Register AD7-AD0)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

The lower 8 bits of the AD conversion result, when the AD conversion ends, it is automatically loaded, read only

RPAGE0～RE(Interrupt Status Register 2 and Wake-up Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<5>: ADIF-AD Conversion end interrupt flag

1: There is an AD interrupt

0: no AD interrupt

Bit<3>: ADWE-ADC wake-up enable bit

1: Enable ADC wake-up

0: Disable ADC wake-up

RPAGE1～RF(System Clock and Status Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Db_en	TIMERSC	CPUS	IDLE	SHS<1:0>		RCM<1:0>	

Bit<3:2>: SHS<1:0>-ADC Sample and hold period selection bit

SHS<1>	SHS<0>	AD Sample and hold cycle
0	0	2TAD
0	1	4TAD
1	0	8TAD

1	1	12TAD

Note: The accuracy, linearity, and speed of successive approximation AD conversion are determined by the characteristics of the ADC and comparator. The sampling resistor directly affects the time required to charge the sample-and-hold capacitor. The application process controls the length of the sampling time to meet the needs of a particular precision.

In general, for every 1K increase in impedance of the sampling resistor, the sampling time is increased by at least 2μs. It is recommended that the maximum resistance of the sampling resistor be 10K.

IOPAGE0～IOCE0(WDT Control Register and Interrupt Enable Register 2)

Bit 7	Bit6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<5>: ADIE-ADC interrupt enable bit

1: Enable

0: Disable

3.8.2 ADC setting instructions

1. Set ADE7-ADE0 of register RPAGE0~R8 to enable analog input channel;
2. Set the register RPAGE0～R9 to select the AD input channel; set the CKR1-CKR0 of the RPAGE0～R9 register to select the clock prescaler of the ADC and the reference voltage of the ADC; set "ADPD=1" to start supplying voltage to AD;
3. Call the AD precision correction subroutine;
4. If you need to use the interrupt function, set ADIE=1 and execute the "ENI" instruction;
5. can enable the AD wake-up function as needed, set ADWE=1;
6. Set "ADRUN=1" to start AD conversion;
7. can choose IDLE / SLEEP mode as needed;
8. Wait for interrupt or ADRUN is cleared to 0; if AD interrupt occurs, clear ADIF to "0" when leaving the interrupt program;
9. Save the results of the conversion. If you need to do multiple AD conversions, skip to step 5.

3.8.3 ADC accuracy adjustment instructions

1. Set ADE7-ADE0 of register RPAGE0~R8 to enable analog input channel;
2. Set the register RPAGE0～R9 to select the AD input channel; set the CKR1-CKR0 of the RPAGE0～R9 register;
3. Select the clock prescaler of the ADC; select the reference voltage of the ADC; set "ADPD=1" to start supplying voltage to AD;
4. set the RPAGE0～RA to 0XF8, enable the ADC correction bit function, set "ADRUN=1" to start AD conversion;
5. Firstly, correct the positive voltage of ADC bit, then correct the ADC level negative voltage, and correct the 2LSB voltage each time;
6. When the AD value is detected as "0", the AD precision correction is ended, that is, set the "CALI" bit of the ADC to "0".

3.9 PWM Pulse width modulation function module

JZ8P2603 has two counters with prescaler to generate pulse width modulation signals. PWM1 and PWM2 are 8Bit (the combination of the them can be configured as 16Bit). In addition, JZ8P2603 has PWM complementary output, dead zone protection and frequency multiplication functions.

3.9.1 PWM Pulse Width Modulation Register Description

RPAGE0～RF(Interrupt Status Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	EXIF	P5ICIF	TCIF

Bit<6>: DT2IF-PWM2 Duty Match Interrupt flag
1: Set when PWM2 Duty Match
0: Reset by software or When the PWM2 duty cycle does not match
Bit<5>: DT1IF-PWM1 Duty Interrupt flag
1: Set when PWM1 Duty Match
0: When the PWM1 duty cycle does not match
Bit<4>: PWM2IF-PWM2 Period Interrupt flag
1: Set when PWM2 period match
0: When the PWM2 period does not match
Bit<3>: PWM1IF-PWM1 Period Interrupt flag
1: Set when PWM1 period match
0: When the PWM1 period does not match

RPAGE1～R7(PWM enable control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PWMCAS	PWM2E	PWM1E

Bit<2>: PWMCAS-PWM1 Cascade Mode
1: 16-Bit PWM (PWM2 as a high bit)
0: 8-Bit PWM
Bit<1>: PWM2E-PWM2 Function control
1: Enable (P51 output)
0: Disable
Bit<0>: PWM1E-PWM1 Function control
1: Enable (P67 output)
0: Disable

RPAGE1～R8(TMR Timer Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2EN	T1EN	T2P<2:0>			T1P<2:0>		

Bit<7>: T2EN-TMR2 function control
1: Enable
0: Disable
Bit<6>: T1EN-TMR1 function control
1: Enable
0: Disable

Bit<5:3>: T2P<2:0>-TMR2 TMR2 clock prescaler option bits

T2P<2>	T2P<1>	T2P<0>	Prescale
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit<2:0>: T1P<2:0>-TMR1 TMR1 clock prescale option bits

T1P<2>	T1P<1>	T1P<0>	Prescale
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

RPAGE1～R9(PWM1 Time Period)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD1<7>	PRD1<6>	PRD1<5>	PRD1<4>	PRD1<3>	PRD1<2>	PRD1<1>	PRD1<0>

PWM1 Cycle setting register, readable and writable

RPAGE1～RA(PWM2 Time Period)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD2<7>	PRD2<6>	PRD2<5>	PRD2<4>	PRD2<3>	PRD2<2>	PRD2<1>	PRD2<0>

PWM2 Cycle setting register, readable and writable

RPAGE1～RB(PWM1 Duty Cycle Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT1<7>	DT1<6>	DT1<5>	DT1<4>	DT1<3>	DT1<2>	DT1<1>	DT1<0>

PWM1 Duty cycle setting register, readable and writable

RPAGE1～RC(PWM2 Duty Cycle Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT2<7>	DT2<6>	DT2<5>	DT2<4>	DT2<3>	DT2<2>	DT2<1>	DT2<0>

PWM2 Duty cycle setting register, readable and writable

RPAGE1～RF(System Clock and Status Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB_EN	TIMERSC	CPUS	IDLE	SHS<1:0>		RCM<1:0>	

Bit<6>: TIMERSC-TCC/PWM clock source select.

1: main-oscillator
0: sub-oscillator

IOPAGE0～IOC90(TMR1 Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR1<7:0>							

TMR1 register, read only

IOPAGE0～IOCA0(TMR2 Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR2<7:0>							

IOPAGE0～IOCF0(Interrupt enable 1 control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	P5ICIE	TCIE

Bit<6>: DT2IE-PWM2 Duty interrupt enable control
1: Enable
0: Disable
Bit<5>: DT1IE-PWM1 Duty interrupt enable control
1: Enable
0: Disable
Bit<4>: PWM2IE-PWM2 Period interrupt enable control
1: Enable
0: Disable
Bit<3>: PWM1IE-PWM1 Period interrupt enable control
1: Enable
0: Disable

3.9.2 PWM Pulse width modulation setting instructions

1. Set the RPAGE1～R7 and RPAGE1～R7 registers to select the corresponding timer as PWM mode, the timer division ratio, the timer interrupt type (if the PWM interrupt is enabled) and the clock source of the timer, etc.
2. Write the value of the RPAGE1～R9 and RPAGE1～RA register to determine the Period of the PWM channel;
3. Write the value of the RPAGE1～RB and RPAGE1～RC register to determine the Duty of the PWM channel;
4. Enable the corresponding timer;
5. Enable or disable the timer interrupt corresponding to the PWM and execute the “ENI” or “DISI” instruction (if required).

3.10 CMP/OP Functional Module

The JZ8P2603 has a set of operational amplifier/comparator. The function of the op amp is suitable for small signal amplification. The comparator can be used as an interrupt source and can also wake up the MCU from sleep/idle state.

3.10.1 CMP/OP Register description

IOPAGE0～IOC80(Comparator/Operational Amplifier Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	CMPOUT	COS<1:0>		0	0	0

Bit<7:6>: Not used. Set to "0" all the time

Bit<5>: CMPOUT- Result of the comparator output. This bit is readable only.

1: Non-inverting input voltage > reverse input voltage

0: Non-inverting input voltage < reverse input voltage

Bit<4:3>: COS<1:0>

COS<1>	COS<0>	Function Description
0	0	Comparator and OP are not used. P64, P65, and P66 are normal I/O pin
0	1	CMP enable, P65 and P66 are Comparator input pins and P64 is normal I/O pin
1	0	CMP enable, P65 and P66 are Comparator input pins and P64 is Comparator output pin (CO)
1	1	Used as OP and P64 is OP output pin (CO)

Bit<2:0>: Not used. Set to "0" all the time.

IOPAGE0～IOCE0(WDT Control Register and Interrupt Enable Register 2)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<4>: CMPIE- CMP interrupt enable bit

1: Enable

0: Disable

RPAGE0～RE(Interrupt flag 2 and wake-up enable 1 register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<4>: CMPIF- Comparator Interrupt flag.

1: interrupt request

0: no interrupt occurs

Bit<2>: CMPWE- Comparator wake-up enable bit

1: Enable Comparator wake-up

0: Disable Comparator wake-up

3.10.2 CMP Comparator settings description

1. Set CIN+ and CIN- as input ports and CO as output port;
2. Set COS1/COS0 of the IOC80 register to 0/1 or 1/0 for use as a comparator;
3. If necessary, enable the comparator interrupt function, execute the "ENI" instruction, and enter the interrupt address;
4. The wake-up function can also be enabled as needed.

Precautions:

1. Comparator wake-up and interrupt are enabled. If the comparator output status changes, the program wakes up from sleep mode, executes the interrupt routine, and then runs the next statement of "SLEP".
2. The offset voltage of the comparator is 10mV.

3.10.3 OP Operational amplifier setup instructions

1. Set CIN+ and CIN- as input ports and CO as output port;
2. Set COS1/COS0 of the IOC80 register to 1/1 and use it as an operational amplifier.

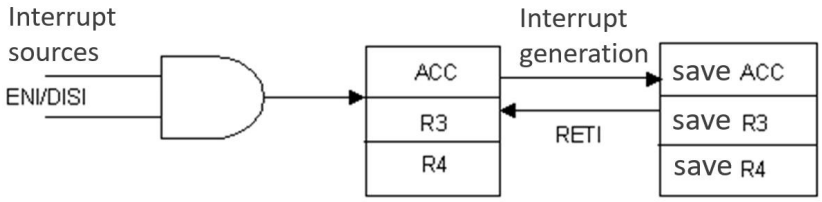
3.11 Interrupt Function Module

The JZ8P2603 has 10 interrupt sources. Regardless of which interrupt is used, the total interrupt must be enabled, that is, the "ENI" instruction is executed. The following are the characteristics of each interrupt, the interrupt address and the priority level:

	interrupt sources	Enable condition	Interrupt flag	Interrupt vector	priority
external	External Interrupt	ENI + EXIE=1	EXIF	003H	2
external	Port input status change	ENI + ICIE=1	ICIF	006H	3
internal	TCC overflow interrupt	ENI + TCIE=1	TCIF	009H	4
internal	Interrupt of AD conversion end	ENI + ADIE=1	ADIF	00CH	5
internal	Comparator interrupt	ENI + CMPIE=1	CMPIF	00FH	6
internal	PWM1 cycle overflow interrupt	ENI + HPWTIE =1	HPWTIF	012H	7
internal	PWM2 cycle overflow interrupt	ENI + LPWTIE =1	LPWTIF	015H	8
internal	PWM1 duty cycle overflow interrupt	ENI+TCCAIE=1	TCCAIF	018H	9
internal	PWM2 duty cycle overflow interrupt	ENI+TCCBIE=1	TCCBIF	01BH	10
internal	Low voltage detection interrupt	ENI+LVDIE=1	LVDIF	021H	1

The RE and RF of BANK0 are interrupt status flag registers that record the interrupt flag bits when an interrupt generates an interrupt request. IOCE0 and IOCF0 are interrupt setting registers. The enable and disable of interrupts are set in these two registers. Bank1 RE is the control register of LVD. The enable and disable of LVD interrupts are set by this register. The total interrupt is enabled by executing the "ENI" instruction. Conversely, the total interrupt is disabled by the "DISI" instruction. When an interrupt is generated, its next instruction will be executed from their specific address. The corresponding interrupt flag must be cleared before leaving the interrupt service routine to avoid interrupted malfunctions.

When the interrupt subroutine is executed, the contents of ACC, R3, and R4 will be saved until the saved subroutine is loaded, and the saved values will be loaded into ACC, R3, and R4. This is to avoid changing the values of ACC, R3, and R4 when the interrupt subroutine is executed, resulting in an error when returning to the main program. As shown below:



3.11.1 Interrupt register description

RPAGE0～RE(Interrupt Flag 2 and Wake Enable 1 Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVD_FG	LVDIF	ADIF	CMPIF	ADWE	CMPWE	P5ICWE	LVDWE

Bit<6>: LVDIF- Low voltage detection interrupt flag
1: Low voltage detection interrupt
0: No low voltage detection interrupt
Bit<5>: ADIF-AD Conversion end interrupt flag
1: There is an AD interrupt
0: no AD interrupt
Bit<4>: CMPIF- Comparator Interrupt flag.
1: interrupt request
0: no interrupt occurs
Bit<3>: ADWE-ADC wake-up enable bit
1: Enable ADC wake-up
0: Disable ADC wake-up

RPAGE0～RF(Interrupt flag 1 register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IF	DT1IF	PWM2IF	PWM1IF	EXIF	P5ICIF	TCIF

Bit<6>: DT2IF-PWM2 Duty Match Interrupt flag
1: Set when PWM2 Duty Match
0: Reset by software or When the PWM2 duty cycle does not match
Bit<5>: DT1IF-PWM1 Duty Interrupt flag
1: Set when PWM1 Duty Match
0: When the PWM1 duty cycle does not match
Bit<4>: PWM2IF-PWM2 Period Interrupt flag
1: Set when PWM2 period match
0: When the PWM2 period does not match
Bit<3>: PWM1IF-PWM1 Period Interrupt flag
1: Set when PWM1 period match
0: When the PWM1 period does not match
Bit<2>: EXIF External interrupt flag
1: Set by falling edge on /INT pin
0: no interrupt occurs
Bit<1>: P5ICIF-P5 input status change interrupt flag

1: Set when Port 5 input changes
0: no interrupt occurs

Bit<0>: TCIF-TCC overflow interrupt flag
1: when TCC overflows.
0: no interrupt occurs

RPAGE1～RE(LVD and External Interrupt Control Registers)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	LVDEN	LVD<1:0>		-	-	-	EXWE

Bit<7>: LVDIE-LVD interrupt enable control
1: Enable
0: Disable

IOPAGE0～IOCE0(WDT Control Register and Interrupt Enable Register 2)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	ADIE	CMPIE	PSWE	PSW<2:0>		

Bit<6>: EIS-Control bit used to define the function of the INT pin
1: external interrupt pin
0: bidirectional I/O pin

Bit<5>: ADIE-ADC interrupt enable bit
1: Enable
0: Disable

Bit<4>: CMPIE- CMP interrupt enable bit
1: Enable
0: Disable

IOPAGE0～IOCF0(Interrupt Enable Register 1)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	DT2IE	DT1IE	PWM2IE	PWM1IE	EXIE	P5ICIE	TCIE

Bit<6>: DT2IE-PWM2 Duty interrupt enable control
1: Enable
0: Disable

Bit<5>: DT1IE-PWM1 Duty interrupt enable control
1: Enable
0: Disable

Bit<4>: PWM2IE-PWM2 Periodic interrupt enable control
1: Enable
0: Disable

Bit<3>: PWM1IE-PWM1 Periodic interrupt enable control
1: Enable
0: Disable

Bit<2>: EXIE- External interrupt enable control
1: Enable
0: Disable

Bit<1>: P5ICIE- P5 Keyboard interrupt enable control
1: Enable

0：Disable(default)

Bit<0>：TCIE-TCC overflow interrupt enable control

1：Enable

0：Disable

3.12 Reset function module

3.12.1 Reset function overview

JZ8P2603 system provides 4 reset modes

1, power-on reset

2. RESET pin input low level reset

3, WDT overflow reset

4, LVR low voltage reset

The first reset time is determined by the SUT in OPTION, as shown in the following table:

Power-on reset setup time:

SUT	Reset setup time
1	18ms
0	4.5ms

When any of the above resets occur, all system registers are restored to their default state, the program stops running, and the program counter PC is cleared. After the reset is complete, the system restarts from vector 0000H.

Any kind of reset situation requires a certain response time, and the system provides a complete reset process to ensure the smooth operation of the reset action. For different types of oscillators, the time required to complete the reset is different. Therefore, the rising speed of VDD and the start-up time of different crystals are not fixed. The RC oscillator has the shortest start-up time and the crystal oscillator has a longer start-up time. In the process of using the user terminal, the requirements of the host for the power-on reset time should be considered.

3.12.2 Power-on reset

Power-on reset is closely related to LVR operation. The process of powering on the system is in the form of a gradually rising curve, which takes a certain amount of time to reach the normal level.

Power-on: The system detects that the power supply voltage has risen and waits for it to stabilize;

External Reset (External Reset Pin Enable Only): The system detects the status of the external reset pin. If not high level, the system remains in reset until the external reset pin is released;

System initialization: all system registers are set to initial values;

The oscillator starts working: the oscillator starts to provide the system clock;

Execution procedure: At the end of power-on, the program starts running.

3.12.3 WDT reset

The watchdog reset is a protection setting for the system. In the normal state, the watchdog timer is cleared by the program. If an error occurs, the system is in an unknown state and the watchdog timer overflows and the system is reset. After the WTD reset, the system restarts to the normal state.

Watchdog timer status: The system detects if the watchdog timer overflows. If it overflows, the system resets.

System initialization: all system registers are set to the default state;

The oscillator starts working: the oscillator starts to provide the system clock;

Execution procedure: At the end of power-on, the program starts running.

Watchdog Timer Application Notes:

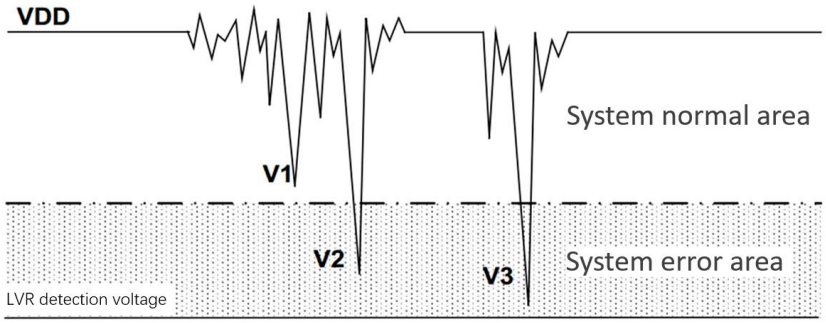
Checking the status of the I/O port and the contents of the RAM before the watchdog is cleared which can improve the reliability of the program before the watchdog is cleared.

The watchdog cannot be cleared in the interrupt, otherwise the main program cannot be detected.

The program should only have the action of clearing the watchdog in the main program. This architecture can maximize the protection function of the watchdog.

3.12.4 LVR low voltage reset

Power-down reset A system voltage dip caused by external factors (for example, interference or changes in external load). A brown-out may cause the system to malfunction or program execution errors.



Voltage drops can enter the system dead zone. The system dead zone means that the power supply does not meet the minimum operating voltage requirements of the system. The figure above is a typical power-down reset diagram. In the figure, VDD is severely disturbed and the voltage drop is very low. The system above the dotted line works normally. In the area below the dotted line, the system enters an unknown working state. This area is called the dead zone. When VDD falls to V1, the system is still in a normal state; when VDD falls to V2 and V3, the system enters the dead zone, which is easy to cause an error. The system may enter the dead zone in the following cases:

DC application:

In DC applications, battery power is generally used. When the battery voltage is too low or the microcontroller drives the load, the system voltage may drop and enter the dead zone. At this time, the power supply does not fall further to the LVD detection voltage, so the system remains in the dead zone.

AC application:

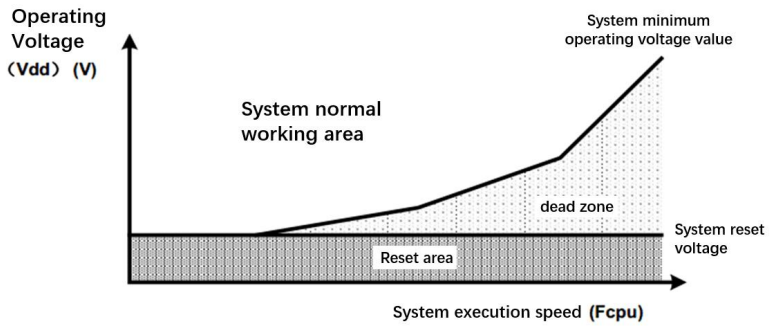
When the system is powered by AC, the DC voltage value is affected by noise in the AC power supply. When the external load is too high, such as driving the motor,

the interference caused by the load action also affects the DC power supply. If VDD falls below the minimum operating voltage due to interference, the system may enter unstable operation.

In the AC application, the system has a long time to power on and off. Among them, the power-on sequence protection makes the system power on normally, but the power-off process is similar to that in the DC operation. After the AC power is turned off, the VDD voltage is easy to enter the dead zone during the slow decline.

3.12.5 Relationship between working frequency and LVR low voltage detection

In order to improve the performance of the system power-down reset, it is necessary to clarify that the system has the minimum operating voltage value. The minimum operating voltage of the system is related to the system execution speed, and the minimum operating voltage value is different at different execution speeds.



As shown in the figure above, the normal operating voltage range of the system is generally higher than the system reset voltage, and the reset voltage is determined by the low voltage detection (LVR) level. When the system execution speed is increased, the minimum operating voltage of the system is also increased accordingly. However, since the system reset voltage is fixed, a voltage region will appear between the system minimum operating voltage and the system reset voltage, and the system will not work normally or reset, this area is the dead zone.

To avoid dead band voltage, select the appropriate LVR reset voltage point when selecting the operating frequency. The following table:

operating frequency	LVR reset voltage point
IRC-16M	LVR-3.5V or more
IRC-8M	LVR-2.7V or more
IRC-4M	LVR-1.8V or more
IRC-1M	LVR-1.6V or more

3.13 System clock function module

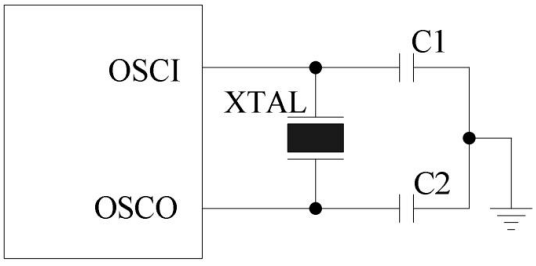
The JZ8P2603 integrates six oscillators internally and can be configured with OPTION. See the following table for details:

Oscillator type	Description
ERC (External resistance oscillator)	P55:ERCIN; P70:GPIO
ERC (External resistance oscillator)	P55:ERCIN; P50:RCOUT
IRC (Built-in RC oscillator)	Can choose 1M/2M/4M/8M through RCM P55: GPIO; P70: GPIO
IRC (Built-in RC oscillator)	Can choose 1M/2M/4M/8M through RCM P55: GPIO; P70: RCOUT
LXT1 (Low speed crystal)	100K～1M
HXT1 (High speed crystal)	12M～16M
LXT2 (Low speed crystal)	32.768KHz
HXT2 (High speed crystal)	6M～12M
XT (crystal)	1M～6M

Note: The system frequency transition point between HXT and LXT is around 400kHz.

3.13.1 External crystal oscillator / ceramic resonator (XT)

In most applications, crystals or ceramic resonators can be connected to the OSCO and OSCI to generate oscillation. The circuit diagram is as follows. Both HXT and LXT modes are applicable. The recommended values for C1 and C2 are shown in the table. Due to the different characteristics of each resonator, the user should select the appropriate values of C1 and C2 with reference to their specifications.



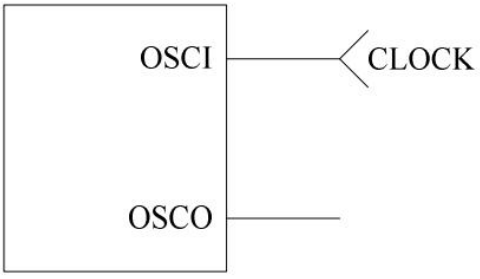
Crystal/oscillator circuit

Capacitor selection reference for crystal oscillator or ceramic oscillator:

Oscillator mode	Frequency mode	Frequency	C1(pF)	C2(pF)

ceramic oscillator	LXT1 (100K～1M)	100 KHz	60	60
		200 KHz	60	60
		455 KHz	40	40
		1 MHz	30	30
	XT (1M～6M)	1 MHz	30	30
		2 KHz	30	30
		4 KHz	20	20
crystal oscillator	LXT2 (32.768K)	32.768 KHz	40	40
	LXT1 (100K～1M)	100 KHz	60	60
		200 KHz	60	60
		455 KHz	40	40
		1 MHz	30	30
	XT (1M～6M)	1 MHz	30	30
		2 MHz	30	30
		4 MHz	20	20
		6 MHz	30	30
	HXT2 (6M～12M)	6 MHz	30	30
		8 MHz	20	20
		12 MHz	30	30
	HXT1 (12M～16M)	12 MHz	30	30
		16 MHz	20	20

Note: The above data is for reference only. Please use the physical test for all use. The JZ8P2603 can also be driven by an external clock signal on the OSCI pin. The application diagram is as follows:



External clock schematic

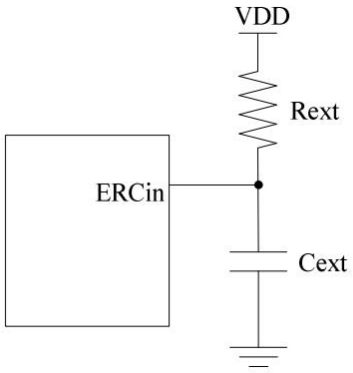
3.13.2 External RC oscillator mode (ERC)

In some applications where clock accuracy is not critical, the use of an RC oscillator can save some cost. However, it should be noted that the frequency of the RC oscillatoris is related with the voltage, the resistance value (Rext), and the capacitance value (Cext), even the operating temperature. In addition, due to the difference in production process between the chips, the frequency will also change slightly.

The smaller the resistance of the RC oscillator, the higher the frequency. On the other hand, for very small resistance values, such as 1k ohms, the oscillator

will become unstable because the NMOS cannot discharge the capacitor correctly. In order to obtain a stable system frequency, the capacitance value cannot be less than 20pF, and the resistance value cannot be greater than 1M ohm. If they are not within this range, the frequency will be very susceptible to noise, moisture and leakage.

Power supply voltage, operating temperature, RC oscillator components, package style, and PCB layout all affect system frequency.



External RC oscillator mode circuit

The RC oscillator frequency reference table is shown below for reference only: (The following data is simulation data, for design reference only)

Rext	Cext	Frequency
5.1K	100p	427.2KHz
	200p	254.4KHz
	300p	189.4KHz

3.13.3 Internal RC Oscillator Mode (IRC)

The JZ8P2603 provides an internal RC mode with a default frequency of 4MHz.

The internal RC oscillator mode has other frequency values such as 16MHz, 8MHz and 1MHz. The IRC operating frequency can be selected by setting the OPTION configuration bits. The following are their correspondences:

Firc	IRC frequency
4 M	IRC frequency is chosen to be 4MHz
16 M	IRC frequency is chosen to be 16MHz
8 M	IRC frequency is chosen to be 8MHz
1 M	IRC frequency is chosen to be 1MHz

3.13.4 Clock module application instructions

The internal oscillator is the most common mode of oscillation, which avoids the use of external circuitry;

When using an external clock input, the clock signal is input from the OSCI and the OSCO can be left floating;

When using an external oscillator and the frequency is greater than 400 kHz, be sure to select an external high-speed oscillator in the OPTION option when programming. Correspondingly, the external low-speed oscillator is selected when less than 400 kHz;

Different external conditions, the clock frequency of each oscillation mode may be slightly different, and should be reasonably selected according to needs when using.

4 CODE OPTION Register

CODE OPTION	option	Description of function
POWER	HIGH	IRC frequency is calibrated at VDD=5V
	LOW	IRC frequency is calibrated at VDD=3V
System clock warm-up (WKCK)	8 Fosc	System clock warm-up time selection 8Fosc
	32 Fosc	System clock warm-up time select 32Fosc (default)
P71port	RESET	P71 as external RESET
	GPIO	P71 as GPIO (default)
WTD	enable	WDT enable
	disable	WDT is disabled (default)
Sub-clock selection	128KHz	Sub clock selection 128KHz
	16KHz	Sub clock selection 16KHz
Reset time	4.5ms	System setup time selection 4.5ms
	18ms	System setup time selection 18ms
Code encryption	enable	Burn mode data encryption
	disable	Burn mode data is not encrypted
Package pin	20PIN	Package style select 20PIN (default)
	16PIN/18PIN	Package type selection 16/18PIN unused pin must set output low
	14PIN	Package type selection 14PIN unused pin must set output low
	8PIN/10PIN	Package type selection 8/10PIN unused pin must set output low
Clocks Frequency division	2Clocks	Instruction cycle selection 2Clocks
	4Clocks	Instruction cycle selection 4Clocks
	8Clocks	Instruction cycle selection 8Clocks
	16Clocks	Instruction cycle selection 16Clocks
Low voltage reset (LVR)	1.6V	Low voltage reset point selects 1.6V
	1.8V	Low voltage reset point selects 1.8V(default)
	2.7V	Low voltage reset point selects 2.7V
	3.5V	Low voltage reset point selects 3.5V
	4V	Low voltage reset point selects 4V
External interrupt filtering (NR)	diaable	External interrupt filtering option disabled
	8Fosc	Filter time 8Fosc
	32Fosc	Filter time 32Fosc
IRC frequency	4M	RC frequency selects 4M

	16M	RC frequency selects 16M
	8M	RC frequency selects 8M
	1M	RC frequency selects 1M
Oscillation mode	ERC mode	ERC mode
	IRC mode	IRC mode
	LXT1（100K～1M）	LXT1（100K～1M） mode
	HXT1（12M～16）	HXT1（12M～16） mode
	LXT2（32K）	LXT2（32K） mode
	HXT2（6M～12M）	HXT2（6M～12M） mode
	XT（1M～6M）	XT（1M～6M） mode
P70 port	GPIO	P70 is used as GPIO
	RCOUT	P70 is used as the instruction cycle output port, open drain output is disabled
	RCOUT_OD	P70 is used as the instruction cycle output port, open drain output is enabled

5 Electrical Characteristics

5.1 Chip limit parameter

Operating temperature (℃)	(√) E:-40-85;
storage temperature (℃)	(√) -65～+150
Limit voltage (V)	(√) other -0.3～6
Limit input voltage (V)	(√) other GND-0.3～VDD+0.5;
Limit output voltage (V)	(√) other GND-0.3～VDD+0.5;

5.2 Chip DC parameters

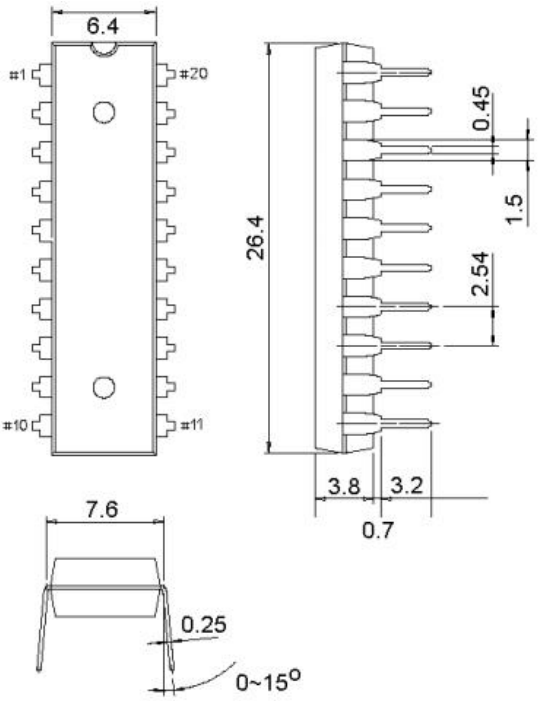
(T=25℃, VDD=5±5%V,GND=0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ERC	外接阻容振荡	R:5.1KΩ, C:100pf	0.76	0.95	1.14	MHz
IRC1	Built-in RC oscillation 1 (after correction)	Firc0:Firc1=1:1		4		MHz
IRC2	Built-in RC oscillation 2 (after correction)	Firc0:Firc1=1:0		16		MHz
IRC3	Built-in RC oscillation 3 (after correction)	Firc0:Firc1=0:1		8		MHz
IRC4	Built-in RC oscillation 4 (after correction)	Firc0:Firc1=0:0		1		MHz
VIH1	Input high level	P5, P6, P70	0.6*VDD		VDD	V
VIL1	Input low level	P5, P6, P70	-0.3V		0.4*VDD	V
IOH1	Output high level drive (except P71)	IOH=VDD-0.6V		4.5		mA
IOH2	Output High Drive Enhancement (P71)	IOH=VDD-0.6V		11		mA
IOL1	IO output low level drive	IOL=GND+0.6V		17		mA
IOL2	IO output low level	IOL= GND+0.6V		35		mA

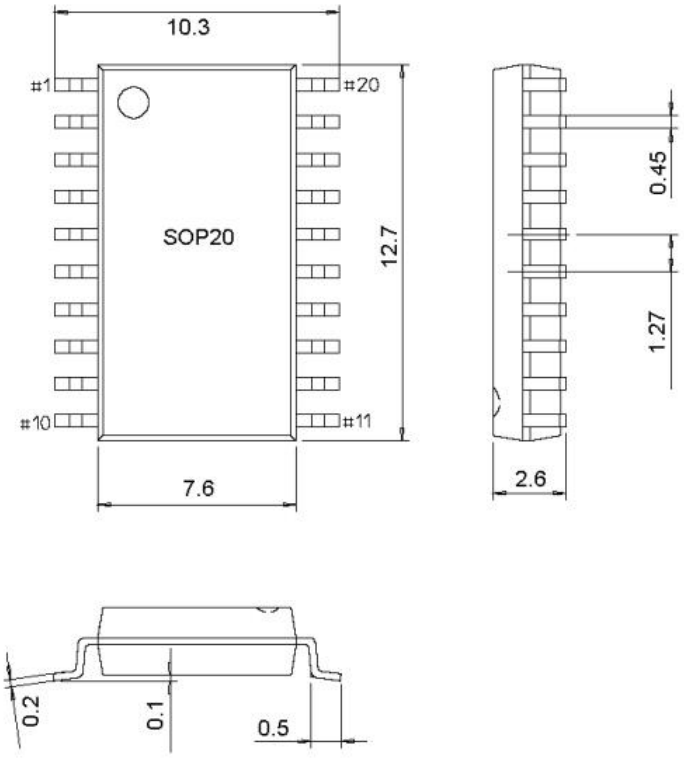
	drive enhancement					
IPH	Pull-up current	Pull-up enable, input is connected to ground		70		μA
IPL	Pull-down current	Pull-down enable, input is connected to VDD		40		μA
Isb1	Shutdown current 1	All inputs are connected to VDD, the output is left floating, WDT, LVD disabled			2	μA
Isb2	Shutdown current 2	All inputs are connected to VDD, the output is left floating, WDT is enabled, LVD is disabled			10	μA
Isb3	Shutdown current 3	All inputs are connected to VDD, the output is left floating, WDT is disabled, LVD is enabled			10	μA
Iop1	Working current 1 (VDD=3V)	32KHz mode, 2clks, input is connected to VDD, output is floating, WDT, LVD are disabled, select low power mode			20	μA
Iop2	Working current 2	System clock 4MHz, 2clks, The output is floating, the input is connected to VDD, and the high power mode is selected.			1.7	mA
LVR1	Low voltage reset voltage 1	Select 1.8V reset poin		1.8		V
LVR3	Low voltage reset voltage 3	Select Vlvr reset poin	Vlvr-0.2	Vlvr	Vlvr+0.2	V
LVD	Low voltage detection voltage	Select Vlvd as the detection point	Vlvd-0.2	Vlvd	Vlvd+0.2	V

6 Package size information

6.1 20PIN Package Size

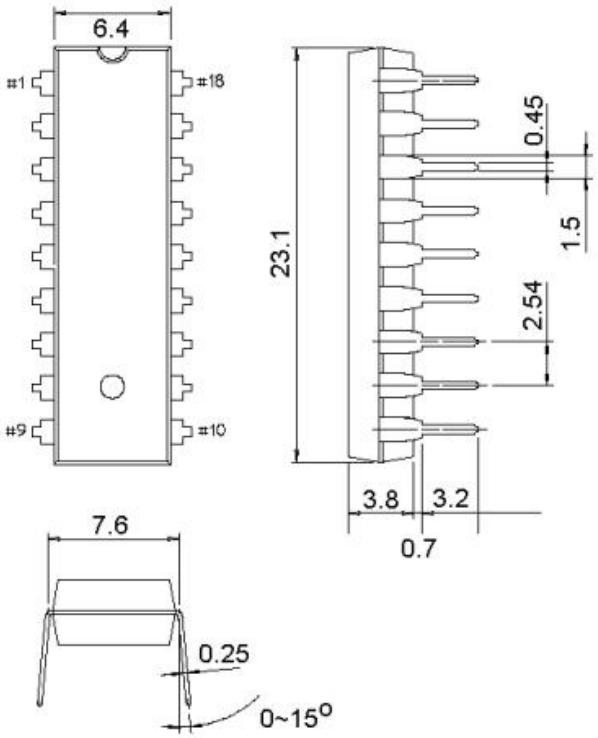


DIP20 Package Size

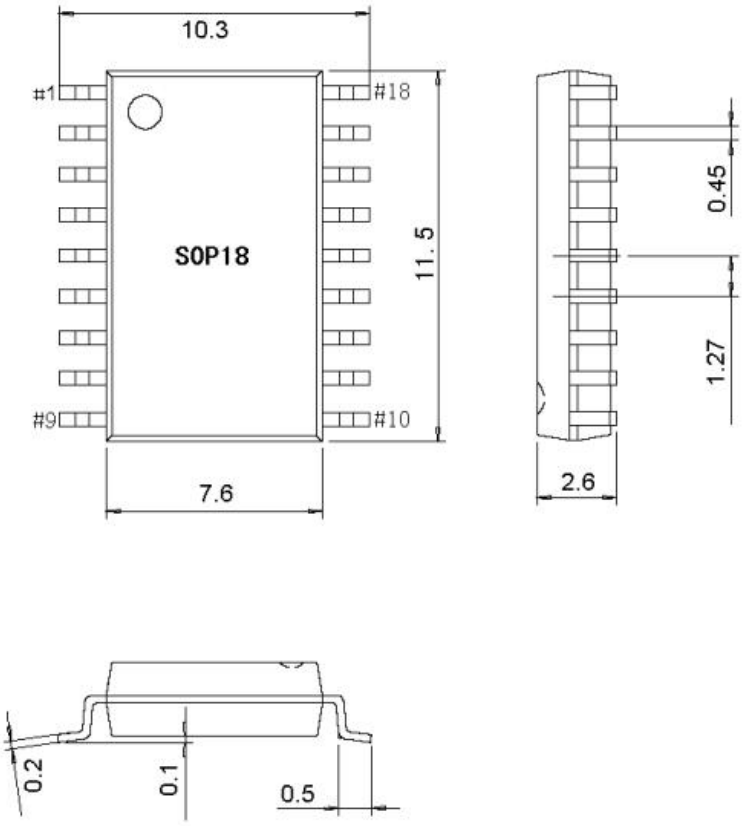


SOP20 Package Size

6.2 18PIN Package Size

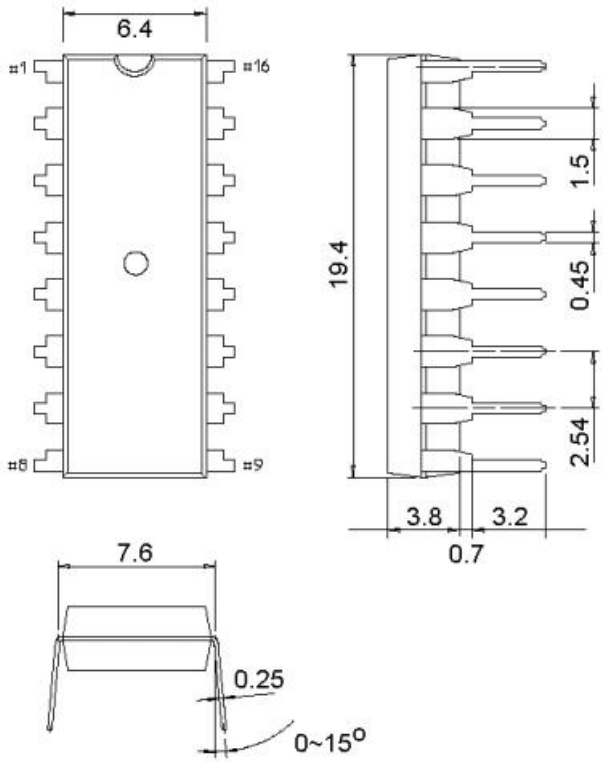


DIP18 Package Size

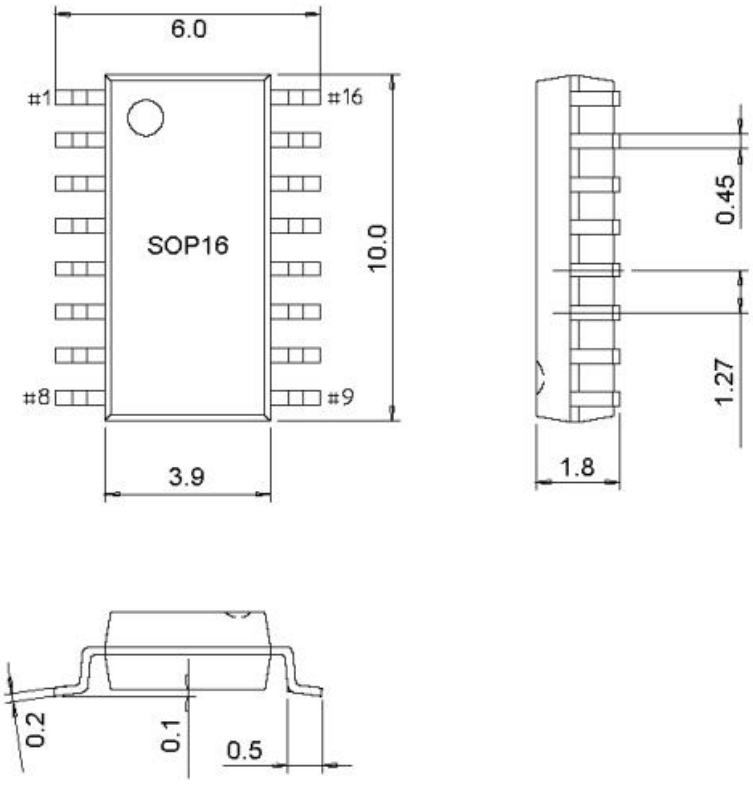


SOP18 Package Size

6.3 16PIN Package Size

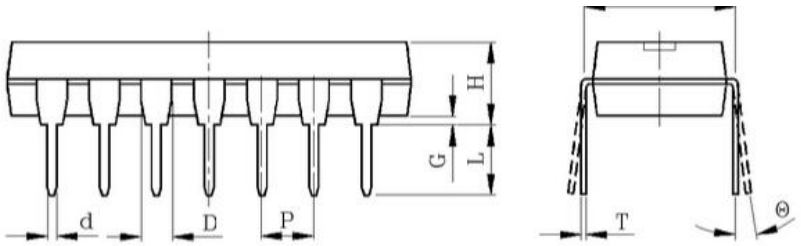


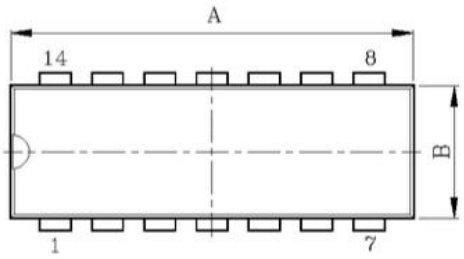
DIP16 Package Size



SOP16 Package Size

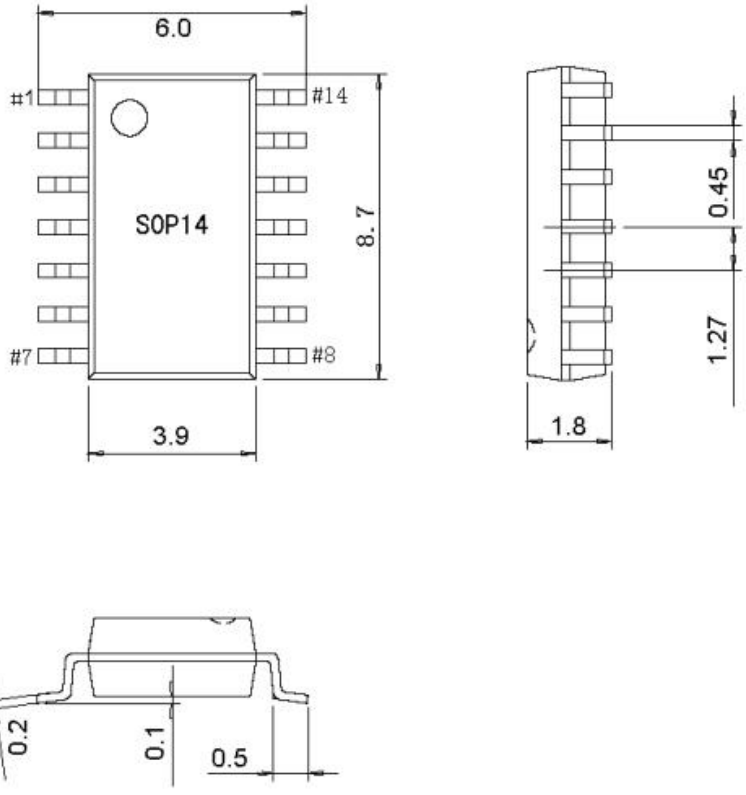
6.4 14PIN Package Size





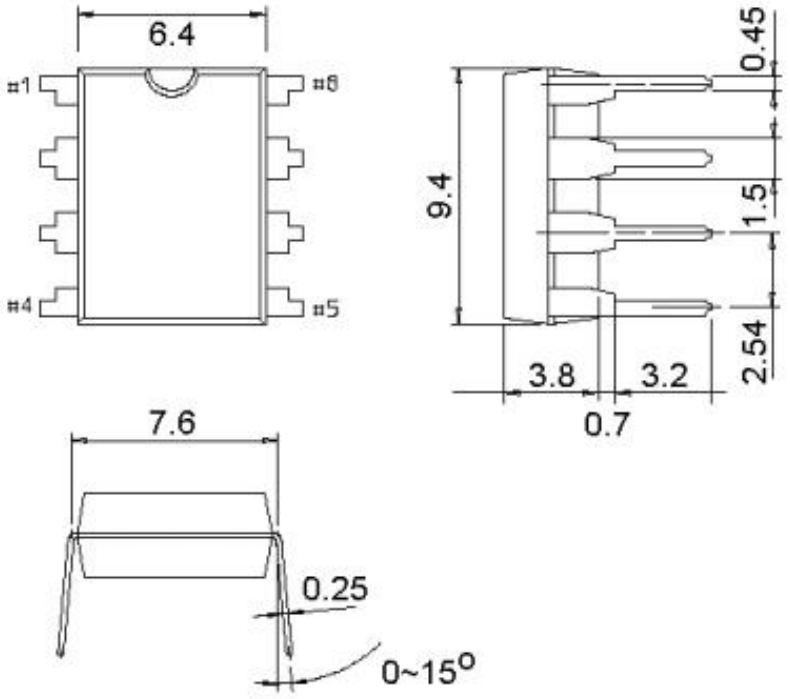
DIM	MILLIMETERS
A	19.3±0.2
B	6.45±0.2
D	1.52±0.1
d	0.46±0.1
G	0.50 MIN
H	3.8±0.3
L	3.3±0.3
P	2.54
T	0.25+0.1/−0.05
W	7.62
Θ	0 ~ 15°

DIP14 Package Size

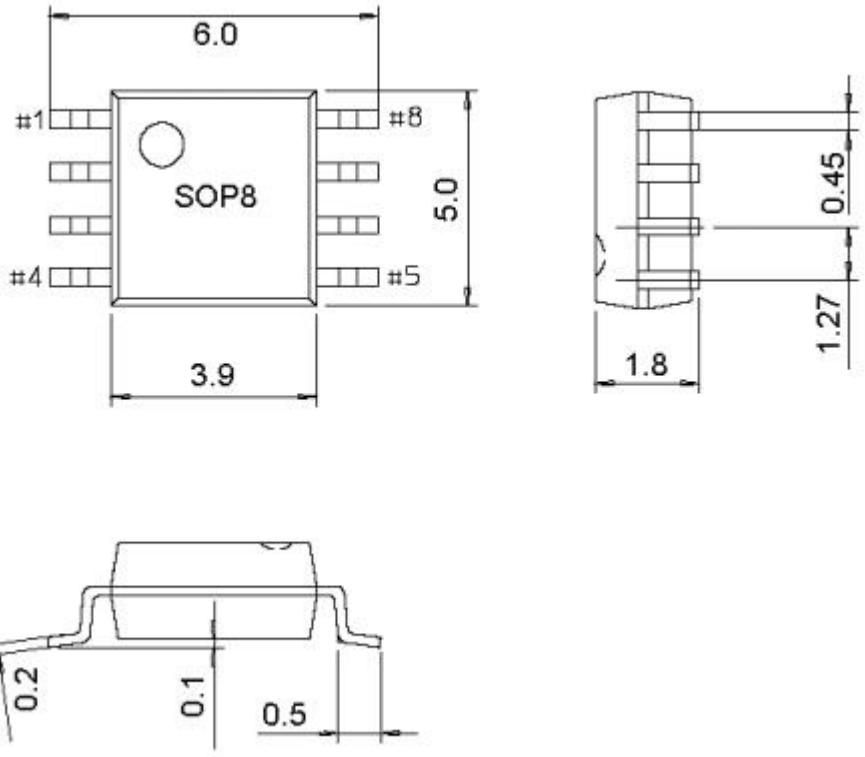


SOP14 Package Size

6.5 8PIN Package Size



DIP8 Package Size



SOP8 Package Size