JZ8P2615

8-Bit Microcontroller with OTP ROM

DATASHEET

VERSION 1.0

Specification Revision History

Version	Modified instructions	Remarks
V0.0	First draft version	
V1.0	Release first version	

Notes:

1. When using PWM3/IPWM3 dead-time complementary clock frequency division function, it is necessary to synchronize PWM1E or IPWM1E bit; When using PWM4/IPWM4 dead-time complementary clock frequency division function, PWM2E or IPWM2E bit should be synchronized and enabled.

2, the use of TC1 timer function, make can still need to make after TC1EN PWM1E/IPWM1E/PWM3E/IPWM3E in any one. (Same with TC2)

3. When using PWM function and clock frequency doubling function at the same time, it must be used with PWM frequency divider to avoid abnormal PWM function.

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1. General Description

1.1 Functional Features

CPU configuration

- 2K×16-Bit OTP ROM
- 128×8-Bit SRAM
- 8 levels of stack space
- 8 programmable Voltage Reset (LVR)
  1.2V, 1.6V, 1.8V, 2.4V
  2.7V, 3.3V, 3.6V, 3.9V
- Operating current less than 2 mA (4MHz/5V)
- Operating current less than 10μA (16KHz/3V)
- Sleep current less than 1μA(sleep mode)

I/O configuration

- 2 sets of bidirectional IO ports: P5, P6
- 14 I/O pins
- Wake-up ports: P5, P6
- 14 programmable pull-up I/O pins
- 14 programmable pull-down I/O pins
- External interrupts:P60, P53
- Reference voltage output:P65

Operating voltage

- Operating voltage range:

V_{LVR}2.4 V ~ 5.5 V | Fcpu = 0 ~ 8 MHz

V_{LVR}1.8 V ~ 5.5 V | Fcpu = 0 ~ 4 MHz

V_{LVR}1.6 V ~ 5.5 V | Fcpu = 0 ~ 2 MHz

Working frequency range

- Internal IHRC oscillation circuit:
  8 MHz / 6 MHz / 5.4 MHz / 4.8 MHz / 3.4 MHz / 1 MHz
- Internal ILRC oscillation circuit:
  14KHz(5V)/8KHz(3V)
- Clock cycle frequency division selection:
  2Clock, 4Clock, 8Clock, 16Clock

Peripheral modules

- 8Bit real-time clock/counter TC0
- 4-way 2 sets of 10Bit complementary cascading pulse width modulators
- 14-channel 12Bit ADC ADC

Interrupt source

- TC0 overflow interrupt
- External interrupt 1
- External interrupt 0
- P6 port input change interrupt
- Interrupt for input change at port P5
- Interrupt for ADC conversion completion
- PWM1 cycle/duty cycle matching interrupt
- PWM2 cycle/duty cycle matching interruption
- PWM3 duty cycle matching interruption
- PWM4 duty cycle matching interrupt

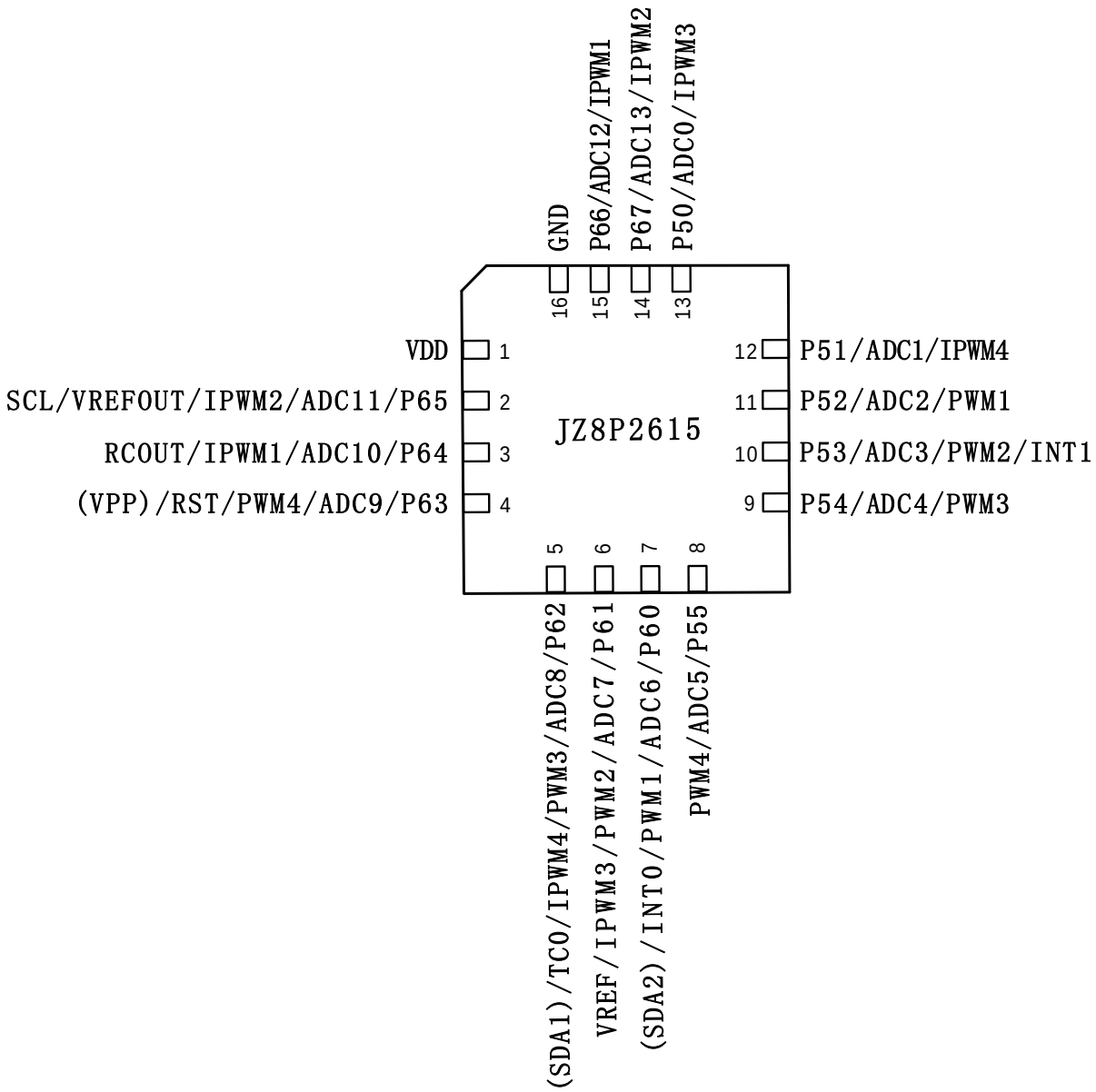
Features

- Programmable WDT timer
- Four working modes switch

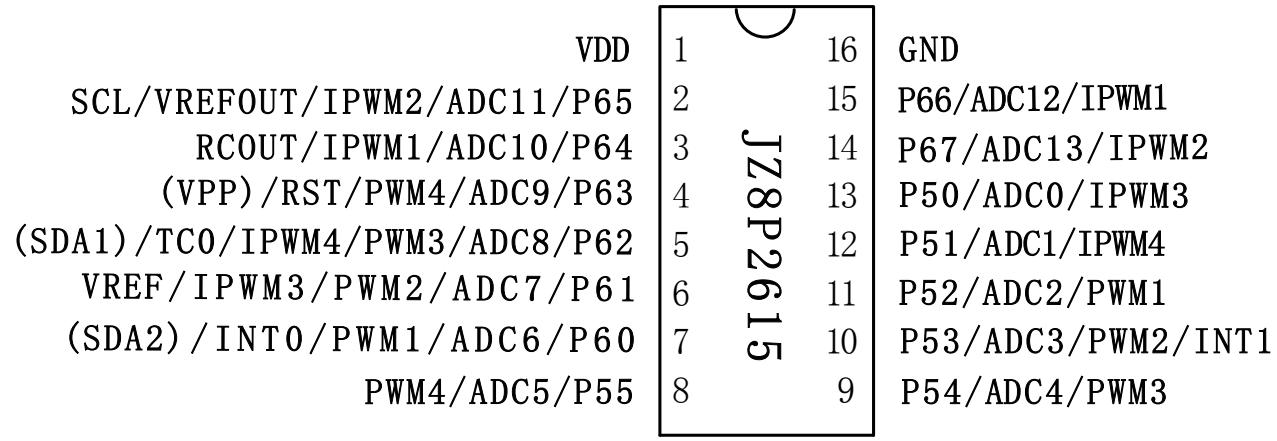
Package type

- JZ8P2615-QFN/DIP/SOP16
- JZ8P2615-DIP/SOP14
- JZ8P2615-MSOP10
- JZ8P2615-DIP/SOP8

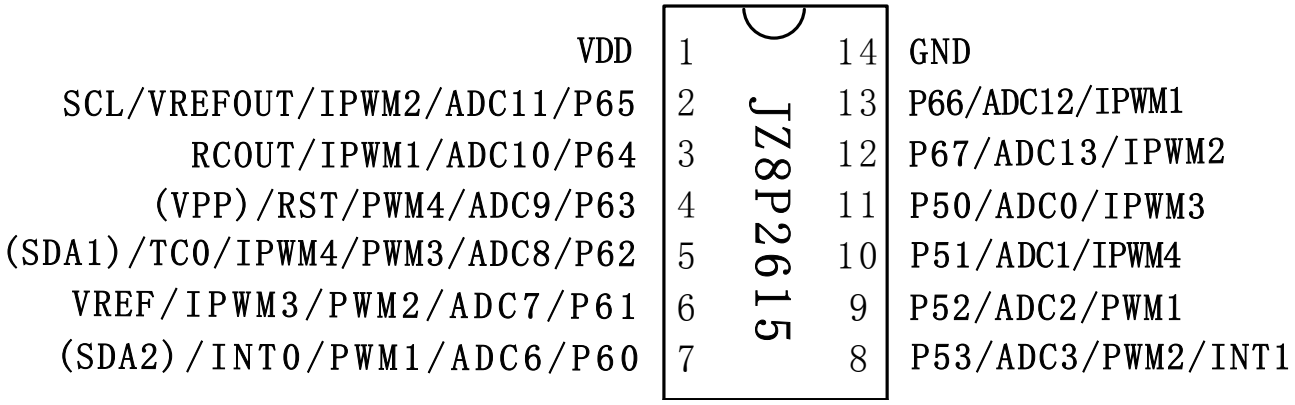
1.2 Pin assignment



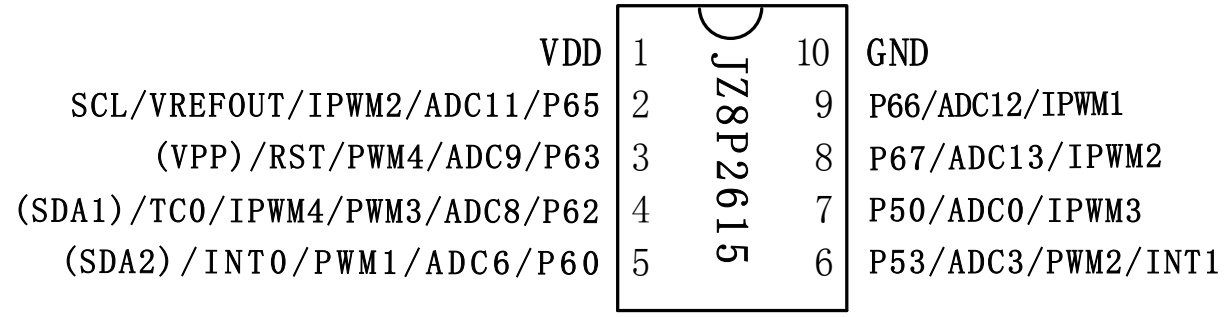
JZ8P2615-QFN16 PIN MAP



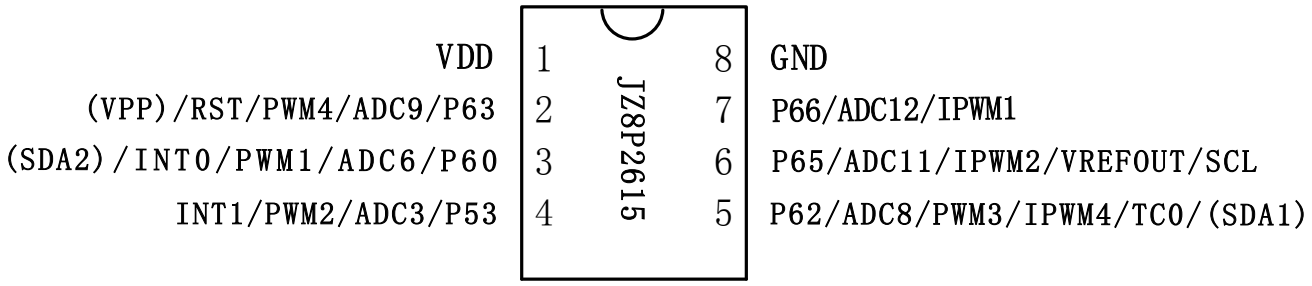
JZ8P2615-16PIN MAP



JZ8P2615-14PIN MAP



JZ8P2615-10PIN MAP



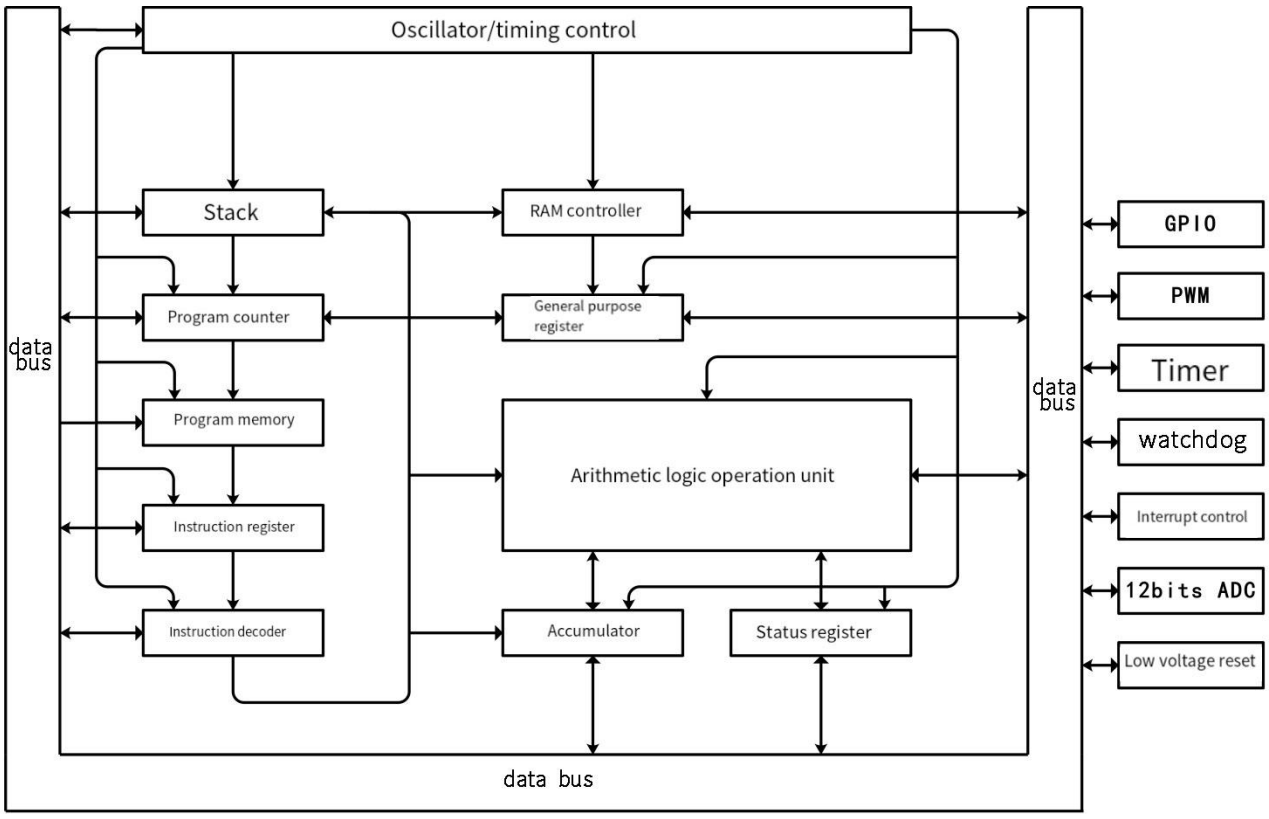
JZ8P2615-8PIN MAP

1.3 Pin description

Num.	Name	I/O	Description
P50	P50	I/O	GPIO, programmable pull up and down, port wake up
	AIN0	AN	ADC input channel
	IPWM3	O	IPWM3 output
P51	P51	I/O	GPIO, programmable pull up and down, port wake up
	AIN1	AN	ADC input channel
	IPWM4	O	IPWM4 output
P52	P52	I/O	GPIO, programmable pull up and down, port wake up
	AIN2	AN	ADC input channel
	PWM1	O	PWM1 output
P53	P53	I/O	GPIO, programmable pull up and down, port wake up
	AIN3	AN	ADC input channel
	PWM2	O	PWM2 output
	INT1	I	External Interrupt 1 Input port
P54	P54	I/O	GPIO, programmable pull up and down, port wake up
	AIN4	AN	ADC input channel
	PWM3	O	PWM3 output
P55	P55	I/O	GPIO, programmable pull up and down, port wake up
	AIN5	AN	ADC input channel
	PWM4	O	PWM4 output
P60	P60	I/O	GPIO, programmable pull up and down, open drain, weak drive,
	AIN6	AN	ADC input channel
	PWM1	O	PWM1 output
	INT0	I	External interrupt 0 input port
	SDA2	I	Burn data port 2
P61	P61	I/O	GPIO, programmable pull up and down, open drain, weak drive,
	AIN7	AN	ADC input channel
	PWM2	O	PWM2 output
	IPWM3	O	IPWM3 output
	VREF	AN	ADC external reference voltage input port
P62	P62	I/O	GPIO, programmable pull up and down, open drain, weak drive,
	AIN8	AN	ADC input channel
	PWM3	O	PWM3 output
	IPWM4	O	IPWM4 output
	TC0	I	TC0 external clock input port
	SDA1	I	Burn data port 1

Num.	Name	I/O	Description
P63	P63	I/O	GPIO, programmable pull up and down, open drain, weak drive,
	AIN9	AN	ADC input channel
	PWM4	O	PWM4 output
	RST	I	External reset input port
	VPP	I	Burn the high pressure port
P64	P64	I/O	GPIO, programmable pull up and down, open drain, weak drive,
	AIN10	AN	ADC input channel
	IPWM1	O	IPWM1 output
	RCOUT	O	Internal instruction clock frequency output
P65	P65	I/O	GPIO, programmable pull up and down, open drain, weak drive,
	AIN11	AN	ADC input channel 13
	IPWM2	O	IPWM2 output
	VREFOU	AN	Reference voltage outlet
	SCL	I	Burn the clock port
P66	P66	I/O	GPIO, programmable pull up and down, open drain, weak drive,
	AIN12	AN	ADC input channel
	IPWM1	O	IPWM1 output
P67	P67	I/O	GPIO, programmable pull up and down, open drain, weak drive,
	AIN13	AN	ADC input channel
	IPWM2	O	IPWM2 output
	VDD	--	Power supply
	GND	--	to

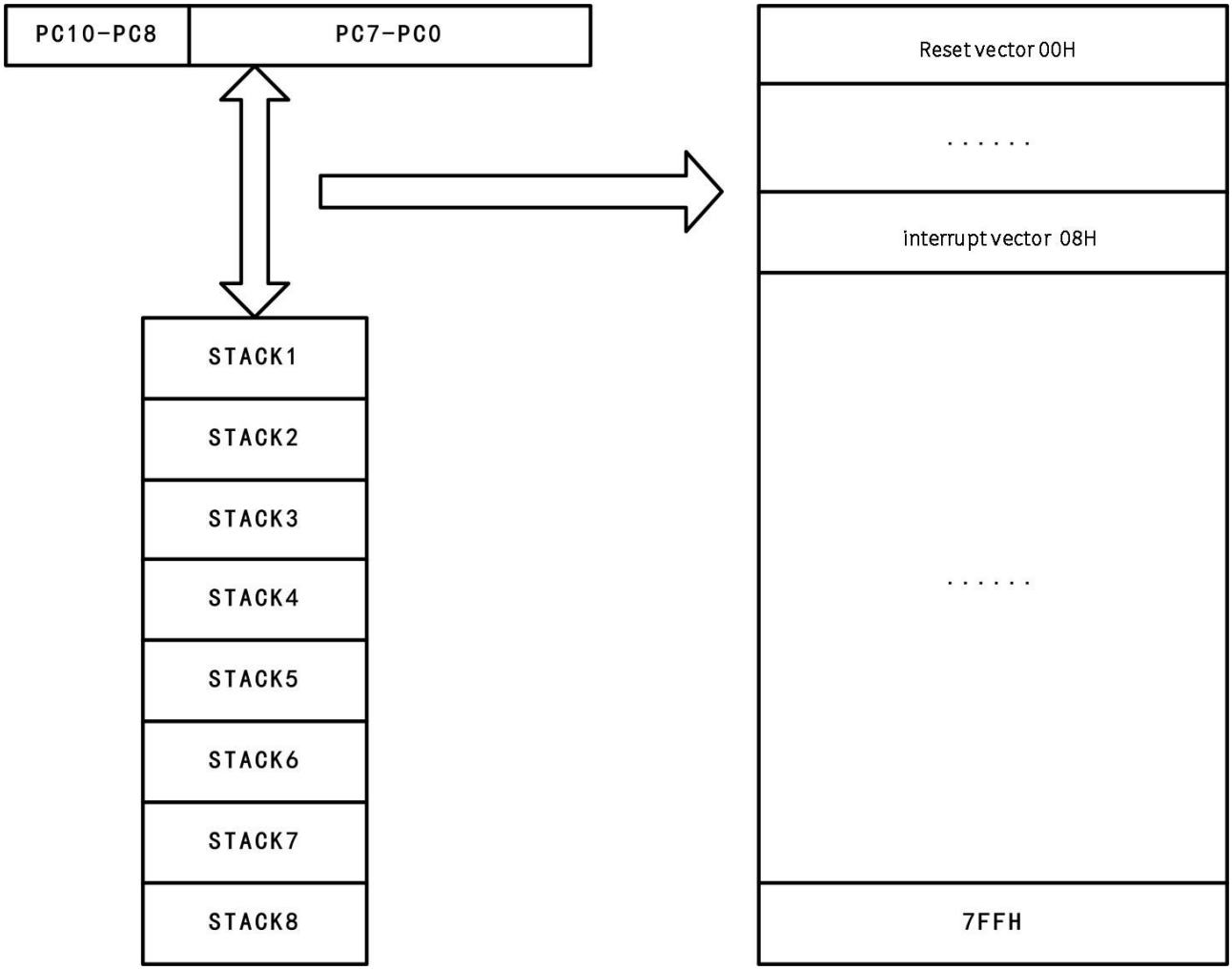
1.4 System block diagram



System circuit block diagram

2. Memory structure

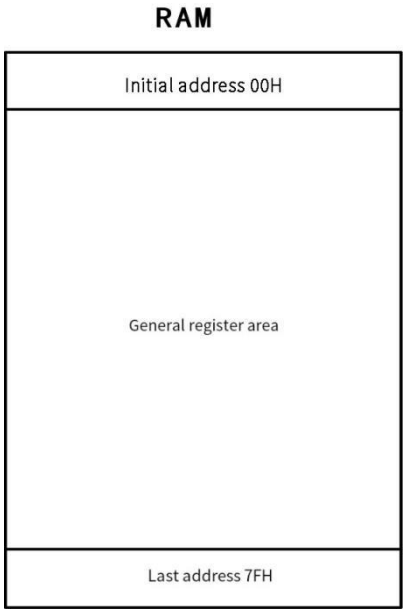
2.1 Structure of the program store



Program store structure diagram

2.2 The data store

2.2.1 Data store structure



Data storage area

2.2.2 Overview of special function registers

Address	0X18_	0X19_	0X1A_	0X1B_	0X1C_	0X1D_	0X1E_	0X1F_
0	RSR	P5PH	P5ADE	TC1CON				
1	PCH	P6PH	P6ADE	TC1PRDL				
2	PCL			PWM1DTL				
3	STATUS	P5PD	ADATH	TC1PRDTH				
4	TC0CON	P6PD	ADATL	TC1CH				
5	TC0C		ADIS	TC1CL				
6	TBRDH		ADCON0	TC2CON	PWMIS	INTE0		
7	TBRDL		ADCON1	TC2PRDL	DEADCON	INTE1		
8	CPUCON			PWM2DTL	PWMCON			
9	IHRCCAL	P6OD		TC2PRDTH	DEADT0			
A (10)	P5	P6WD		TC2CH	DEADT1	INTF0		
B (11)	P6			TC2CL		INTF1		
C (12)		P5IWE		PWM3DTH				
D (13)	P5CON	P6IWE		PWM3DTL				
E (14)	P6CON			PWM4DTH				
F (15)			WDTCON	PWM4DTL				IAR

3 Functional description

3.1 Operate registers

3.1.1 R180/RSR(RAM Select Register)

0X180	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSR	-	RSR<6:0>						
Read/write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	X	X	X	X	X	X	X

RSR<6:0> is used in indirect addressing mode to select the RAM register address (addressing range: 0X00 to 0X7F).

The RSR register is used to cooperate with the R1FF register to realize the indirect addressing operation. You can place the address corresponding to a register in the RSR, and then by accessing the indirectly addressed register R1FF, the address will point to the register at the corresponding address in the RSR.

3.1.2 R181/PCH(Program Count High Bit Register)

0X181	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCH	-	-	-	-	-	PC<10:8>		
Read/write	R	R	R	R	R	R	R	R
Reset values	0	0	0	0	0	0	0	0

3.1.3 R182 /PCL(Program Count Low Bit Register)

0X182	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCL	PC<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

The program counter (PC) is a pointer used to record the instructions to be processed by the CPU in each instruction cycle. During the CPU run cycle, the PC pushes the instruction pointer into the program memory, and the pointer is incremented by 1 to enter the next cycle. The JZ8P2615 has an 11-bit wide program counter (PC) whose low bytes come from the readable and writable PCL register and high bytes come from the readable PCH register.

The stack is used to record the instruction pointer returned by the program. When a subprogram is called, the PC pushes the instruction pointer onto the stack. When the return

instruction is to be executed, the stack sends the instruction pointer back to the PC to continue the original process. The JZ8P2615 has an 8-level stack that occupies neither program nor data storage space, and the stack pointer cannot be read or written.

The program counter (PC) and the stack are described in detail as follows:

(1) Both the register PC and the built-in 8-level stack are 11 bits wide and are used for addressing 2K×16Bit OTP ROMs.

(2) In general, PC is incremented by one; When reset, all bits of PC are reset.

(3) Instruction "JMP" allows to load the 11-bit address directly and then push PC+1 onto the stack. Therefore, the JMP instruction allows the PC to jump to any position in the program.

(4) Instruction "CALL" allows to load the 11-bit address of the PC and then push PC+1 onto the stack. Therefore, the subroutine entry address can be located at any position in the program.

(5) Execute the "RET" instruction to send the top of the stack data to the PC.

(6) Execute the "ADD PCL,A" instruction to add a relative address to the current PC, and the ninth and above bits of the PC are incremented one by one.

(7) Perform the instruction "MOV PCL,A" to load an address from the "A" register to the lower 8 bits of the PC, and the ninth bit and above of the PC remain unchanged.

(8) Any instruction (other than the "ADD PCL,A" instruction) that writes A value to the PCL (for example: "MOV PCL,A", "BTC PCL,1") will leave the ninth and tenth bits of the PC unchanged.

(9) Any instruction except "TBRD R" is a single instruction cycle.

The stack works like a loop buffer, meaning that after eight stack pushes, the data in the ninth push will overwrite the data in the first push, the data in the tenth push will overwrite the data in the second push, and so on.

3.1.4 R183 /STATUS(Status flag register)

0X183	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	RST	GP1	GP0	T	P	Z	DC	C
Reading/Writing	R	R/W	R/W	R	R	R/W	R/W	R/W
Reset value	0	0	0	1	1	X	X	X

Bit<7> : Rst-reset or wakeup flag bit

0: Other reset type

1: Wake up by pin state change

Bit<6> : GP1- General purpose register bit

Bit<5> : GP0- General register bit

Bit<4> : T- time overflow bit

0: WDT overflow

1: Perform "SLEEP" and "CWDT" commands or low voltage reset

Bit<3> : P- power down flag bit

0: Execute the "SLEEP" command

1: Power on reset or execute "CWDT" command

The events that affect T/P are listed in the table below:

Type	RST	T	P
Power on reset	0	1	1
Press RESET in work mode	0	Keep	Keep
RESET Wake up	0	1	0
WDT overflows in working mode	0	0	Keep
WDT overflow wakes up	0	0	0
Port input change wake up	1	1	0
Execute the CWDT command	Keep	1	1
Execute the SLEEP command	Keep	1	0

Bit<2> : Z- Set to "1" if the result of an arithmetic or logical operation is zero.

0: When the result of an arithmetic or logical operation is not 0

1: When the result of an arithmetic or logical operation is 0

Bit<1> : DC- Auxiliary carry flag

0: When performing the addition, no carry is generated for the lower four bits; / when performing a subtraction operation, the lower four bits produce a borrow

1: When performing the addition operation, the lower four bits have carry generation; / When performing subtraction, no borrow is generated for the lower four bits

Bit<0> : C- Carry flag

0: When performing the addition, no carry is generated for the upper four bits; / when performing subtraction, the high four bits produce a borrow

1: When performing the addition operation, the higher four bits have carry generation; / When performing subtraction, no borrows are generated

3.1.5 R184 /TC0CON(TC0 control register)

0X184	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CON	TC0CKS	GIE	TS	TE	PAB	TC0PSR<2:0>		
Read/write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	1	1	1	1

Bit<7>：TC0CKS-TCO clock select bit

1: Select the system clock

0: Select instruction cycle clock or external input clock, TC0CKS=0 clock source determined by TS

Bit<6> : GIe-interrupt enable flag bit

0: Interrupts are forbidden by instruction or hardware

1: Interrupt enabled by instruction

Bit<5> : TS-TC0 signal source selection bit

0: Internal instruction cycle clock

1: External input signal (P62 needs to be set as input port)

Bit<4>： TE-TC0 signal edge selection bit

0: TC0 pin signal changes from low to high plus 1

1: TC0 pin signal change from high to low add 1

Bit<3>： PAB-pre-divider allocates bits

0: predivider is assigned to TC0

1: predivider is assigned to WDT

Bit<2:0> : TC0PSR<2:0>-TC0/WDT pre-divider selection control bit:

TC0PSR<2>	TC0PSR<1>	TC0PSR<0>	TC0 frequency division coefficient	WDT frequency division coefficient
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Note: When switching between PAB and TC0PSR<2:0>, the watchdog must be disabled first, and the watchdog can be enabled after the switch is completed.

3.1.6 R185 /TC0C (TC0 count register)

0X185	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0C	TC0C<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

TC0 is an 8Bit uplink counter, clock source optional internal clock/external clock, count overflow can form interrupts, TC0C register can be read and written.

TC0 can be triggered by the signal edge on pin P62 / command cycle clock/system clock to generate 1 + operation. If the PAB bit is reset, there will be a predivider assigned to TC0, and when the TC0 register or TC0 predivider is assigned, the value of the predivider will be reset.

3.1.7 R186 /TBRDH (look-up table pointer High Bit Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	-	-	-	-	-	RBIT<10:8>		
Read/write	R	R	R	R	R	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

3.1.8 R187 /TBRDL (look-up table pointer low bit register)

0X187	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDL	RBIT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

3.1.9 R188/CPUCON (CPU Mode Control Register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	INT1WE	INT0WE	ADCWE	TC1TC2WE	TC0WE	STPHX	CLKMD	IDLE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7>：INT1WE-external interruption INT1 wake up enable bit

1: External interrupt INT1 wakeup enable, can wake up idle mode

0: External interrupt INT1 wakeup disabled

Bit<6>：INT0WE-external interruption INT0 wake up enable bit

1: External interrupt INT0 wakeup enable, can wake up idle mode

0: External interrupt INT0 wakeup disabled

Bit<5>：ADCWE-ADC wake up enable bit

1: ADC wakeup enable, can wake up the idle mode

0: ADC wakeup disabled

Bit<4> : TC1TC2WE-TC1/TC2 wakeup enable bit

1: TC1/TC2 wakeup enable to wake up the idle mode

0: TC1/TC2 wakeup disabled

Bit<3>：TC0WE-TC0 wake up enable bit

1: TC0 wakeup enable to wake up idle mode

0: TC0 wakeup disabled

Bit<2>：STPHX-high speed clock control bit

1: Stop the high-speed clock

0: The high-speed clock is working properly

Bit<1>：CLKMD-system clock control bit

1: System clock uses Low Speed Oscillator (ILRC) clock

0: System clock uses High Speed Oscillator (IHRC) clock

When the system enters low speed mode from high speed mode, CLKMD=1 is set first, and then STPHX=1 is set.

When the system enters the high speed mode from low speed mode, set STPHX=0 first, and then set CLKMD=0.

Bit<0>：IDLE-Idle mode enable bit

1: The system enters idle mode when it executes the SLEEP command, and the system clock works normally

TC0 and PWM can continue to work in idle mode if the system clock is selected, and the system can be woked up.

0: The system enters SLEEP mode when the sleep command is executed

3.1.10 R189 /IHRCCAL(IHRC frequency fine-tuning register)

0X189	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IHRCCAL	IHRCCAL<7:0>							
Reading/writing	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	X	X	X	X	X	X	X	X

IHRC high speed oscillator frequency fine tuning

3.1.11 R18A /P5(P5 data register)

0X18A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5	-	-	P5<5:0>					
Reading/writing	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	1	1	1	1	1

P5 Port Data control

3.1.12 R18B/P6(P6 data register)

0X18B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6	P6<7:0>							
Reading/writing	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P6 port data control

3.1.13 R18D/P5CON(P5 control register)

0X18D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5CON	-	-	P5CON<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P5 port input and output control bits:

0: Output

1: Input

3.1.14 R18E/P6CON(P6 control register)

0X18E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6CON	P6CON<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P6 port input and output control bits:

0: Output

1: Input

3.1.15 R190/P5PH(P5 pull-up control register)

0X190	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PH	-	-	P5PH<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P5 port pull-up control bit:

0: Enable

1: Forbid

3.1.16 R191/P6PH(P6 pull-up control register)

0X191	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PH	P6PH<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Port P6 pull-up control bit:

0: Enable

1: Forbid

3.1.17 R193/P5PD(P5 pull-down control register)

0X193	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PD	-	-	P5PD<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

P5 port pull-down control bit:

0: Enable

1: Forbid

3.1.18 R194/P6PD(P6 pull-down control register)

0X194	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PD	P6PD<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Pull-down control bit for port P6:

0: Enable

1. Prohibition

3.1.19 R199/P6OD(P6 drain open control register)

0X199	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6OD	P6OD<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P6 port open drain output control bit:

0: Forbidden

1: Enable

3.1.20 R19A /P6WD(P6 weak drive control register)

0X19A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6WD	P6WD<7:0>							

Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P6 port weak drive control bit:

0: Forbidden

1: Enable

3.1.21 R19C /P5IWE(P5 input change interrupt, wake up enable register)

0X19C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5IWE	-	-	P5IWE<5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P5 port input change wake-up control bit:

0: Forbidden

1: Enable

3.1.22 R19D/P6IWE(P6 input change interrupt, wake up enable register)

0X19D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6IWE	P6IWE <7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P6 port input change wake-up control bit:

0: Forbidden

1: Enable

3.1.23 R1A0/P5ADE(P5 analog port enable register)

0X1A0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5ADE	-	-	P5ADE <5:0>					
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P5 port ADC channel selection control bit:

0: Port is set to GPIO

1: Port set to analog input port

3.1.24 R1A1/P6ADE(P6 analog port enable register)

0X1A1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6ADE	P6ADE <7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

P6 port ADC channel selection control bit:

0: Port is set to GPIO

1: Port set to analog input port

3.1.25 R1A3 /ADATH(ADC data High 8-bit register)

0X1A3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATH	ADAT<11:4>							
Read/write	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit<7:0> : ADAT<11:4>-AD conversion result is 8 bits higher

3.1.26 R1A4 /ADATL(ADC data low 8 bit register)

0X1A4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATL	ADAT<7:0>							
Read/write	R	R	R	R	R	R	R	R
Reset values	X	X	X	X	X	X	X	X

Bit<7:0> : ADAT<7:0>-AD converts the result to the lower 8 bits

3.1.27 R1A5 /ADIS(ADC channel selection and ADC data high 4-bit register)

0X1A5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADIS	ADIS<3:0>				ADAT<11:8>			
Read/write	R/W	R/W	R/W	R/W	R	R	R	R
Reset values	0	0	0	0	X	X	X	X

Bit<7:4> : ADIS<3:0>-AD input port selection

ADIS3	ADIS2	ADIS1	ADIS0	Channel selection
0	0	0	0	AD0/P50
0	0	0	1	AD1/P51
0	0	1	0	AD2/P52

0	0	1	1	AD3/P53
0	1	0	0	AD4/P54
0	1	0	1	AD5/P55
0	1	1	0	AD6/P60
0	1	1	1	AD7/P61
1	0	0	0	AD8/P62
1	0	0	1	AD9/P63
1	0	1	0	AD10/P64
1	0	1	1	AD11/P65
1	1	0	0	AD12/P66
1	1	0	1	AD13/P67
1	1	1	0	AD14/ built-in voltage
1	1	1	1	Channel testing

Notes:

1. When AD14 chooses built-in reference voltage, VREFS=0 is the internal voltage reference, VREFS=1 is the external voltage reference;
2. The channel test option is used for factory test, and users should avoid operating this option;
3, the port as the analog input port will prohibit other IO port functions including input, output, pull up, pull down and other multiplexing functions.

Bit<3:0> : ADAT<11:8>-AD conversion result is 4 bits higher

3.1.28 R1A6 /ADCON0(ADC control register 0)

0X1A6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON0	ADPSR<1:0>		-	-	-	VREF<2:0>		
Read/write	R/W	R/W	R	R	R	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:6> : ADPSR<1:0>-ADC clock divider selection (Fosc is system clock frequency)

ADPSR<1>	ADPSR<0>	ADC clock
0	0	Fosc/16
0	1	Fosc/4
1	0	Fosc/64
1	1	Fosc/1

Bit<5:3> : Unused

Bit<2:0> : VREF<2:0>- Internal reference voltage selection

VREF<2>	VREF<1>	VREF<0>	Internal reference voltage
0	0	0	VDD
0	0	1	4V
0	1	0	3V
0	1	1	2V

1	0	0	1.5 V

3.1.29 R1A7 /ADCON1(ADC control register 1)

0X1A7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON1	ADRUN	ADEN	VREFS	CALI	SIGN	VOF<2:0>		
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : ADRUN

1: ADC starts sampling

0: ADC no sampling or end of sampling

Bit<6> : ADEN

1: ADC enabled

0: ADC disabled (Turn off ADC in sleep mode, otherwise there is power consumption)

Bit<5> : VREFS

1: ADC uses external reference voltage (P61 port)

0: ADC uses internal reference voltage

Bit<4> : CALI

1: ADC tuning 0 calibration enabled

0: ADC 0-tuned calibration is forbidden

Bit<3> : SIGN

1: ADC to 0 positive polarity

0: ADC is tuned to 0 negative polarity

Bit<2:0> : VOF<2:0>- ADC zero calibration bit

VOF<2>	VOF<1>	VOF<0>	Calibration range
0	0	0	0 LSB
0	0	1	2 LSB
0	1	0	4 LSB
0	1	1	6 LSB
1	0	0	8 LSB
1	0	1	10 LSB
1	1	0	12 LSB
1	1	1	14 LSB

3.1.30 R1AF /WDTCON(WDT, external interrupt, internal reference control register)

0X1AF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	INT0EN	INT1EN	VFOE	INT1EDG	INT0EDG	-	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Reset values	1	0	0	0	0	0	0	0

Bit<7>：WDTE-WDT enable control

1: Enable

0: Forbid

Bit<6> : INT0EN-P60 external interrupt enable bit

1: Enable, P60 is the input port, optional along trigger

0: Forbidden, P60 is GPIO, INT0 channel is blocked

Bit<5> : INT1EN-P53 external interrupt enable bit

1: Enable, P53 is the input port, optional along trigger

0: Forbidden, P53 is GPIO, INT1 channel is blocked

Bit<4> : VFOE- Internal benchmark output

1: Internal reference voltage output enabled, P65 as analog port, the output voltage is selected according to VREF< 2:0 >

0: Internal reference voltage output forbidden, P65 as ordinary IO

Bit<3> : INT1EDG-P53 external interrupt triggers along selection

1: Rising edge trigger

0: Falling edge trigger

Bit<2> : INT0EDG-P60 External interrupt trigger edge selection

1: Rising edge trigger

0: Falling edge trigger

Bit<1:0> : Unused

3.1.31 R1B0 /TC1CON(TC1 control register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	IPWM3E	PWM3E	IPWM1E	PWM1E	TC1PSR<2:0>		
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : TC1EN-PWM1/3 timer enable bit

0: Forbidden

1: enabling (when used alone timer function can still need to make PWM1E /PWM3E / IPWM1E/ PWM3E in any one)

Bit<6> : IPWM3E-IPWM3 output enable bit

0: IPWM3 forbidden

1: IPWM3 enabled

Bit<5> : PWM3E-PWM3 output enable bit

0: PWM3 forbidden

1: PWM3 enabled

Bit<4> : IPWM1E-IPWM1 output enable bit

0: IPWM1 forbidden

1: IPWM1 enabled

Bit<3> : PWM1E-PWM1 output enable bit

0: PWM1 disabled

1: PWM1 enabled

Bit<2:0> : TC1PSR<2:0>-TC1 clock divider selection

TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	TC1 frequency
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.32 R1B1 /TC1PRDL(TC1/PWM cycle low 8-bit register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM3) cycle 8 bits lower

3.1.33 R1B2 /PWM1DTL(PWM1 low duty cycle 8-bit register)

0X1B2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DTL	PWM1DT<7:0>							

Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

PWM1 duty cycle is 8 bits lower

3.1.34 R1B3 /TC1PRDTH(2 bits higher cycle for TC1/PWM and 2 bits higher duty cycle for PWM1)

0X1B3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD <9:8>		-	-	PWM1DT<9:8>		-	-
Read/Write	R/W	R/W	R	R	R/W	R/W	R	R
Reset values	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM3) cycle 2 bit higher and PWM1 duty cycle 2 bit higher

3.1.35 R1B4/TC1CH(TC1 count 2 bits higher register)

0X1B4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CH	-	-	-	-	-	-	TC1C<9:8>	
Reading/writing	R	R	R	R	R	R	R	R
Reset values	0	0	0	0	0	0	0	0

The TC1 timer count is 2 bits high

3.1.36 R1B5/TC1CL(TC1 count low 8-bit register)

0X1B5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CL	TC1C<7:0>							
Read/write	R	R	R	R	R	R	R	R
Reset values	0	0	0	0	0	0	0	1

The TC1 timer count is 8 bits lower

3.1.37 R1B6/TC2CON(TC2 control register)

0X1B6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	IPWM4E	PWM4E	IPWM2E	PWM2E	TC2PSR<2:0>		
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : TC2EN-PWM2/4 timer enable bit

0: Forbidden

1: enabling (when used alone timer function can still need to make PWM2E/PWM4E/IPWM2E/IPWM4E in any one)

Bit<6> : IPWM4E-IPWM4 output enable bit

0: IPWM4 forbidden

1: IPWM4 enabled

Bit<5> : PWM4E-PWM4 output enable bit

0: PWM4 is forbidden

1: PWM4 enabled

Bit<4> : IPWM2E-IPWM2 output enable bit

0: IPWM2 forbidden

1: IPWM2 enabled

Bit<3> : PWM2E-PWM2 output enable bit

0: PWM2 disabled

1: PWM2 enabled

Bit<2:0> : TC2PSR<2:0>-TC2 clock divider selection

TC2PSR2<2>	TC2PSR<1>	TC2PSR<0>	TC2 frequency
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

3.1.38 R1B7 /TC2PRDL(TC2/PWM cycle low 8-bit register)

0X1B7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

TC2 (PWM2, PWM4) cycle 8 bits lower

3.1.39 R1B8 /PWM2DTL(PWM2 duty cycle lower 8 bit register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2DTL	PWM2DT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

PWM2 duty cycle is 8 bits lower

3.1.40 R1B9 /TC2PRDTH(TC2/PWM cycle 2 bit higher and PWM2 duty cycle 2 bit higher register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD<9:8>		-	-	PWM2DT<9:8>		-	-
Read/Write	R/W	R/W	R	R	R/W	R/W	R	R
Reset values	0	0	0	0	0	0	0	0

TC2 (PWM2, PWM4) cycle 2 bit higher and PWM2 duty cycle 2 bit higher

3.1.41 R1BA /TC2CH(TC2 count 2 bits higher register)

0X1BA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CH	-	-	-	-	-	-	TC2C<9:8>	
Read/write	R	R	R	R	R	R	R	R
Reset values	0	0	0	0	0	0	0	0

The TC2 timer count is 2 bits high

3.1.42 R1BB /TC2CL(TC2 count low 8-bit register)

0X1BB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CL	TC2C<7:0>							
Read/write	R	R	R	R	R	R	R	R
Reset values	0	0	0	0	0	0	0	1

The TC2 timer count is 8 bits lower

3.1.43 R1BC/PWM3DTH(PWM3 duty cycle 2 bit higher register)

0X1BC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM3DTH	-	-	-	-	-	-	PWM3DT <9:8>	
Read/write	R	R	R	R	R	R	R/W	R/W

Reset value	0	0	0	0	0	0	0	0

PWM3 duty cycle is 2 bits higher

3.1.44 R1BD /PWM3DTL(PWM3 low duty cycle 8-bit register)

0X1BD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM3DTL	PWM3DT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

PWM3 duty cycle is 8 bits lower

3.1.45 R1BE /PWM4DTH(PWM4 duty cycle 2 bit higher register)

0X1BE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM4DTH	-	-	-	-	-	-	PWM4DT <9:8>	
Read/write	R	R	R	R	R	R	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

PWM4 duty cycle is 2 bits higher

3.1.46 R1BF /PWM4DTL(PWM4 duty cycle low 8-bit register)

0X1BF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM4DTL	PWM4DT<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

PWM4 duty cycle is 8 bits lower

3.1.47 R1C6 /PWMIS(PWM port Map control register)

0X1C6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMIS	IPWM4S	PWM4S	IPWM3S	PWM3S	IPWM2S	PWM2S	IPWM1S	PWM1S
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : IPWM4S-IPWM4 port mapping selection

0: Select P51 port output

1: Select P62 port output

Bit<6> : PWM4S-PWM4 port mapping selection

0: Select P63 port output

1: Select P55 port output

Bit<5> : IPWM3S-IPWM3 port mapping selection

0: Select P50 port output

1: Select P61 port output

Bit<4> : PWM3S-PWM3 port map selection

0: Select P62 port output

1: Select P54 port output

Bit<3> : IPWM2S-IPWM2 port mapping selection

0: Select P67 port output

1: Select P65 port output

Bit<2> : PWM2S-PWM2 port mapping selection

0: Select P61 port output

1: Select P53 port output

Bit<1> : IPWM1S-IPWM1 port mapping selection

0: Select P66 port output

1: Select P64 port output

Bit<0> : PWM1S-PWM1 port map selection

0: Select P60 port output

1: Select P52 port output

3.1.48 R1C7 /DEADCON(Dead zone control register)

0X1C7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DEADCON	DEADT1E	DEADT0E	DEAD1_SEL	DEAD0_SEL	DEAD1PSR<1:0>		DEAD0PSR<1:0>	
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : DEADT1E-PWM2/4 deadzone adjustment enable control bit

0: Forbidden

1: Enable

Bit<6> : DEADT0E-PWM1/3 dead zone adjustment enable control bit

0: Forbidden

1: Enable

Bit<5> : DEAD1_SEL-PWM2/4 Dead zone selection control bit

0: Select PWM2 to use dead-zone function

1: Select PWM4 to use the dead zone function

Bit<4> : DEAD0_SEL-PWM1/3 dead select control bit

0: Select PWM1 to use dead-zone function

1: Select PWM3 to use the dead zone function

Bit<3:2> : DEAD1PSR<1:0>-DEAD1 clock divider selection

DEAD1PSR<1>	DEAD1PSR<0>	DEAD1 division ratio
0	0	1:1
0	1	1:2
1	0	1:4
1	1	1:8

Bit<1:0> : DEAD0PSR<1:0>-DEAD0 clock divider selection

DEAD0PSR<1>	DEAD0PSR<0>	DEAD0 split frequency ratio
0	0	1:1
0	1	1:2
1	0	1:4
1	1	1:8

3.1.49 R1C8 /PWMCON(PWM control register)

0X1C8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON	PWMCAS	PWMCKS	-	-	INV2H	INV2L	INV1H	INV1L
Read/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : PWMCAS-PWM1/2 cascade enable bit

0: Forbidden

1: Enable (PWM1 and PWM2 cascade for 20bitsPWM)

Bit<6> : PWMCKS-PWM clock selection control bit

0: The instruction clock

1: System clock

Bit<5:4> : Unused

Bit<3> : INV2H-PWM2/4 takes the reverse control bit

0: No negation

1: Negate (PWM2/4 determined by DEAD2_SEL bit)

Bit<2> : INV2L-IPWM2/4 Take the reverse control bit

0: No negation

1: Negate (determined by the DEAD2_SEL bit IPWM2/4)

Bit<1> : INV1H-PWM1/3 takes the reverse control bit

0: No negation

1: Negate (PWM1/3 determined by DEAD1_SEL bit)

Bit<0> : INV1L-IPWM1/3 takes the reverse control bit

0: No negation

1: Negate (IPWM1/3 determined by DEAD1_SEL bit)

3.1.50 R1C9 /DEADT0(dead time control register 0)

0X1C9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DEADT0	DEADT0<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

3.1.51 R1CA /DEADT1(dead time control register 1)

0X1CA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DEADT1	DEADT1<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

3.1.52 R1D6 /INTE0(Interrupt enable control register 0)

0X1D6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE0	-	-	ADIE	EX1IE	EX0IE	P6ICIE	P5ICIE	TC0IE
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : Unused

Bit<6> : Unused

Bit<5> : ADIE - AD interrupt enable bit

0: forbidden

1: Enable

Bit<4> : EX1IE - INT1 Interrupt the enable bit

0: Disable

1: Enable

Bit<3> : EX0IE -- INT0 Interrupt the enable bit

0: Disable

1: Enable

Bit<2> : P6ICIE - P6IC interrupt enable bit

0: Forbidden

1: Enable

Bit<1> : P5ICIE - P5IC interrupt enable bit

0: Forbidden

1: Enable

Bit<0> : TC0IE - TC0 interrupt enable bit

0: Forbidden

1: Enable

3.1.53 R1D7/INTE1(Interrupt enable control register 1)

0X1D7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE1	-	-	DT4IE	DT3IE	DT2IE	DT1IE	TC2IE	TC1IE
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : Unused

Bit<6> : Unused

Bit<5> : DT4IE - DT4 interrupt enable bit

0: Disable

1: Enable

Bit<4> : DT3IE - DT3 interrupt enable bit

0: Forbidden

1: Enable

Bit<3> : DT2IE - DT2 interrupt enable bit

0: Forbidden

1: Enable

Bit<2> : DT1IE - DT1 interrupt enable bit

0: Forbidden

1: Enable

Bit<1> : TC2IE - TC2 interrupt enable bit

0: Forbidden

1: Enable

Bit<0> : TC1IE - TC1 interrupt enable bit

0: Forbidden

1: Enable

3.1.54 R1DA/INTF0(Interrupt flag register 0)

0X1DA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF0	-	-	ADIF	EX1IF	EX0IF	P6ICIF	P5ICIF	TC0IF
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : Unused

Bit<6> : Unused

Bit<5> : ADIF - ADC interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<4> : EX1IF -int1 interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<3> : EX0IF -int0 interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<2> : P6ICIF - P6IC interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<1> : P5ICIF - P5IC interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<0> : TC0IF - TC0 interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

3.1.55 R1DB /INTF1(Interrupt flag register 1)

0X1DB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF1	-	-	DT4IF	DT3IF	DT2IF	DT1IF	TC2IF	TC1IF
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : Unused

Bit<6> : Unused

Bit<5> : DT4IF-DT4 interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<4> : DT3IF-DT3 interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<3> : DT2IF -DT2 interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<2> : DT1IF -DT1 interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<1> : TC2IF -tc2 interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

Bit<0> : TC1IF -tc1 interrupt flag bit

0: No interrupt was triggered

1: Interrupt triggered

3.1.56 R1FF /IAR(Indirect addressing register)

0X1FF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAR	IAR<7:0>							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	X	X	X	X	X	X	X	X

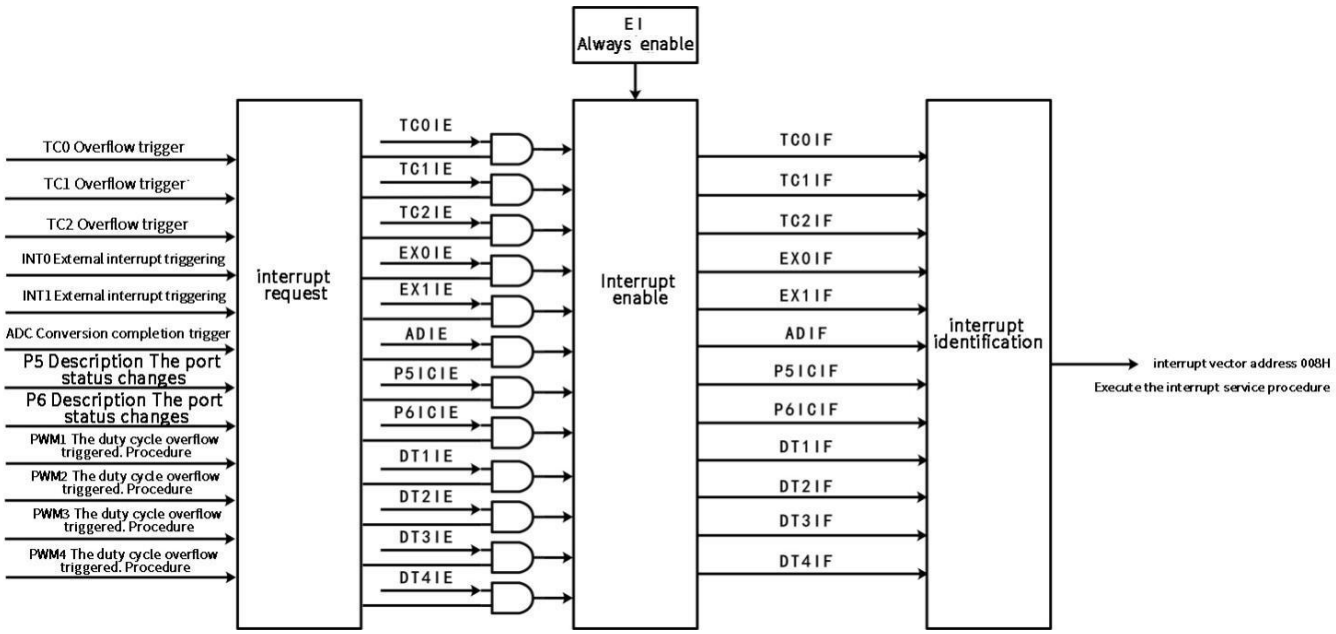
The indirection addressing register is not an actual register, its main function is to act as a pointer to indirection addressing. Any instruction that has R1FF as a pointer actually corresponds to the data pointed to by R180 (RAM select register) RSR<6:0>.

3.2 Interrupts

The JZ8P2615 has 12 interrupt sources, whichever interrupt is used must enable the total interrupt, that is, the "EI" instruction. The interrupt vector address is fixed to 008H. Here are the characteristics of each interrupt, respectively:

Interrupt source	Enabling condition	Interrupt flag
TC0 overflow interrupt	EI + TC0IE=1	TC0IF
TC1 overflow interrupt	EI + TC1IE=1	TC1IF
TC2 overflow interrupt	EI + TC2IE=1	TC2IF
INT0 External interrupt	EI + EX0IE=1	EX0IF
INT1 External interrupt	EI + EX1IE=1	EX1IF
ADC conversion completion	EI + ADIE=1	ADIF
P5 port input change interrupt	EI + P5ICIE=1	P5ICIF
P6 Port input change interrupt	EI + P6ICIE=1	P6ICIF
PWM1 duty cycle overflow	EI + DT1IE=1	DT1IF
PWM2 duty cycle overflow	EI + DT2IE=1	DT2IF
PWM3 duty cycle overflow	EI + DT3IE=1	DT3IF
PWM4 duty cycle overflow	EI + DT4IE=1	DT4IF

R1DA/R1DB are interrupt flag registers that record the interrupt bit when an interrupt request is generated. R1D6/R1D7 are interrupt enable control registers in which interrupt permission and disallow are set. The total interrupt is allowed by the "EI" instruction, on the contrary, the total interrupt is forbidden by the "DI" instruction. When an interrupt is generated, the execution of its next instruction will be performed from the interrupt vector address 008H. The corresponding interrupt flag must be reset before leaving the interrupt service routine, so that the wrong action of the interrupt can be avoided.



Schematic diagram of interrupt principle

3.2.1 Interruption site protection

In the process of responding to an interrupt, the hardware has an interrupt protection function, which saves the contents of ACC, R183 and R180 until it leaves the interrupt service routine, and then reloads the saved values into ACC, R183 and R180. This is to avoid that when the interrupt subroutine is executed, the contents of ACC, R183 and R180 will be saved. An instruction will change the value of ACC, R183, R180, resulting in an error when returning to the main program. This is shown below:

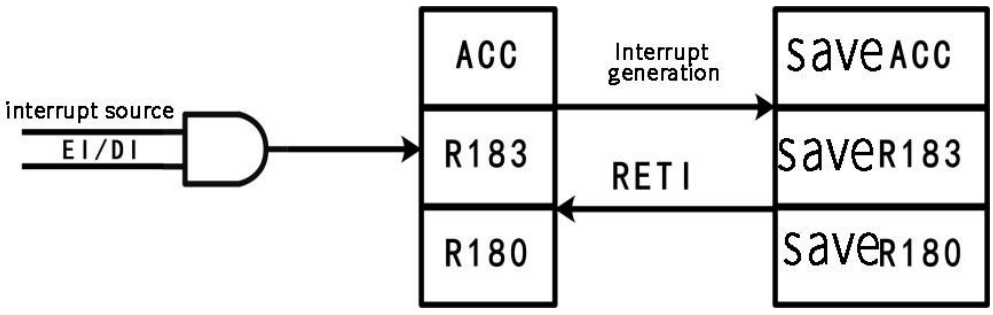


Diagram of the interruption site protection

3.3 Reset

3.3.1 Overview of reset function

The JZ8P2615 system provides four reset methods:

- POR Power on reset
- RESET foot input low reset
- WDT Watchdog overflow reset
- LVR low voltage reset

When any of the above reset occurs, all system registers are initialized to the reset value, the program stops running, and the program counter PC is reset. After the reset, the system starts running again from the vector 0000H.

Any reset situation requires a certain response time, and the system reset mechanism can ensure a reliable reset of the MCU. Different types of oscillators require different time to complete reset. Therefore, the rising rate of VDD and the starting time of different oscillators are not fixed. The RC oscillator has the shortest onset time, while the crystal oscillator has a longer onset time. In the process of using the user terminal, attention should be paid to the requirements of the application scene for power on and reset time.

3.3.2 POR Power-on reset

Power on reset is closely related to LVR operation. The power-on process of the system is in the form of a gradually rising curve, and it takes a certain time to reach the normal level value.

- Power on: The system detects a rise in the supply voltage and waits for it to stabilize;
- System initialization: all system registers are set to their initial values;
- Oscillator starts working: the oscillator starts to supply the system clock;
- Execute the program: the power on ends, and the program starts to run;

The power-on reset time is determined by the [Reset Time] selection in the OPTION, as shown in the following table:

PWRT and WDT	Reset setup time
PWRT=WDT	4.5ms(follow watchdog reset time)
PWRT=WDT	18ms(follow watchdog reset time)

PWRT=WDT	72ms(follow watchdog reset time)
PWRT=WDT	288ms(follow watchdog reset time)
PWRT≠WDT	140us(independent fixed reset time)

3.3.3 WDT watchdog reset

The watchdog reset is a protective setting for the system. In the normal state, the watchdog timer is reset by the program. If an error occurs, the system is in an unknown state, the watchdog timer overflows, and the system is reset. After the watchdog is reset, the system is restarted into a normal state.

- Watchdog timer state: The system detects whether the watchdog timer is overflowing, if it is overflowing, the system is reset;
- System initialization: all system registers are set to their initial default values;
- Oscillator starts to work: the oscillator starts to provide the system clock;
- Execute the program: the power on ends, and the program starts to run;

Instructions for the watchdog to wake up:

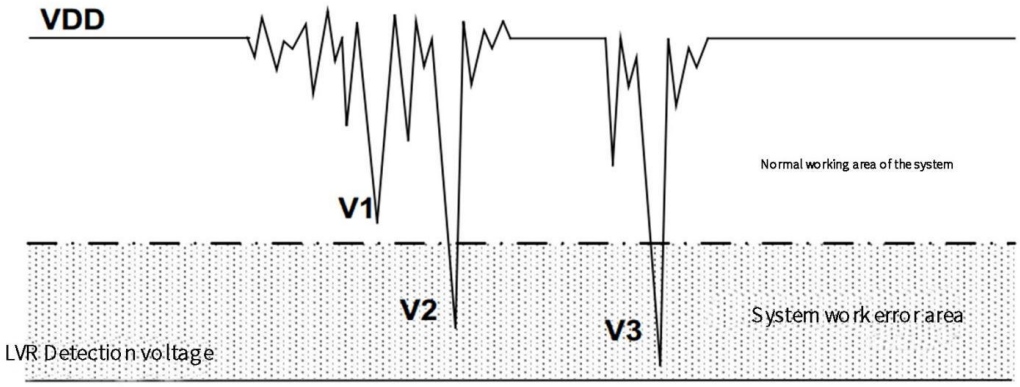
The watchdog reset can be reset in idle mode and sleep mode. After the system reset, the program is executed from the address 0X00. The user can judge the time overflow bit of R183 (STATUS) register Bit4, if it is WDT overflow, it can be judged as a watchdog reset, and the corresponding wake-up subroutine is executed. Note that the watchdog wakeup is actually a special application of watchdog reset.

Notes on application of Watchdog Timer:

- Before the watchdog reset, check the I/O port status and RAM can enhance the reliability of the program;
- Do not reset the watchdog in an interrupt, otherwise the main program running cannot be detected;
- The program should only clear the watchdog once in the main program. This structure can maximize the protection function of the watchdog.

3.3.4 LVR low voltage reset

Power down reset is aimed at the system voltage sag caused by external factors (e.g., interference or external load changes). Power down may cause abnormal system working status or program execution errors.



The voltage sag may enter the system dead zone. System dead zone means that the power supply does not meet the minimum operating voltage requirements of the system. The figure above is a schematic of a typical power-down reset. In this picture, the VDD is severely disturbed and the voltage drop is very low. Above the dotted line, the system works normally. Below the dotted line, the system enters an unknown operating state. This region is called the dead zone. When VDD drops to V1, the system is still in a normal state; When VDD falls to V2 and V3, the system enters the dead zone, which is prone to errors. The system may enter the dead zone if:

DC in use:

Battery power supply is generally used in DC application. When the battery voltage is too low or the microcontroller drives the load, the system voltage may drop and enter the dead zone. At this time, the power supply will not further drop to the LVR detection voltage, so the system remains in the dead zone.

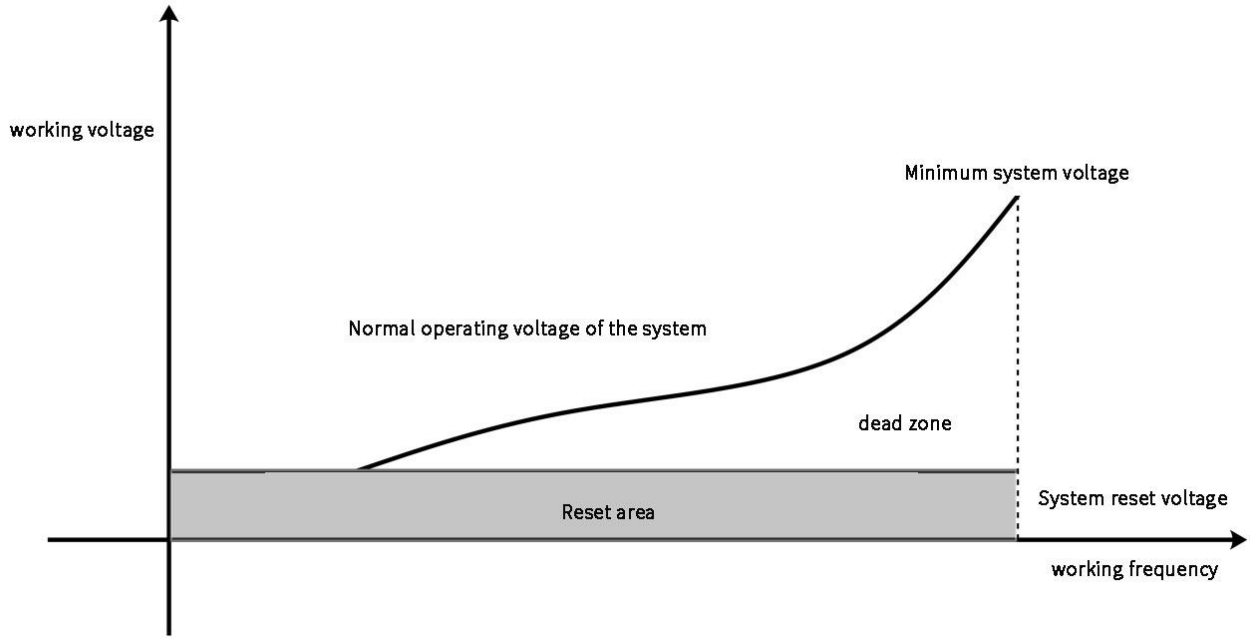
In AC operation:

When the system uses AC power supply, the DC voltage value is affected by the noise in the AC power supply. When the external load is too high, such as when driving the motor, the interference caused by the load action also affects the DC power supply. If the VDD falls below the minimum operating voltage due to interference, the system will likely enter an unstable working state. In the AC application, the system power on and power off time are long. Among them, the

power on timing protection makes the system power on normally, but the power down process is similar to the situation in the DC application. After the AC power is turned off, the VDD voltage is easy to enter the dead zone in the process of slow decline.

3.3.5 Relationship between working frequency and LVR low voltage detection

In order to improve the performance of the system power down reset, first of all, the minimum operating voltage value of the system must be clarified. The minimum operating voltage of the system is related to the execution speed of the system, and the minimum operating voltage value is different under different execution speed.



As shown in the figure above, the system normal operating voltage region is generally higher than the system reset voltage, and the reset voltage is determined by the low voltage detection (LVR) level. When the system execution speed increases, the minimum operating voltage of the system also increases accordingly. However, since the system reset voltage is fixed, there will be a voltage region between the minimum operating voltage of the system and the system reset voltage. The system will not work properly and will not reset, and this region is called dead zone.

In order to avoid the occurrence of dead zone voltage, when selecting the working frequency, the corresponding LVR reset voltage point should be selected. The following table:

IRC Frequency	Oscillator frequency multiplier	Clocks frequency division	LVR reset voltage point
IRC-8MHz	Frequency doubling	2 Clocks	As = 2.4 V

IRC-8MHz	Not octave	2 Clocks	As = 1.8 V
IRC-1MHz	Frequency doubling	2 Clocks	As = 1.6 V
IRC-1MHz	Not octave	2 Clocks	As = 1.6 V

Note: 1, working frequency = instruction cycle frequency =IRC frequency + Clocks frequency; 2, this working frequency and the corresponding value of the LVR reset voltage point, only recommended value, the user in the use of the process, according to the specific application can be adjusted reset voltage point.

3.4 Working mode

The JZ8P2615 can operate at different clock frequencies in four operating modes, which can control the operation of the oscillator, the execution of the program, and the functional loss of the analog circuit.

- High speed mode: the system clock selects the internal high speed clock, the low speed clock works normally;
- Low-speed mode: the system clock selects the internal low-speed clock, and the high-speed clock stops working.
- Idle mode: the system clock works normally, other parts of the system go to sleep (TC0, TC1 and TC2 select the system clock to continue to work and wake up the system), and can also be woked up by P5IWE, P6IWE, INT0WE, INT1WE, ADCWE;
- Sleep mode: all functions stop working, the system goes to sleep, can be awakened by TC0 (P62 input clock), P5IWE, P6IWE, INT0WE, INT1WE;

Function module	High speed mode	Low Speed mode	Idle mode	Sleep mode
IHRC	Run	Stop	Run	Stop
ILRC	Run	Run	Run	Stop
CPU	Execution	Execution	Stop	Stop
TC0	Working	Workable	Workable	Working (P62 input clock)
TC1	Workable	Workable	Workable	Stop
TC2	Workable	Workable	Workable	Stop
Interruption	All valid	All valid	All valid (TC0,TC1,TC2 select system clock)	TC0IE,P5ICIE,P6ICIE,EX0IE,EX1IE
Wakeup function	-	-	(TC0,TC1,TC2 select system clock to wake up)P5IWE,P6IWE,INT0WE, INT1WE,ADCWE	TC0WE,P5IWE,P6IWE, INT0WE,INT1WE
Watchdog	WDT option	WDT Option	WDT Option control	WDT Option control

3.4.1 High Speed mode

High-speed mode is the system high-speed clock operation mode, and the system clock source is provided by the high-speed RC oscillator. The program is executed. After a power-on reset or either reset is triggered, the system goes into high speed mode to execute the program. In the high-speed mode, the high-speed oscillator works normally and consumes the most power.

◆ The program is executed and all functions can be controlled;

- The system rate is high;
- Both the high speed oscillator and the internal low speed oscillator work normally;
- High speed mode can be switched to low speed mode;
- Enter from high-speed mode to sleep mode, wake up and return to high-speed mode;
- Enter from high-speed mode to idle mode, wake up and return to high-speed mode;

3.4.2 Low speed mode

Low speed mode is the system low speed clock operation mode. The system clock source is provided by the low-speed RC oscillator. The low-speed mode is controlled by the CLKMD bit of the CPU mode control register. When CLKMD=0, the system is in high speed mode; When CLKMD=1, the system enters the low speed mode. After entering the low speed mode, the system cannot automatically disable the high speed RC oscillator and must disable it by SPTHX=1 to reduce power consumption.

- The program is executed and all functions can be controlled;
- The system rate is low;
- The internal low-speed oscillator works normally, and the high-speed oscillator stops working.
- Low speed mode can be switched to high speed mode;
- Enter from low speed mode to sleep mode, wake up and return to low speed mode;
- Enter from low speed mode to idle mode, wake up and return to low speed mode;

3.4.3 Idle mode

Idle mode is another ideal state. In sleep mode, all functions and hardware devices are disabled, but in idle mode, the system clock is kept working and the power consumption in idle mode is greater than that in sleep mode. In idle mode, no program is executed, but the TC0, TC1, TC2, P5IWE, P6IWE, INT0WE, INT1WE, ADCWE with wake-up function still work normally, and the clock source of timers TC0, TC1 and TC2 is the system clock that is still working. Whether to enter the IDLE mode is decided by the IDLE bit of the system clock and the status control register. When IDLE=1, the program will enter the idle mode after executing SLEEP.

- The program stops executing, and all functions are forbidden;
- Modules with wakeup function work properly;

- The system clock works properly;
- Enter from high-speed mode to idle mode, and return to high-speed mode after being woken up;
- Enter from low speed mode to idle mode, return to low speed mode after waking up;
- The wakeup mode in idle mode is P5IWE, P6IWE, INT0WE, INT1WE, ADCWE;
- The functions of TC0, TC1 and TC2 are still valid in idle mode;

3.4.4 Sleep mode

Sleep mode is the ideal state for the system, where the program is not executed and the oscillator stops working. The power consumption of the whole chip is below 1uA. Sleep mode can be woked up by TC0 (P62 input clock), P5IWE, P6IWE, INT0WE, INT1WE. Enter sleep mode from high speed mode or low speed mode, and return to the corresponding mode after being woken up. The system clock and the IDLE bit of the status control register control whether to enter the SLEEP mode. When IDLE=0, the execution of sleep will enter the sleep mode.

- The program stops executing, and all functions are forbidden;
- All oscillators, including the external high speed oscillator, the internal high speed oscillator and the internal low speed oscillator are stopped working;
- Power consumption below 1uA;
- Enter from high speed mode to sleep mode, and return to high speed mode after waking up;
- Enter into sleep mode from low speed mode, return to low speed mode after waking up;
- The wake-up mode in sleep mode is TC0 (P62 input clock), P5IWE, P6IWE, INT0WE, INT1WE;

3.5 System clock

JZ8P2615 is integrated with two kinds of oscillators, high speed RC oscillator IHRC and low speed RC oscillator ILRC. The system clock can be switched between high and low speed oscillators by R188/CPUCON register.

3.5.1 Internal RC oscillator

The JZ8P2615 provides an internal IHRC frequency configurable function with a default frequency of 4MHz.

The internal IHRC oscillator contains six frequency values of 1M/3.4M/4.8M/5.4M/6M/8M Hz. By setting the configuration bit of the OPTION, the IHRC operating frequency can be selected, and the following is their corresponding relationship:

RCM	IRC frequency
1M	The IHRC frequency is chosen to
3.4 M	The IHRC frequency is chosen to
4.8 M	The IHRC frequency is chosen to
5.4 M	The IHRC frequency is chosen to
6M	The IHRC frequency is chosen to
8M	The IHRC frequency is chosen to

JZ8P2615 provides a variety of frequency division options, can be selected in the OPTION, suitable for more occasions. The following table:

Clocks	Clocks frequency division
2clock	Frequency division is 2clock
4clock	The frequency division is 4clock
8clock	The frequency division is 8clock
16clock	The frequency division is 16clock
32clock	Frequency division is 32clock

3.6 I/O ports

JZ8P2615 has 2 groups of bidirectional I/O ports, 14 inputs and 14 outputs in total, most of the I/O can be reused for other functions.

14 programmable pull-up I/O pins: P50 to P55, P60 to P67;

14 programmable pull-down I/O pins: P50 to P55, P60 to P67;

14 optionally selectable drive enhanced I/O pins: P50 to P55, P60 to P67 (P63 pull current boost not available);

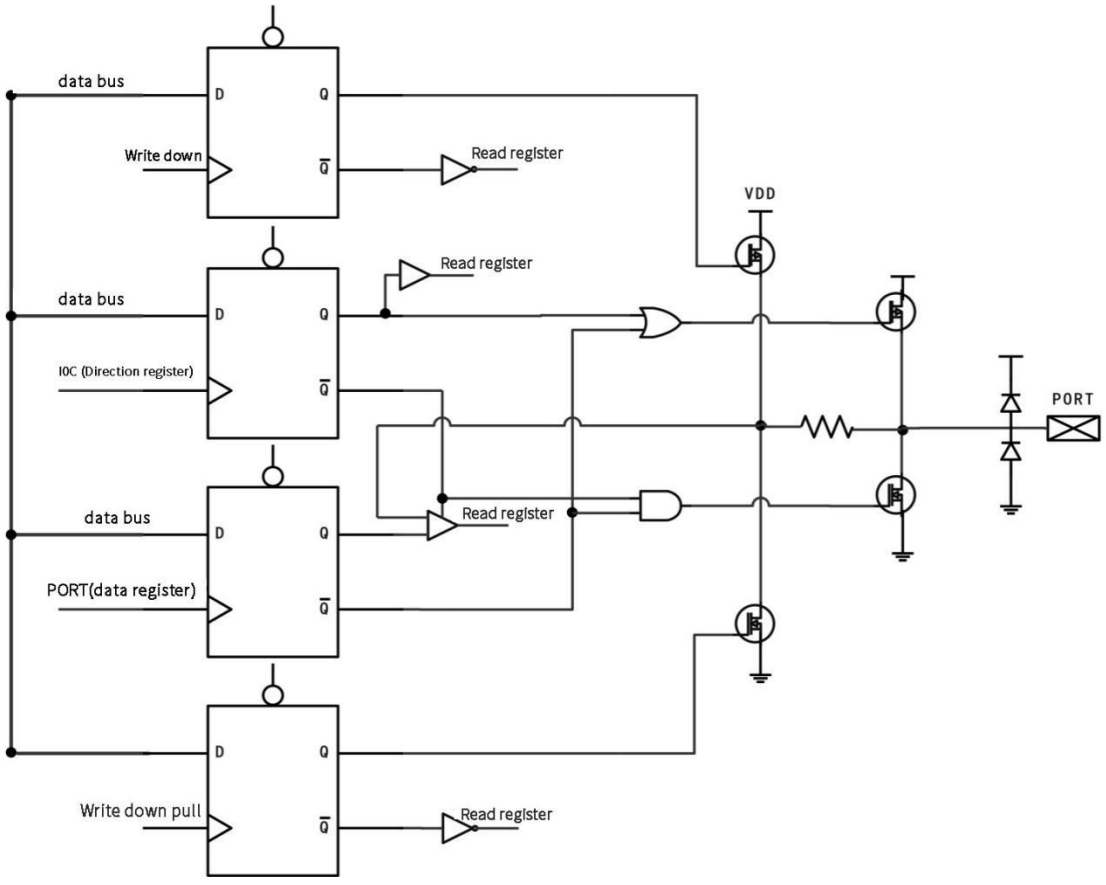
14 programmable wake-up I/O pins: P50 to P55, P60 to P67;

8 programmable weak drive I/O pins: P60 to P67;

8 programmable open-drain I/O pins: P60 to P67;

3.6.1 GPIO internal structure diagram

The following internal structure diagram is for reference only and does not represent the actual circuit.



IO control register/data register/pull-up/pull-down structure circuit

3.6.2 Port input change wake-up

The JZ8P2615 contains 14 programmable ports for input change wake-up I/ OS: P50 to P55, P60 to P67. The chip can enter the SLEEP mode or idle mode by executing the "sleep" command. At this point, the CPU does not execute instructions. The port input change can be woken up by the program to continue the original process (execute DI before SLEEP) or execute the corresponding jump (execute EI before SLEEP), and the corresponding interrupt enable control needs to be opened. After the port input change wakes up, it jumps to the interrupt service program.

Port state change query mode Wakeup Settings:

1. Port input changes and wake-up port is set as input;

2. The internal pull up or pull down of the wake up port can be selected according to the need;

3, enable port input change wake-up control P5IWE/P6IWE;

Execute DI instruction, do not enter the interrupt address port;

Execute "SLEEP" instruction, IDLE=0 enter sleep mode or IDLE=1 enter idle mode;

6. After waking up, execute the next command of SLEEP;

Port state change interrupt mode wake up Settings:

1. Port input change wake-up port is set as input;

2. The internal pull up or pull down of the wake up port can be selected according to the need;

3, enable port input change wake-up control P5IWE/P6IWE;

4, enable port input change interrupt P5ICIE/P6ICIE;

Execute "EI" instruction and wait to enter the interrupt address port;

Execute "SLEEP" instruction, IDLE=0 enter sleep mode or IDLE=1 enter idle mode;

7, after waking up, it will enter the interrupt address port, exit the interrupt, execute the next instruction SLEEP;

3.6.3 Port Schmidt parameter

The Schmidt characteristics of the JZ8P2615 port are tabulated as follows (for reference only) :

Ports	SMT	
P50 to P55	0.25 * VDD	0.5 * VDD
P60 ~ P62	0.25 * VDD	0.5 * VDD
P63	0.5 * VDD	0.5 * VDD
P64 to P67	0.25 * VDD	0.5 * VDD

The above parameters are for reference only, please refer to the measured data of the target prototype.

3.7 Timing counter

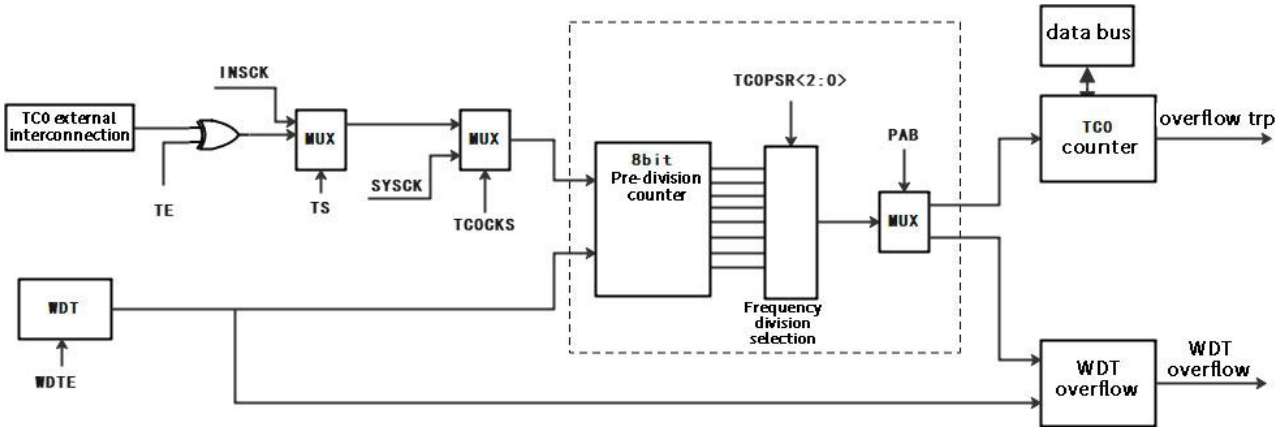
3.7.1 TC0 timing counter

The JZ8P2615 provides an 8-bit timing counter as a pre-divider for TC0 and WDT. The predivider is used only for TC0 or only for WDT at the same time, and the PAB bit of the TC0CON register determines the frequency division of the predivider, and the TC0PSR<2:0> three bits determine the predivision ratio. In the TC0 mode each time the TC0C is written a value, the pre-division register is reset. When the predivider is assigned to WDT mode, the values of the WDT and predivider registers are reset when the "CWDT" or "SLEEP" instruction is executed. If the predivider is assigned to the TCC first and then to the WDT, the contents of the predivider counter will be automatically cleared, and vice versa.

TC0 is an 8Bit uplink counter that works whenever there is a clock. The clock source can be either an internal instruction clock, a system clock, or optionally an external clock (input by pin P62, trigger edge optional), and the clock arrival counter is implemented by adding 1.

TC0 count overflow can form an interrupt signal.

In the IDLE mode, the TC0 interrupt can wake up the circuit, after waking up, you can choose to interrupt or continue to execute the original program, the method refers to the port input change to wake up. In sleep mode, TC0 is set to P62 external input clock to interrupt the overflow and wake up the circuit.



Block diagram of TC0 structure

3.7.1.1 TC0 timing setup instructions

1. Assign the initial value to the TC0C register;

2, set the value of the TC0CON register (select the clock source and pre-frequency ratio);

3, used as a counter, need to select the TC0 signal source in the TC0CON register as an external input signal;

If you need to execute the interrupt function, you must set the TC0IE (Bit0) in the INTE0 register to 1, and execute the EI instruction;

5. ACC, STATUS and RSR data will be saved automatically when the system executes the interrupt service program. After executing the RETI instruction, the data will be restored automatically.

3.7.1.2 TC0 timing calculation instructions

The TC0 timing function assigns the initial value to the timer by writing a value to the TC0C register, and the timer starts to accumulate from the initial value position until the timer overflows and interrupts.

TC0 timing time calculation formula (select internal system clock) :

$$\text{TC0 timing time} = (1/\text{Fosc}) \times (\text{TC0 fractional frequency}) \times (256 - \text{TC0 initial value})$$

Example:

Fosc=8 MHz, TC0 divider selection =8 divider, TC0 initial value =156;

$$\text{TC0 timing time} = (1/8) \times (8) \times (256 - 156) = 100\ \text{us}$$

TC0 timing time calculation formula (select external input clock) :

$$\text{TC0 timing time} = (1/\text{UEXTCLK}) \times (\text{TC0 fractional frequency}) \times (256 - \text{TC0 initial value})$$

Example:

External input clock =1 MHz, TC0 divider selection =4 divider, TC0 initial value =156;

$$\text{TC0 timing time} = (1/1) \times (4) \times (256 - 156) = 400\ \text{us}$$

3.7.1.3 TC0 idle mode wake-up instructions

In the idle mode, the system instruction stops executing, the module with the wake-up function and the system clock work normally, and other functions are forbidden.

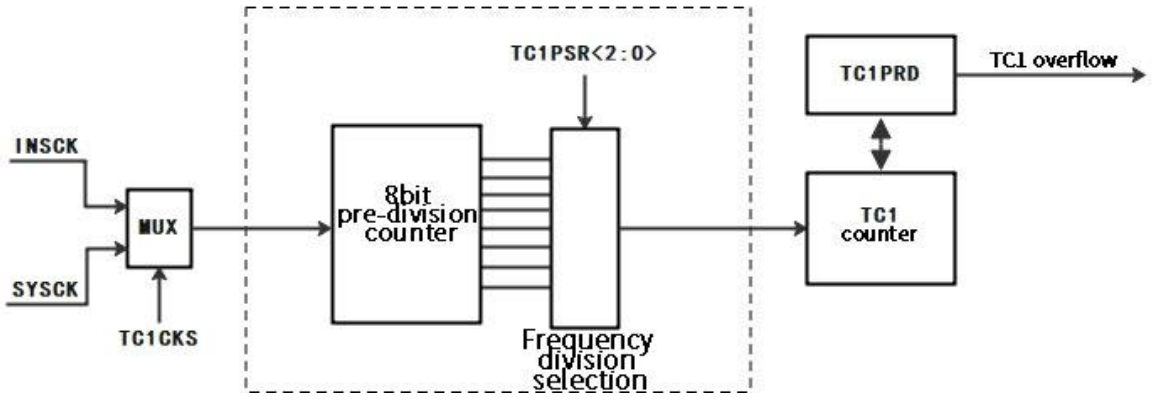
TC0 can wake up the IDLE mode, set R188/CPUCON register Bit4 TC0WE to 1, IDLE = 1 plus SLEEP instruction system into idle mode, TC0 timer normal work (select system clock). When the TC0 timer overflows, the system is woked up. If TC0IE and EI are enabled, an interrupt will be entered after waking up; if DI is executed, the next instruction will be executed after waking up.

3.7.2 TC1 timing counter

The TC1 timing counter provides an 8-bit predivider, and the TC1PSR<2:0> three bits of the TC1CON register determine the predivider ratio. Each time TC1EN is enabled in TC1 mode, the pre-division register is reset.

TC1 is a 10Bit uplink counter. TC1 timers need to be TC1EN enabled to work. The clock source is the internal instruction clock/internal system clock. The counter is incremented by 1 for each clock cycle. Overflow occurs when the TC1 count value is consistent with the TC1PRD set value. If TC1IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service program.

In IDLE mode, TC1 interrupt can wake up the circuit (clock select system clock), after waking up, you can choose to enter the interrupt or continue to execute the original program, the method refers to the port input change to wake up.



TC1 structure block diagram

3.7.2.1 TC1 10Bit timing setup instructions

1, TC1PRDL, TC1PRDTH register assignment, set the count value;

2. Set the pre-frequency ratio of TC1CON register;

3, enable R1D7/INTE1 register TC1IE open interrupt enable, and execute EI instruction;

4, can make TC1EN and PWM1E/PWM3E IPWM1E/IPWM3E (any one), began to TC1 timer count;

5. The system will automatically save ACC, STATUS and RSR data when executing the interrupt service program, and the data will be automatically restored after executing the RETI instruction. The TC1 interrupt flag should be cleared before exiting the interrupt;

3.7.2.2 Description of 20Bit timing setting for TC1 and TC2 cascade

1, enable PWMCON register bit7 bit PWMCAS;

2, TC1PRDL, TC1PRDTH, TC2PRDL, TC2PRDTH register assignment, set count value;

3. Set the pre-frequency ratio of TC1CON register;

4, enable R1D7/INTE1 register TC1IE open interrupt enable, and execute EI instruction;

5, can make TC1EN and PWM1E/PWM3E IPWM1E/IPWM3E (any one), began to TC1 timer count;

6. The system will automatically save ACC, STATUS and RSR data when executing the interrupt service program, and the data will be automatically restored after executing the RETI instruction. The TC1 interrupt flag should be cleared before exiting the interrupt;

3.7.2.3 TC1 timing calculation instructions

The TC1 timing function writes values to TC1PRDL and TC1PRDTH registers, and the timer accumulates from the initial value 0x01 until the timer count matches the value of TC1PRD<9:0>, then the interrupt service program is overflowing.

TC1 timing time calculation formula (select 10Bit counter mode) :

$$\text{TC1 Timing time} = (1/\text{Fosc}) \times (\text{TC1 fractional frequency}) \times (\text{TC1PRD} - 1)$$

Example:

Fosc=8 MHz, TC1 frequency selection =8, TC1PRD value =512;

$$\text{TC1 Timing time} = (1/8) \times (8) \times （512 - 1） = 511\text{us}$$

TC1 timing time calculation formula (select 20Bit counter mode) :

$$\text{TC1 Timing time} = (1/\text{Fosc}) \times (\text{TC1 fractional frequency}) \times (\text{TC1PRD, TC2PRD} - 1)$$

Example:

Fosc=1 MHz, TC1 divider selection =4 divider, TC1PRD, TC2PRD value =0X15A0=5536;

$$\text{TC1 Timing time} = (1/1) \times (4) \times (5536 - 1) = 22140\text{us}$$

3.7.2.4 TC1 idle mode wakeup instructions

TC1 can wake up the idle mode, enable the R188/CPUCON register Bit4 TC1TC2WE, select the TC1 clock source as the system clock. IDLE = 1 plus SLEEP command the system enters idle mode and the TC1 timer works normally. After the TC1 timer overflows, the system is woken up.

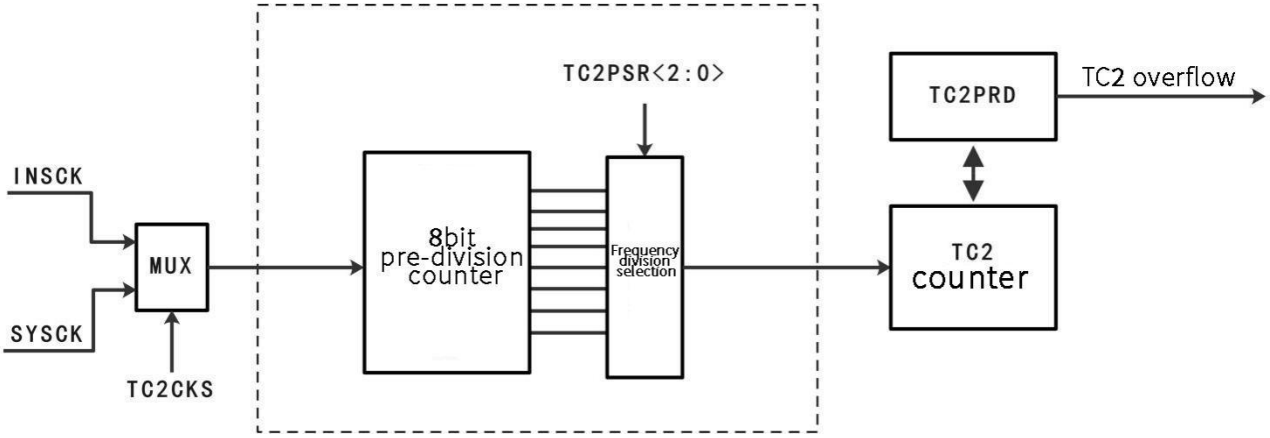
If TC1IE and EI are enabled, the system will wake up and enter the interrupt. If DI is executed, the system will wake up and execute the next instruction.

3.7.3 TC2 timing counter

The TC2 timing counter provides an 8-bit predivider, and the TC2PSR<2:0> three bits of the TC2CON register determine the predivision ratio. Each time TC2EN is enabled in TC2 mode, the pre-division register is reset.

TC2 is a 10Bit uplink counter. TC2 timers need to be TC2EN enabled to work. The clock source is the internal instruction clock/internal system clock. The counter is incremented by 1 for each clock cycle. Overflow occurs when the TC2 count value is consistent with the TC2PRD set value. If TC2IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service program.

In IDLE mode, TC2 interrupt can wake up the circuit (clock select system clock), after waking up, you can choose to enter the interrupt or continue to execute the original program, the method refers to the port input change to wake up.



TC2 structure block diagram

3.7.3.1 TC2 10Bit timing setup instructions

1, TC2PRDL, TC2PRDTH register assignment, set the count value;

2. Set the pre-frequency ratio of TC2CON register;

3, enable R1D7/INTE1 register TC2IE open interrupt enable, and execute EI instruction;

4, can make TC2EN and PWM2E/PWM4E IPWM2E/IPWM4E (any one), began to TC2 timer count;

5. The system will automatically save ACC, STATUS and RSR data when executing the interrupt service program, and the data will be automatically restored after executing the RETI instruction. The TC2 interrupt flag should be cleared before exiting the interrupt;

3.7.3.2 Description of 20Bit timing setting for TC2 and TC1 cascade

Refer to 3.7.2.2 TC1, TC2 cascaded 20Bit timing setting instructions;

3.7.3.3 TC2 timing calculation instructions

The TC2 timing function writes values to TC2PRDL and TC2PRDTH registers, and the timer accumulates from the initial value 0x01 until the timer count matches the value of TC2PRD<9:0>, then the interrupt service program is overflows.

TC2 timing time calculation formula (select 10Bit counter mode) :

$$\text{TC2 Timing time} = (1/\text{Fosc}) \times (\text{TC2 fractional frequency}) \times (\text{TC2PRD} - 1)$$

Example:

Fosc=8 MHz, TC2 divider selection =8 divider, TC2PRD value =512;

$$\text{TC2 Timing time} = (1/8) \times (8) \times （512 - 1） = 511\text{us}$$

3.7.3.4 TC2 idle mode wakeup instructions

TC2 can wake up the idle mode to enable the R188/CPUCON register Bit4 TC1TC2WE and select the TC2 clock source as the system clock. IDLE = 1 plus SLEEP command the system enters idle mode and the TC2 timer works normally. After the TC2 timer overflows, the system is woken up. If TC2IE and EI are enabled, an interrupt will be entered after the wake-up, and if DI is executed, the next instruction will be executed after the wake-up.

3.8 PWM pulse width modulation

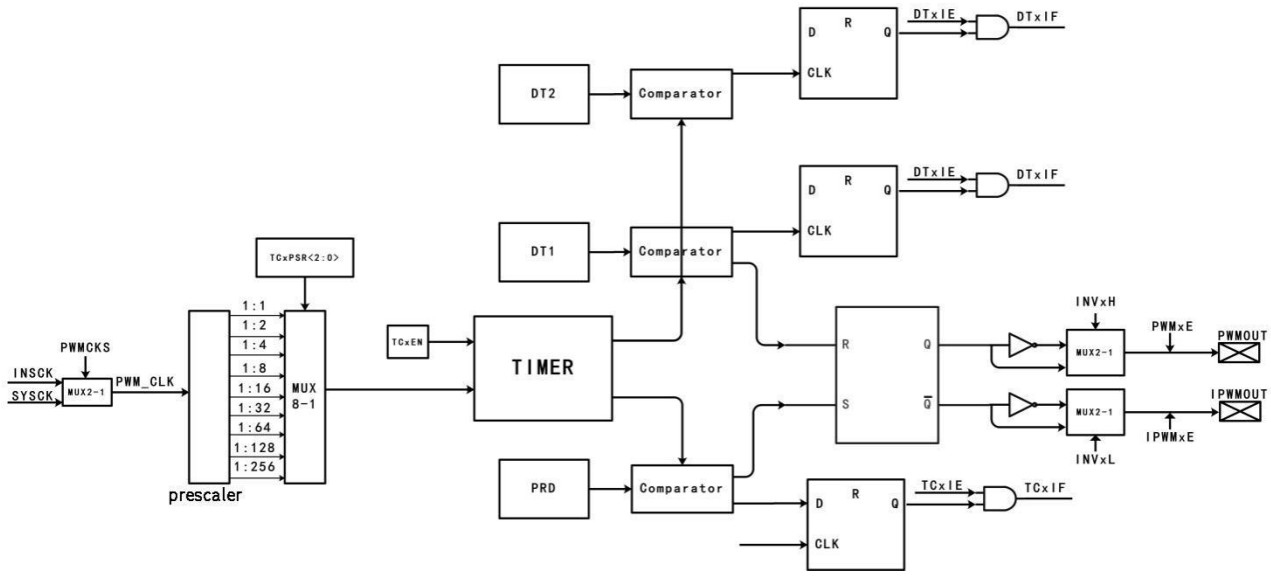
JZ8P2615 built-in 4 10Bit PWM(PWM1/PWM3 common cycle, PWM2/PWM4 common cycle), can be mapped to select the output port, can set the dead-time complementary, can be cascaded into a 20BitPWM. PWM module built-in 2 8Bit frequency divider, can choose frequency division ratio through TC1CON/TC2CON register, PWM1/PWM3 share a set of counter (TC1) and pre-divider, PWM2/PWM4 share another set of counter (TC2) and pre-divider, PWM2/PWM4 share another set of counter (TC2) and pre-divider. The PWM clock source can be configured as internal instruction clock and internal system clock.

The PWM has a cycle overflow interrupt and a duty cycle matching interrupt, which can jump to the interrupt service routine when enabled.

In IDLE mode, the clock source selects the internal system clock and enables either TC1TC2WE + TC1IE or TC1TC2WE + TC2IE to wake up the system.

3.8.1 Internal structure and timing of PWM

The following internal structure diagram is for reference only and does not represent the actual circuit.



PWM working structure circuit

3.8.2 PWM cycle and duty cycle

The PWM1/PWM3 and PWM2/PWM4 provide a 10bit clock counter with 8bit programmable predivision as the baud rate clock generator of the PWM module. The TCxEN in the register can be enabled by enabling the PWM control to enable the counter function. Through the TCxPSR<2:0> control bit, the counter can be pre-divided. INVxH and INVxL control the output to invert, PWMxE and IPWMxE enable PWM function and PWM complementary function, respectively.

The PWM cycle writes values to the TCxPRDL (low eight bits) and TCxPRDTH (high two bits) cycle registers. When the value of the counter is equal to the PRD value, the following events occur in the next increment cycle:

- The counter clears;
- Corresponding PWM output pin high level (IPWM pin low level);
- Generate PWM cycle overflow interrupt (if enabled);
- The PWM duty cycle is latched from PWMxDTL/TCxPRDTH register to DT/TIMER compare register;

PWM cycle calculation formula:

$$\text{PWM cycle} = (\text{PRD}) \times (\text{PWM_CK}) \times (\text{PWM Timing time})$$

Examples:

PWMxRD=100, Fosc=8MHz, PWMCKS=1, PWM divider selection =2 dividers;

$$\text{PWM cycle} = (100) \times (1/8) \times (2) = 25\ \text{us}$$

PWM duty cycle by writing the value to the PWM duty cycle register, when the value of the counter overflow clear, the value of the PWMxDT is latched to the DT/TIMER comparison register. When the value of the DT/TIMER comparison register is equal to the value of the TIMER counter, the PWM output pin is set to low. The value of PWMxDT can be written at any time, but the value of the DT/TIMER comparison register is only written when the cycle overflows:

PWM duty cycle calculation formula:

$$\text{PWM dutyratio} = (\text{DT}) \times (\text{PWM_CK}) \times (\text{PWM Timing time})$$

Example:

PWMxDT=50, Fosc=8MHz, PWMCKS=1, PWM divider selection =2 dividers;

$$\text{PWM dutyratio} = (50) \times (1/8) \times (2) = 12.5\ \text{us}$$

3.8.3 20-Bits PWM cascade mode

The PWM cascade mode enables two 10Bit PWM functions to be combined into one 20Bit PWM. Enabled by the PWMCAS bit of the R1C8 PWM control register, enabled by cascading TC1 and TC2 combined to form a 20Bit PWM. In this mode, the necessary parameters are redefined as shown in the table below:

20Bit PWM	DT(duty cycle)	PRD (cycle)	TIME (timer)
10 Bit high	PWM2DT	TC2PRD	TC2
10 Bit lower	PWM1DT	TC1PRD	TC1

The predivider in 20Bit PWM mode uses the predivider of TC1, the interrupt function multiplexes TC1IE and DT1IE, and the waveform output pin multiplexes PWM1 and IPWM1 ports.

3.8.4 PWM dead-time control Instructions

JZ8P2615 PWM module with dead-time control, complementary output function.

PWM1/PWM3 share a set of dead-time control counters, PWM2/PWM4 share a set of dead-time control counters, by configuring R1C7/DEADCON(dead-time control register) bit<7:6> to enable the dead-time function, configuring bit<5:4> to allocate the dead-time counter, Configure bit<3:0> to select the frequency division of the dead-time clock. The bit<3:0> of R1C8/PWMCON(PWM control register) INVxH is the reverse option of PWMx output, and INVxL is the reverse option of IPWMx output (PWM1/PWM3 and PWM2/PWM4 are shared respectively, and are selected according to DEAD2_SEL and DEAD1_SEL); R1C9/DEADT0 and R1CA/DEADT1 are dead-time control registers, which are assigned values. When the dead-time counter counts to the given value, the PWM high and low conversion operation is performed, which is the actual dead-time.

3.8.5 PWM idle mode wakeup instructions

In the idle mode, the CPU instruction stops executing, the module with the wake-up function and the system clock work normally, and other functions are forbidden.

PWM can wake up the idle mode, set the TC1TC2WE wake-up enable, select the clock source as the system clock (SYSCK). Set the corresponding cycle or duty cycle interrupt enable, IDLE = 1+ SLEEP command system into idle mode, PWM timer normal work.

When the corresponding interrupt condition is met, the system is woken up. If EI is enabled, the system will enter the interrupt after waking up, and if DI is enabled, the next instruction will be executed after waking up.

3.8.6 PWM pulse width modulation setting instructions

1. Set R1C8/PWMCON register as needed: PWM clock source, PWM cascade and whether the corresponding port is reversed;

2, according to the need to set R1B0/TC1CON or R1B6/TC2CON register: select the pre-frequency ratio, enable PWM/IPWM output;

3, according to the need to set R1C6/PWMIS register: select output port;

4. Set R1C7/DEADCON, R1C9/DEADT0, R1CA/DEADT1 registers as needed;

5, write PWM cycle register value;

6, write PWM duty cycle register value;

7, according to the need to set interrupt enable bit, wake up bit, clear flag bit;

Enable the corresponding PWM counter (TCxEN);

9. After triggering the interrupt, if the enable "EI", the chip jumps to the interrupt vector address, if the enable "DI" instruction will execute the next instruction;

3.9 ADC analog-to-digital conversion

The JZ8P2615 ADC module provides a 12-bit precision SAR AD converter containing 15 analog channels.

The ADC converter uses successive approximation analog-to-digital conversion, and the results are stored in R1A3/ADATH(ADC conversion result high 8-bit register), R1A4/ADATL(ADC conversion result low 8-bit register), R1A5/ADIS(AD sampling port enabled and AD high 4-bit register) result registers. The channel selection, zero correction, internal and external reference voltage sources, sampling clock, ADC startup and ADC power consumption are set through ADCON0 and ADCON1 control registers.

The completion of AD conversion can enter the interrupt, or can be judged by querying the ADRUN bit of R1A7/ADCON1.

If the AD wakeup function is enabled, the completion of AD conversion can be woken from sleep mode or idle mode.

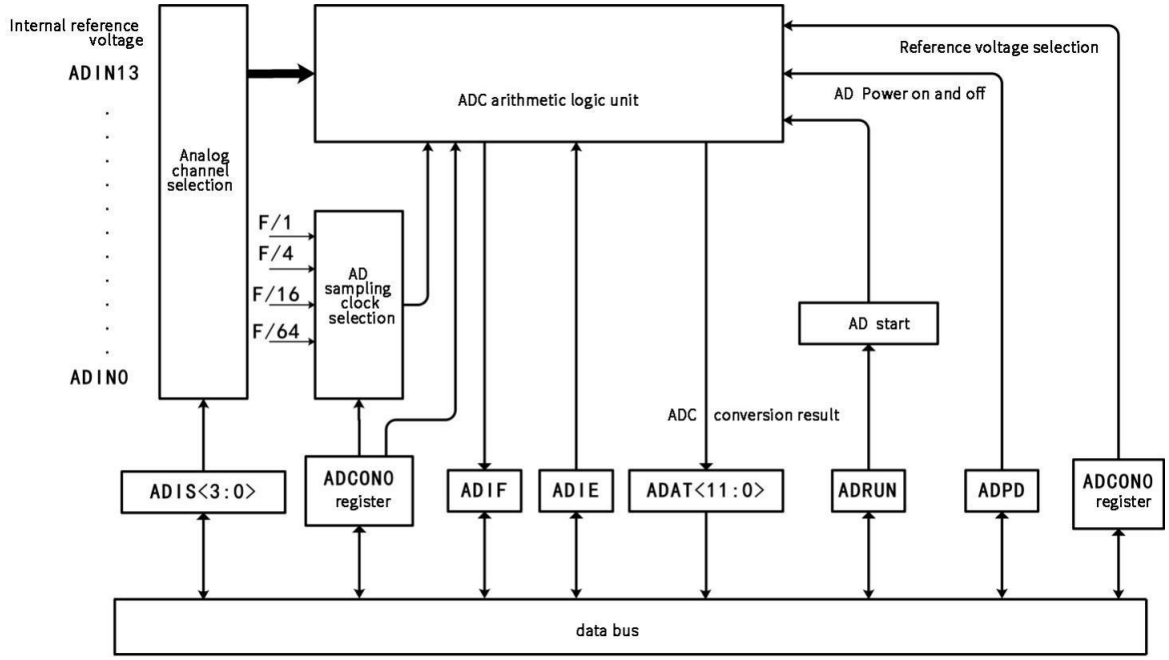


Illustration of the AD conversion function

AD sampling time calculation method:

Starting from ADRUN=1, the time to complete one AD sampling =**ADC sampling-hold period +AD conversion time**

AD conversion time:

It takes one TAD time for AD to convert 1 bit, and 12 TAD time for chip built-in 12bit AD.

AD sampling voltage value calculation:

$$\text{ADC Sampling voltage} = \frac{\text{sampling value}}{4096} * \text{Voltage reference}$$

Example: the reference voltage is the internal reference 3V, and the sampling value is 0x800=2048

$$\text{ADC Sampling voltage} = \frac{2048}{4096} * 3 = 1.5\text{V}$$

3.9.1 ADC detection power supply voltage description

By configiting the ADIS register, the channel selection bit ADIS<3:0>=1110 selects AD14 (built-in reference voltage), at which time the ADC reference voltage is automatically set to the internal VDD voltage. The selected built-in reference voltage is used as the sampling voltage of the ADC, for example, VREF<2:0>=100 selects 1.5V as the sampling channel AD14 voltage input to the ADC.

Taking 1.5V as the sampling value and VDD as the reference voltage, the conversion result is obtained by ADC conversion. The voltage value of VDD can be deduced reversely:

$$\text{Conversion result} = (1.5/\text{VDD}) \times 4096$$

the

$$\text{VDD} = (1.5 \times 4096) / \text{Conversion result}$$

3.9.2 ADC analog to digital conversion Settings

1. Enable ADC input port and select analog channel, set R1A0/P5ADE, R1A1/P6ADE, R1A5/ADIS registers;

2. ADC reference voltage source, clock pre-frequency and reference voltage selection, set R1A6/ADCON0, R1A7/ADCON1 registers;

3. If the interrupt function is needed, set ADIE=1 and execute the "EI" instruction;

4. Set "ADPD=1" to start AD supply voltage;

5, call AD precision correction subroutine;

6, according to the need to select the IDLE/SLEEP mode, set the AD wake-up function, ADCWE=1;

7, set "ADRUN=1" to start AD conversion;

8, wait for the interrupt or ADRUN is clear 0, if the AD interrupt occurs, the ADIF should be clear 0 when leaving the interrupt program;

9, save the result of conversion. If you need to do multiple AD conversions, skip to step 7;

3.9.3 Description of ADC analog to digital conversion accuracy correction

1. Enable ADC to compensate and calibrate CALI on the basis of completing steps 1 to 4 of 3.9.2 ADC analog-to-digital conversion setup instructions;

2. Set the ADC compensation voltage polarity SIGN, and calibrate the positive voltage of the ADC first, and then the negative voltage of the ADC, each time

2LSB compensation amplitude;

Cyclic detection of AD value, the result is "0" to end the AD accuracy correction, the "CALI" position of ADC is 0;

4.OPTION configuration table

CODE OPTION	Options	Feature Description
Watchdog	Enable	Watchdog WDT enables
	Forbidden	Watchdog WDT prohibited
Clocks split frequency	2 Clocks	2 Clocks are selected for instruction clock division
	4 Clocks	Select 4 Clocks for instruction clock division
	8 Clocks	8 Clocks are selected for instruction clock division
	16 Clocks	16 Clocks are selected for instruction clock division
	32 Clocks	32 Clocks are selected for instruction clock division
IRC frequency	910KHz	Choose 910KHz for IRC frequency
	1M	Choose 1M for IRC frequency
	3.4 M	IRC frequency choose 3.4M
	4.8 M	IRC frequency choose 4.8M
	5.4 M	IRC frequency choose 5.4M
	6M	Choose 6M for IRC frequency
	8M	Choose 8M for IRC frequency
Oscillator octave option	Enable	Oscillator doubling function enabled
	Forbidden	Oscillator doubling function prohibited
Low voltage reset	As = 1.2 V	Choose 1.2V for the low voltage reset point
	As = 1.6 V	Choose 1.6V as the low voltage reset point
	As = 1.8 V	Choose 1.8V as the low voltage reset point
	As = 2.4 V	Choose 2.4V as the low voltage reset point
	As = 2.7 V	Choose 2.7V as the low voltage reset point
	As = 3.3 V	Choose 3.3V as the low voltage reset point
	As = 3.6 V	Choose 3.6V for the low voltage reset point
	As = 3.9 V	Choose 3.9V as the low pressure reset point
	Forbidden	LVR feature forbidden, testing only, not for mass production
OTP paging selection	Use 2K	Choose 2K storage for the OTP ROM
	Use the first 1K	Select the first 1K of storage for OTP ROM
	Use the last 1K	OTP ROM selection after 1K storage space
Code encryption	No encryption	ROM area data is not encrypted
	Encryption	ROM area data encryption
Reset port pull up	Enable	Reset port pull-up feature enabled
	Forbidden	Reset port pull-up is disabled
P63 port	RST	P63 port for external reset port
	GPI	P63 port serves as a universal input port
	GPIO	The P63 port serves as a general-purpose input/output port
Drive enhancement	Enable	Port driver enhancements enable
	Forbidden	Port drive enhancements forbidden
Reset time	PWRT = WDT = 4.5 ms	Reset setup time =WDT overflow time (regardless of frequency) = 4.5ms

	PWRT=WDT=18ms	Reset setup time =WDT overflow time (regardless of frequency) = 18ms
	PWRT=WDT=72ms	Reset setup time =WDT overflow time (regardless of frequency) = 72ms
	PWRT=WDT=288ms	Reset setup time =WDT overflow time (regardless of frequency) = 288ms
	PWRT = 140 us, WDT = 4.5 ms	Reset setup time =140us,WDT overflow time (regardless of frequency) =4.5ms
	PWRT=140us,WDT=18ms	Reset setup time =140us,WDT overflow time (regardless of frequency) =18ms
	PWRT=140us,WDT=72ms	Reset setup time =140us,WDT overflow time (regardless of frequency) =72ms
	PWRT=140us,WDT=288ms	Reset setup time =140us,WDT overflow time (regardless of frequency) =288ms
ADC sample hold time	12TAD	Choose 12TAD for the ADC sample hold time
	8TAD	Choose 8TAD for the ADC sample hold time
	4TAD	Choose 4TAD for the ADC sample hold time
	2TAD	Choose 2TAD for ADC sample hold time
The ADC sample value is forced to raise 14 least significant bits	Forbidden	Disallow the ADC sample value to force up 14 least significant bits
	Enable	Enable ADC sample values to force up 14 least significant bits
IRC oscillator voltage source selection	Choose LDO voltage for IRC	IRC oscillator voltage source Select LDO voltage
	Choose VDD voltage for IRC	Choose VDD voltage for IRC oscillator voltage source
Encapsulate pin	16pin	16 pins are selected for chip packaging
	14pin	Choose 14 pin for chip package foot position

5. Instruction set

Instructions	Command action	Flag impact
ADD A,R	A+R→A	Z,C,DC
ADD R,A	A+R→R	Z,C,DC
AND A,R	A&R→A	Z
AND R,A	A&R→R	Z
CLRA	0→A	Z
CLR R	0→R	Z
INVA R	/R→A	Z
INV R	/R→R	Z
DA	The A register is adjusted to the BCD value	C
DECA R	R-1→A	Z
DEC R	R-1→R	Z
DJA R	R-1→A, skip if zero	-
DJ R	R-1→R, skip if zero	-
INCA R	R+1→A	Z
INC R	R+1→R	Z
IJA R	R+1→A, skip if zero	-
IJ R	R+1→R, skip if zero	-
MOV R,A	A→R	-
MOV A,R	R→A	Z
MOV R,R	R→R	Z
OR A,R	A∨VR→A	Z
OR R,A	A∨VR→R	Z
SUB A,R	R-A→A	Z,C,DC
SUB R,A	R-A→R	Z,C,DC
XOR A,R	A⊕R→A	Z
XOR R,A	A⊕R→R	Z
BTC R,b	0→R(b)	-
BTS R,b	1→R(b)	-
JBTC R,b	if R(b)=0, skip	-
JBTS R,b	if R(b)=1, skip	-
LCR R	R(n)→R(n+1),R(7)→C, C→R(0)	C
LCA R	R(n)→A(n+1),R(7)→C, C→A(0)	C

RCR R	R(n)→R(n-1),R(0)→C, C→R(7)	C
RCA R	R(n)→A(n-1),R(0)→C, C→A(7)	C
SWAP R	R(0-3) ↔ R(4-7)	-
SWAPA R	R(0-3)→A(4-7),R(4-7)→A(0-3)	-
ADD A,k	A+k→A	Z,C,DC
AND A,k	A&k→A	Z
MOV A,k	k→A	-
OR A,k	A∨k→A	Z
SUB A,k	k-A→A	Z,C,DC
XOR A,k	A⊕k→A	Z
CALL k	PC+1→[SP], (Page,k)→PC	-
DI	Disallow interruption	-
EI	Enable Interrupt	-
JMP k	K (Page,k)→PC	-
NOP	Empty instruction	-
RET	[top of stack]→PC	-
RETI	[top of stack]→PC, enable interrupt	-
RETL k	k→A,[top of stack]→PC	-
SLEEP	0→WDT, the oscillator stops oscillating (sleep mode)	T,P
CWDT	0→WDT	T,P
TBRD R	Machine code bit7 ~ 0 to ACC Machine code bit15 to 8 to R (general purpose register)	-

6. Electrical characteristics

6.1 Limit parameters

Working temperature... -40℃ ~ 85℃
Storage temperature... -65 C to 150 C
The input voltage... Vss-0.3V ~ Vdd+0.5V
The output voltage... Vss-0.3V ~ Vdd+0.5V
Working voltage... 1.8 V to 5.5 V

6.2 DC electrical characteristics

(V_{DD} =5V, operating temperature =25 ° C, unless otherwise stated)

Symbol	Parameter description	Conditions	Minimum	Typical	Largest	Units
IRC1	IRC1 (after correction)	OPTION select 8MHz	-	8	-	MHz
IRC2	IRC2 (after correction)	The OPTION is 6MHz	-	6	-	MHz
IRC3	IRC3 (after correction)	OPTION select 5.4MHz	-	5.4	-	MHz
IRC4	IRC4 (after correction)	OPTION to choose 4.8MHz	-	4.8	-	MHz
IRC5	IRC5 (after correction)	OPTION select 3.4MHz	-	3.4	-	MHz
IRC6	IRC6 (after correction)	OPTION select 1MHz	-	1	-	MHz
IRC7	IRC7 (after correction)	OPTION select 910KHz	-	910	-	KHz
IOH1	Output high level driver (except P63)	Ioh = 4.4 V	6	7	8	mA
IOH2	Output High level driver (P63)	Ioh = 4.4 V	11	13	15	mA
IOH3	Output high level drive enhancement	Ioh = 4.4 V	16	18	20	mA
IOH4	Output high level weak drive (except	Ioh = 4.4 V	3.3	3.8	4.3	mA
IOH5	Output High Level Weak Drive (P63)	Ioh = 4.4 V	6	7	8	mA
IOL1	Output low level driver (except P63)	Iol = 0.6 V	11	13	15	mA
IOL2	Output Low Level driver (P63)	Iol = 0.6 V	6	8	10	mA
IOL3	Output low level drive enhancement	Iol = 0.6 V	24	26	28	mA
IOL4	Output Low Level Drive	Iol = 0.6 V	15	17	19	mA
IOL5	Output low level weak drive (except	Iol = 0.6 V	4	4.5	5	mA
IOL6	Output Low Level Weak Drive (P63)	Iol = 0.6 V	1	2	3	mA
IPH	Pull-up current	Pull up enable, input ground	80	90	100	μA
IPD	Pull-down current	Pull down enable, input to	80	90	100	μA
Isb1	Power off current 1	The input is connected to VDD, and the output is	-	-	1	μA
Isb2	Power off current 2	The input is connected to VDD, the output is	-	-	10	μA
Isb3	Power off current 3	Input to VDD, output dangling, ADC enabled	-	430	-	μA
Iop1	Operating current 1 (VDD=5V)	IRC=8MHz 2clock	-	-	2	mA
Iop2	Working current 2 (VDD=5V)	IRC=1MHz 2clock	-	0.2	-	mA
LVR	Low voltage reset (1M 16CLOCK)	Select the LVR reset point	Vlvr - 0.2 -	Vlvr	Vlvr + 0.2	V

6.3 AD conversion feature

(V_{DD} =5V, V_{SS}=0V, operating temperature =25℃)

Symbols		Parameter Description	Conditions	Minimum	Typical	Largest	Units
V_{AREF}		Analog reference voltage	$V_{AREF} - V_{ASS} \geq 2V$	2	-	V_{DD}	V
V_{ASS}				V_{SS}	-	V_{SS}	V
VAI		Analog input voltage	-	V_{ASS}	-	V_{AREF}	V
IAI1	I_{VDD}	Analog supply current	V_{AREF}=VDD=5V V_{ASS}=0V FS[*1]=100KHz FIN[*1]=1KHz (VREF from internal Vdd)	-	1000	1400	u A
	I_{VREF}			-	-	10	u A
IAI2	I_{VDD}	Analog supply current	V_{AREF}=VDD=5V V_{ASS}=0V FS[*1]=100KHz FIN[*1]=1KHz (VREF from external VREF pin)	-	-	900	u A
	I_{VREF}			-	-	500	u A
RN		Resolution	-	-	12	-	Bits
TAD		ADC periodic clock	VDD= V_{AREF}= 5V and	1	-	-	u s
T_{SH}		Sample and hold time	VDD=3 to 5.5V V_{ASS}=0V, Ta=25 ° C	4	-	-	u s
			VDD=2.5 ~ 3V V_{ASS}=0V, Ta=25 ° C	16	-	-	u s
TCN		AD conversion time	VDD=2.5 to 5.5V, V_{ASS}=0V	14	-	24	TAD
TADD1		AD "ADRUN" position high starts the delay between the first TAD	VDD=2.5 to 5.5V V_{ASS}=0V	0.5	-	-	TAD
PSRR		Power supply rejection ratio	V_{AREF} = 2.5 V V_{ASS}=0V VIN[*1]=0V ~ 2.5V	-	-	2	LSB

6.4 VREF feature

(V_{DD} =5V, V_{SS}=0V, Ta=-40 ~ 85 ° C)

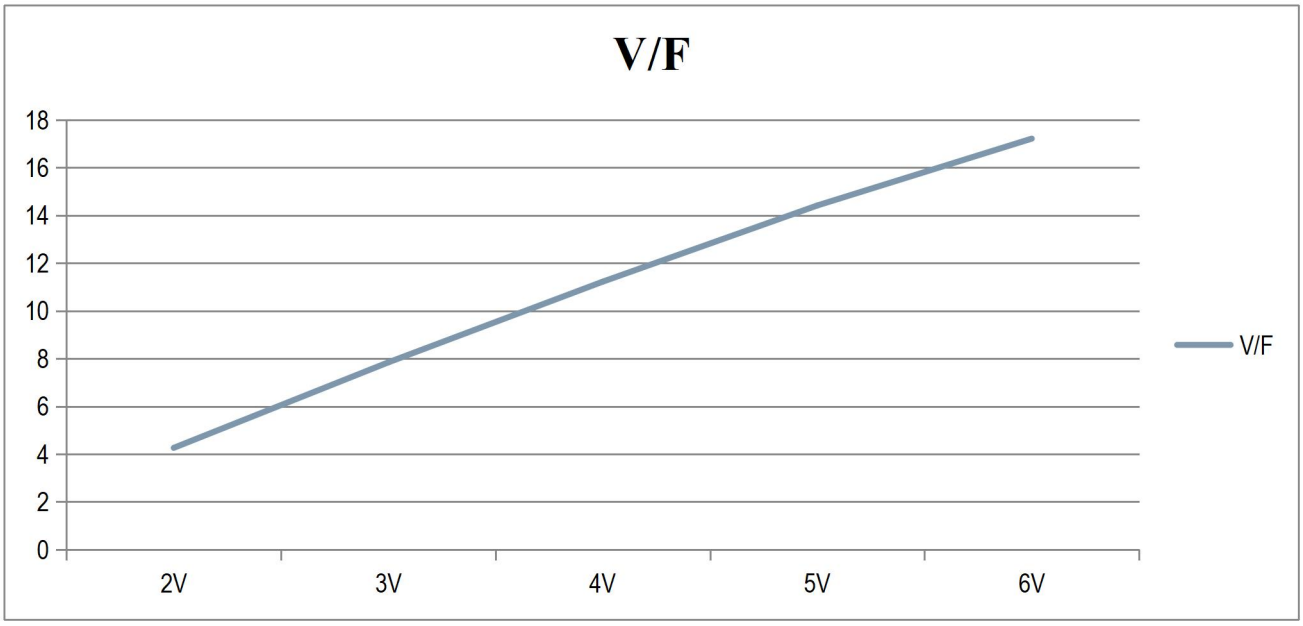
Symbol	Parameter description	Conditions	minimum	Typical	Largest	Units
VDD	Supply voltage	-	2.2	-	5.5	V
I_{VDD}	DC supply current	No load	-	-	250	u A
VREF	Reference voltage output	2 V, 1.5 V, 3 V, 4 V	-	Plus or minus	1.75	%
Warm up Time	Refer to voltage preparation time	VDD = VDDmin - 5.5 V, Cload = 19.2 pf Rload-15.36KΩ	-	38	50	u s
VDDmin	Minimum supply voltage	-	-	VREF + 0.2	-	V

6.5 Characteristic curve plot

The curves listed in this chapter are for design reference only, part of the data given may exceed the specified working range of the chip, in order to ensure the normal operation of the chip, please strictly refer to the electrical characteristics.

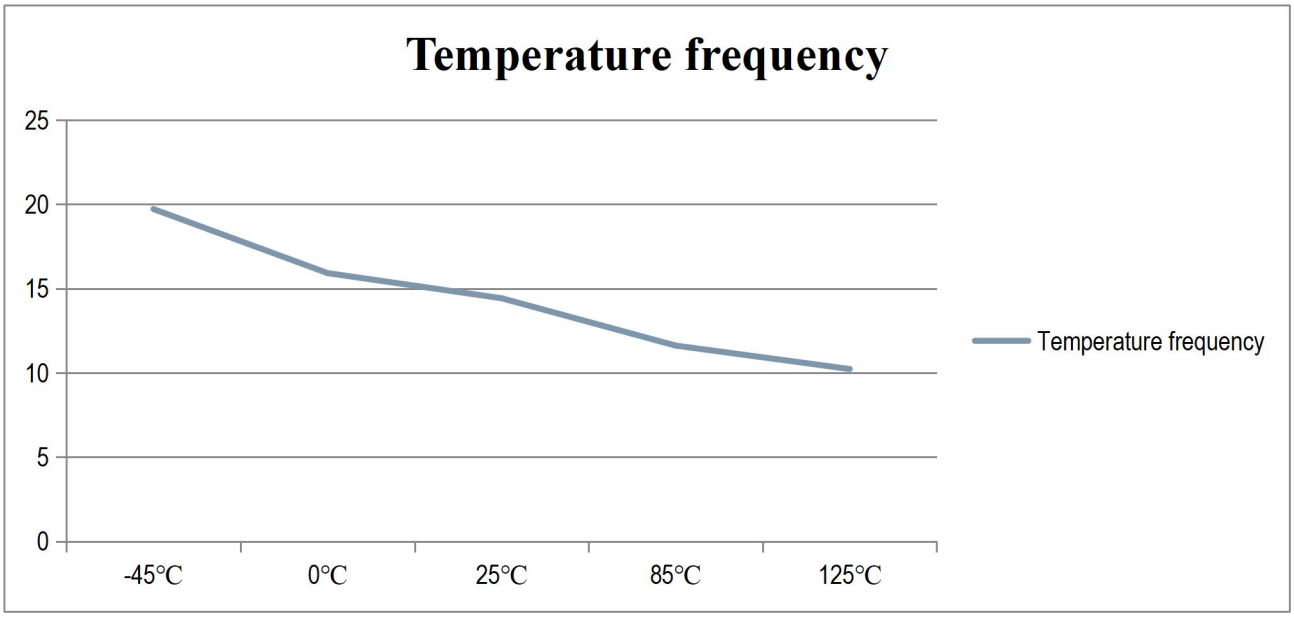
6.5.1 Internal Low speed oscillator - voltage frequency characteristic curve

Operating temperature at 25℃ : (in KHz)



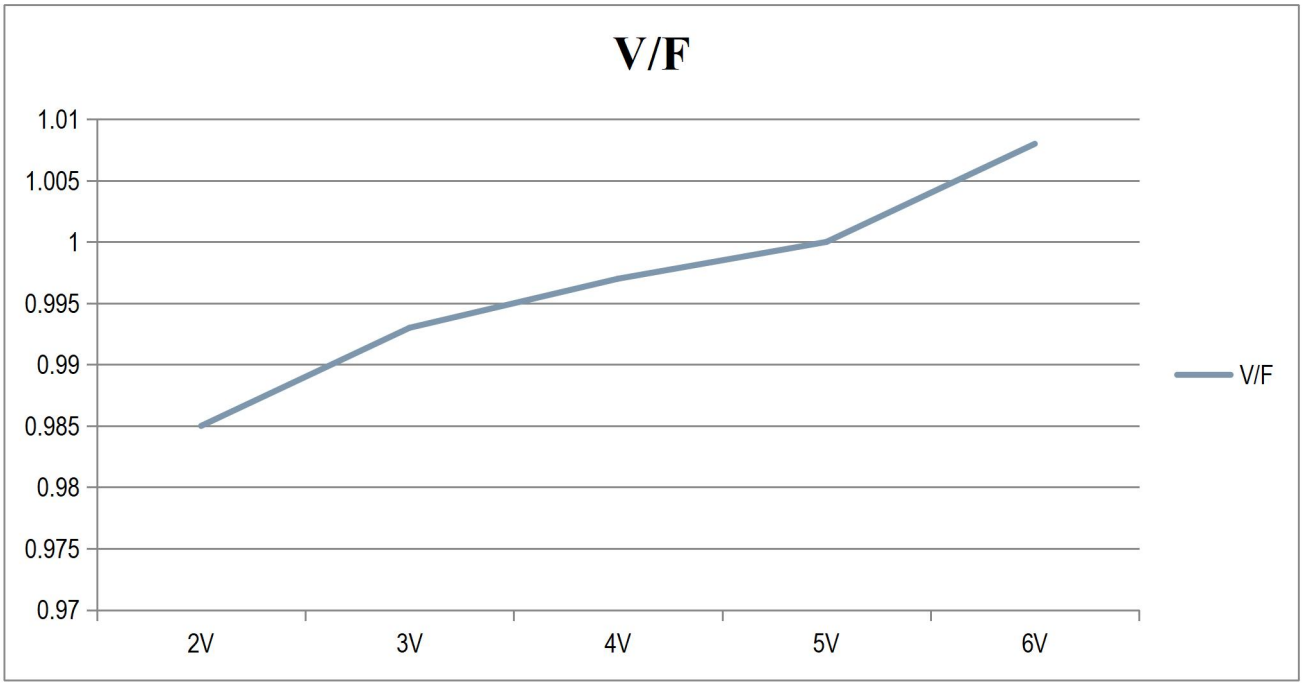
6.5.2 Internal low speed oscillator temperature frequency characteristic curve

Operating voltage at 5V: (in KHz)



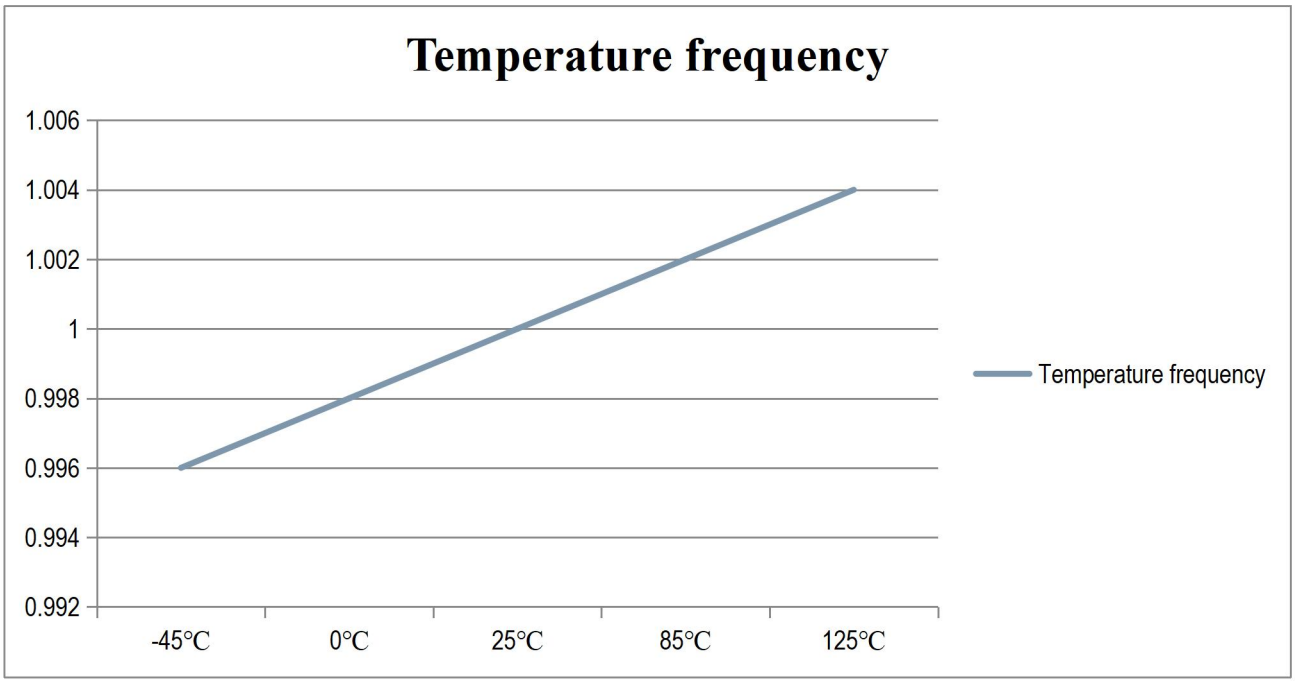
6.5.3 Internal 1Mhz RC oscillator - voltage-frequency characteristic curve

Operating temperature at 25℃ : (in Mhz)



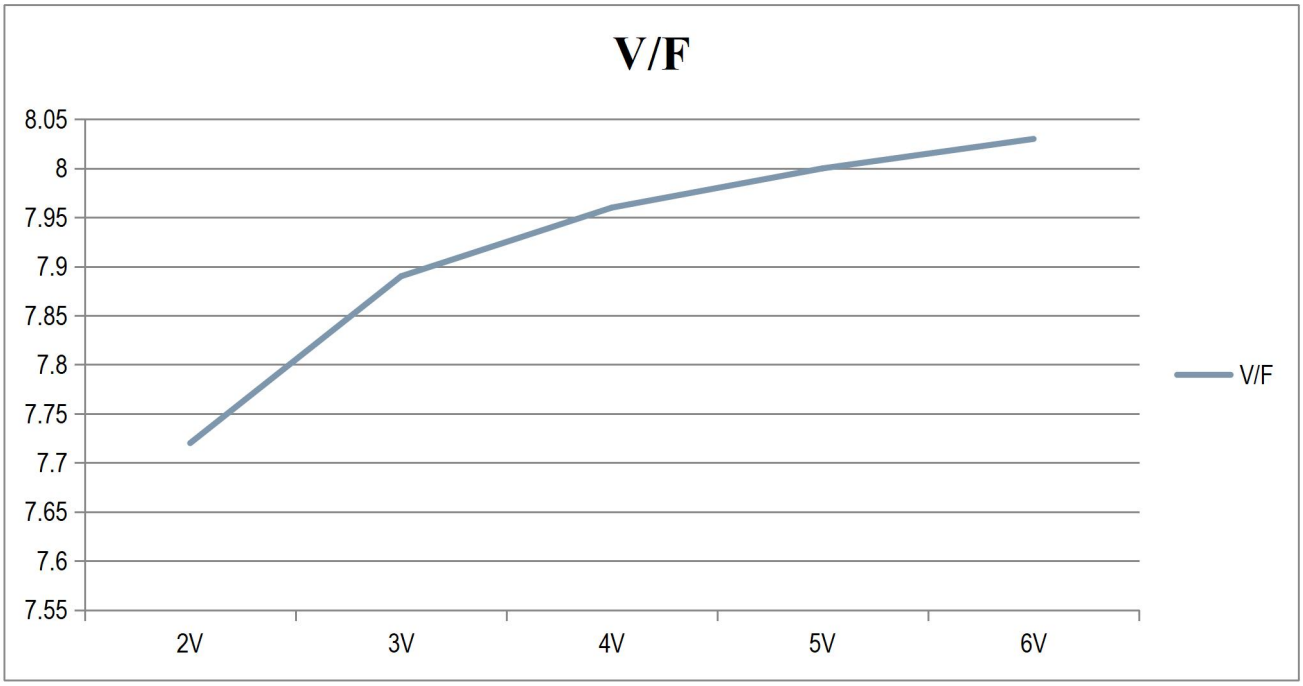
6.5.4 Internal 1Mhz RC oscillator - Temperature-frequency characteristic curve

Operating voltage at 5V: (in Mhz)



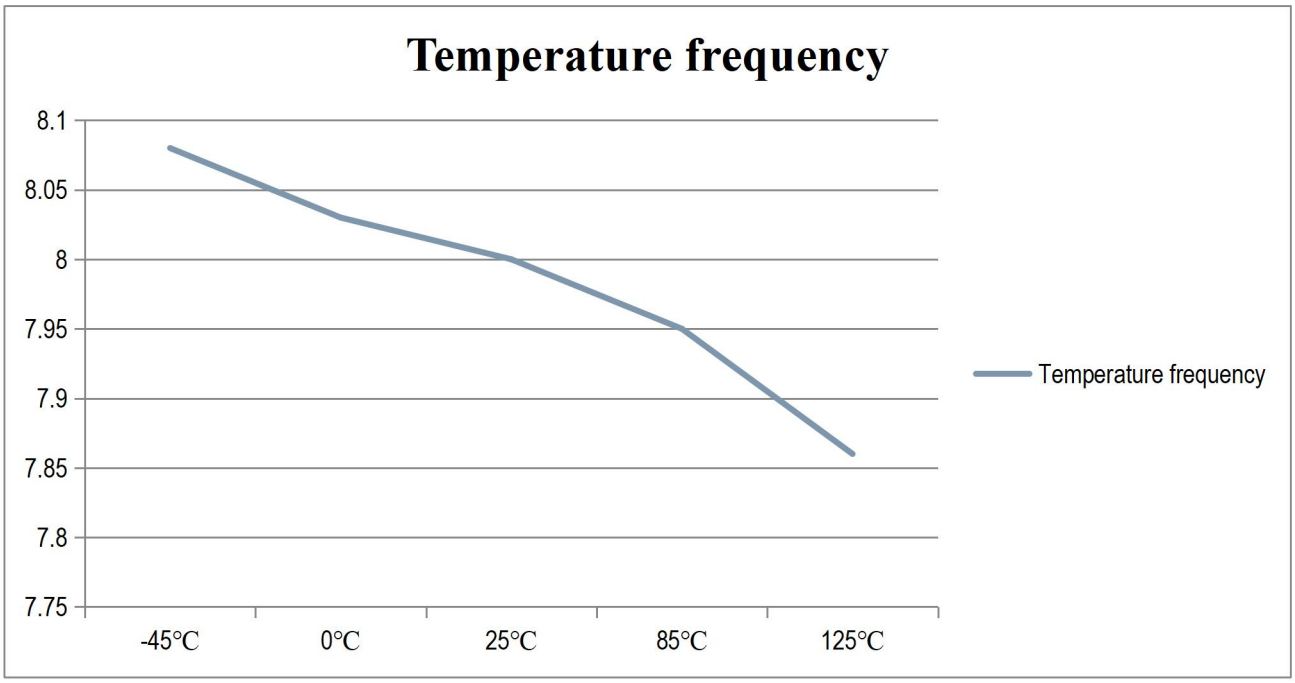
6.5.5 Internal 8Mhz RC oscillator - voltage-frequency characteristic curve

Operating temperature at 25℃ : (in Mhz)



6.5.6 Internal 8Mhz RC oscillator - Temperature-frequency characteristic curve

Operating voltage at 5V: (in Mhz)



6.6 IHRC frequency fine-tuning parameter description

The parameter description is only for reference of change trend, the actual deviation.

IHRCCAL correction value (hexadecimal)	IHRC 8MHz correction ratio (percentage in base 8MHz)
00	- 32.04%
01	- 31.84%
02	- 31.58%
03	- 31.39%
04	- 31.06%
05	- 30.86%
06	- 30.59%
07	- 30.39%
08	- 30.01%
09	- 29.80%
0A	- 29.54%
0B	- 29.33%
0C	- 28.98%
0D	- 28.76%
0E	- 28.48%
0F	- 28.28%
10	- 27.96%
11	- 27.74%
12	- 27.44%
13	- 27.21%
14	- 26.86%
15	- 26.63%
16	- 26.31%
17	- 26.10%
18	- 25.68%
19	- 25.43%
1A	- 25.11%
1B	- 24.88%
1C	- 24.49%
1D	- 24.25%
1E	- 23.93%
1F	- 23.70%
20	- 23.61%
21	- 23.35%
22	- 23.03%
23	- 22.78%
24	- 22.38%
25	- 22.11%
26	- 21.76%
27	- 21.50%
28	- 21.03%

29	- 20.75%
2A	- 20.40%
2B	- 20.13%
2C	- 19.69%
2D	- 19.40%
2E	- 19.03%
2F	- 18.76%
30	- 18.38%
31	- 18.08%
32	- 17.66%
33	- 17.38%
34	- 16.93%
35	- 16.63%
36	- 16.21%
37	- 15.93%
38	- 15.36%
39	- 15.06%
3A	- 14.65%
3B	- 14.34%
3C	- 13.83%
3D	- 13.50%
3E	- 13.46%
3F	- 13.14%
40	- 13.09%
41	- 12.79%
42	- 12.73%
43	- 12.39%
44	- 11.88%
45	- 11.53%
46	- 11.09%
47	- 10.76%
48	- 10.15%
49	- 9.78%
4A	- 9.33%
4B	- 8.98%
4C	- 8.41%
4D	- 8.04%
4E	- 7.55%
4F	- 7.19%
50	- 6.69%
51	- 6.30%
52	- 5.81%
53	- 5.41%
54	- 4.80%
55	- 4.40%

56	- 3.86%
57	- 3.45%
58	- 2.75%
59	- 2.30%
5A	- 1.75%
5B	- 1.31%
5C	- 0.68%
5D	- 0.22%
5E	0.34%
5F	0.76%
60	0.85%
61	1.30%
62	1.89%
63	2.35%
64	3.05%
65	3.54%
66	4.14%
67	4.64%
68	5.45%
69	5.98%
6A	6.61%
6B	7.14%
6C	7.90%
6D	8.44%
6E	9.14%
6F	9.66%
70	10.33%
71	10.91%
72	11.60%
73	12.15%
74	12.98%
75	13.58%
76	14.33%
77	14.90%
78	15.90%
79	16.54%
7A	17.33%
7B	17.96%
7C	18.90%
7D	19.58%
7E	20.39%
7F	21.03%
80	- 1.30%
81	- 1.03%
82	- 0.66%

83	- 0.36%
84	0.09%
85	0.36%
86	0.76%
87	1.04%
88	1.57%
89	1.86%
8A	2.26%
8B	2.60%
8C	3.09%
8D	3.42%
8E	3.81%
8F	4.10%
90	4.53%
91	4.89%
92	5.35%
93	5.70%
94	6.20%
95	6.59%
96	7.01%
97	7.36%
98	7.93%
99	8.31%
9A	8.76%
9B	9.13%
9C	9.65%
9D	10.03%
9E	10.50%
9F	10.84%
A0	10.89%
A1	11.28%
A2	11.74%
A3	12.09%
A4	12.65%
A5	13.03%
A6	13.51%
A7	13.88%
A8	14.53%
A9	14.96%
AA	15.46%
AB	15.86%
AC	16.50%
AD	16.91%
AE	17.45%
AF	17.84%

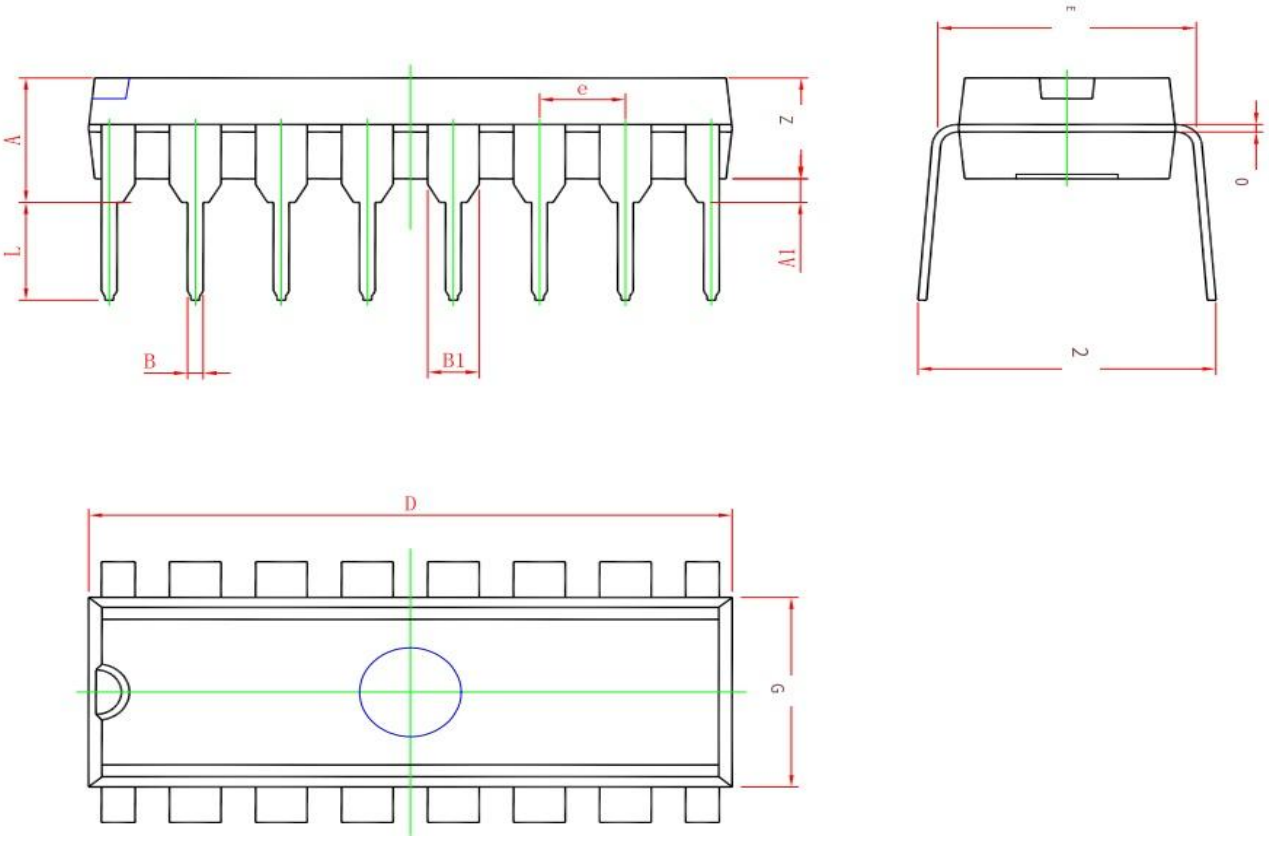
B0	18.38%
B1	18.81%
B2	19.35%
B3	19.79%
B4	20.48%
B5	20.91%
B6	21.49%
B7	21.93%
B8	22.65%
B9	23.13%
BA	23.70%
BB	24.15%
BC	24.81%
BD	25.25%
BE	25.38%
BF	25.88%
C0	25.88%
C1	26.38%
C2	26.50%
C3	27.00%
C4	27.63%
C5	28.13%
C6	28.75%
C7	29.25%
C8	30.13%
C9	30.63%
CA	31.25%
CB	31.88%
CC	32.63%
CD	33.13%
CE	33.88%
CF	34.38%
D0	35.13%
D1	35.63%
D2	36.38%
D3	37.00%
D4	37.75%
D5	38.38%
D6	39.13%
D7	39.75%
D8	40.75%
D9	41.38%
DA	42.13%
DB	42.75%
DC	43.75%

DD	44.38%
DE	45.25%
DF	45.88%
E0	45.88%
E1	46.63%
E2	47.38%
E3	48.13%
E4	49.13%
E5	49.75%
E6	50.63%
E7	51.38%
E8	52.50%
E9	53.25%
EA	54.25%
EB	55.00%
EC	56.13%
ED	56.88%
EE	57.75%
EF	58.63%
F0	59.50%
F1	60.38%
F2	61.38%
F3	62.25%
F4	63.38%
F5	64.25%
F6	65.38%
F7	66.25%
F8	67.63%
F9	68.63%
FA	69.75%
FB	70.75%
FC	72.00%
FD	72.88%
FE	74.00%
FF	75.00%

7. Package size

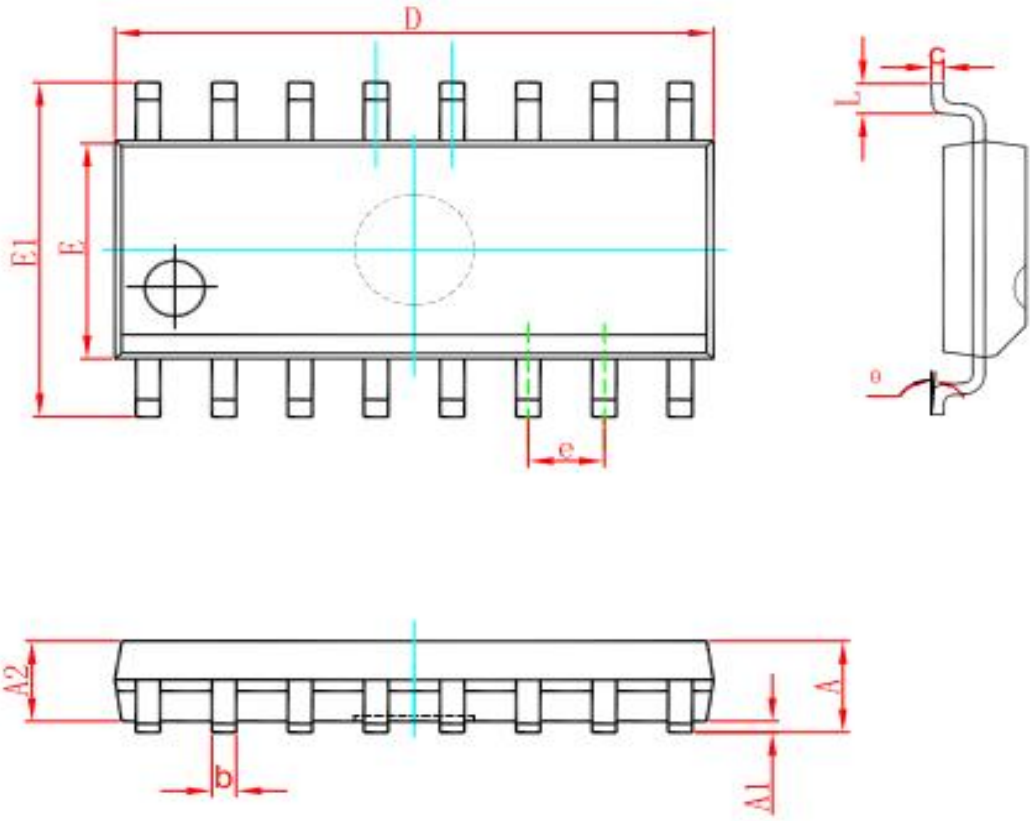
7.1 16PIN package size

DIP16



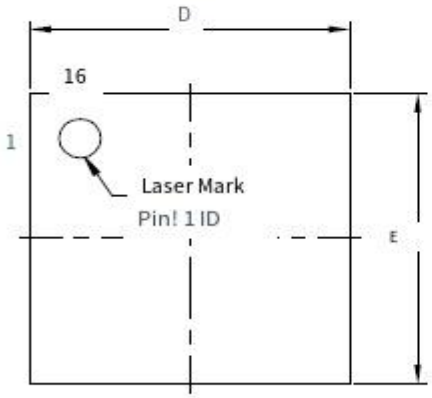
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.974	0.288	0.314
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

SOP16

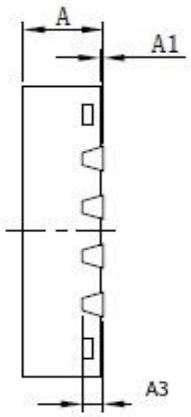


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

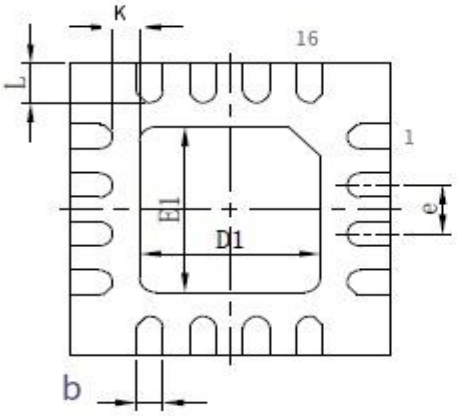
QFN16



Top View



Side View

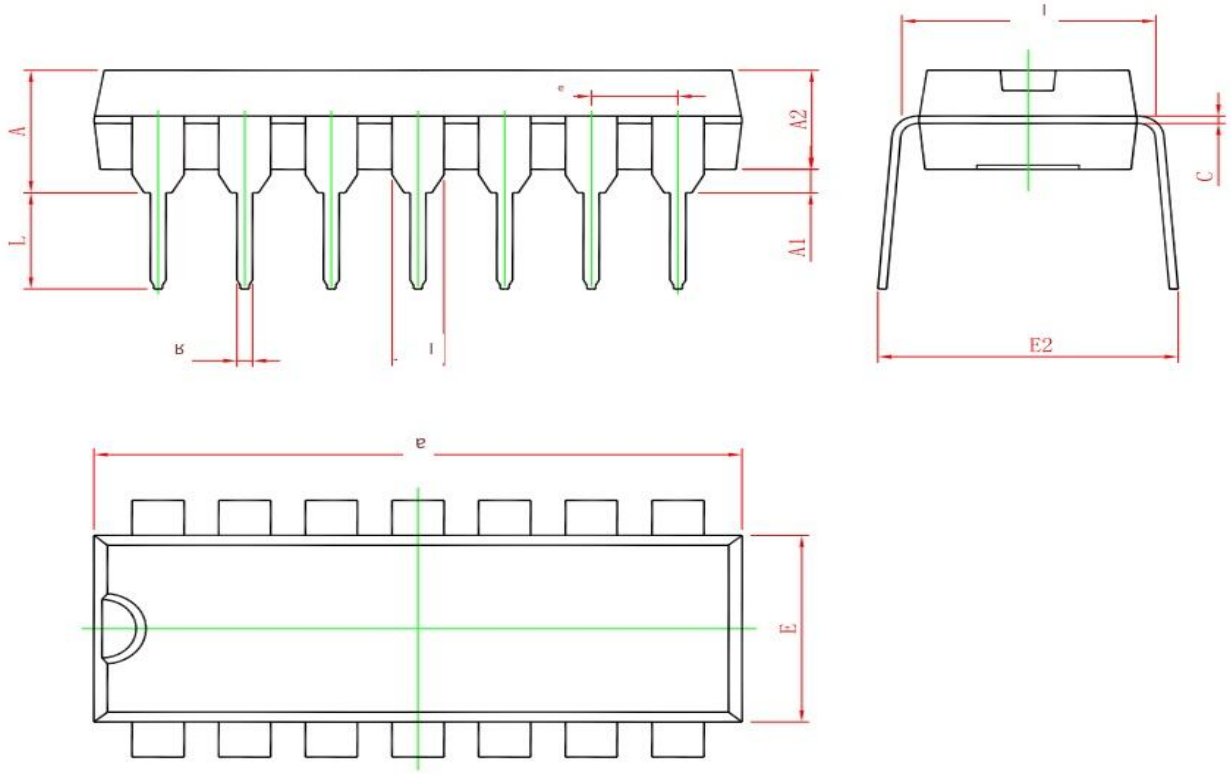


Bottom View

Size / Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
b	0.20	0.25	0.30
e	0.50 BSC		
K	0.300 REF		
L	0.30	0.35	0.40

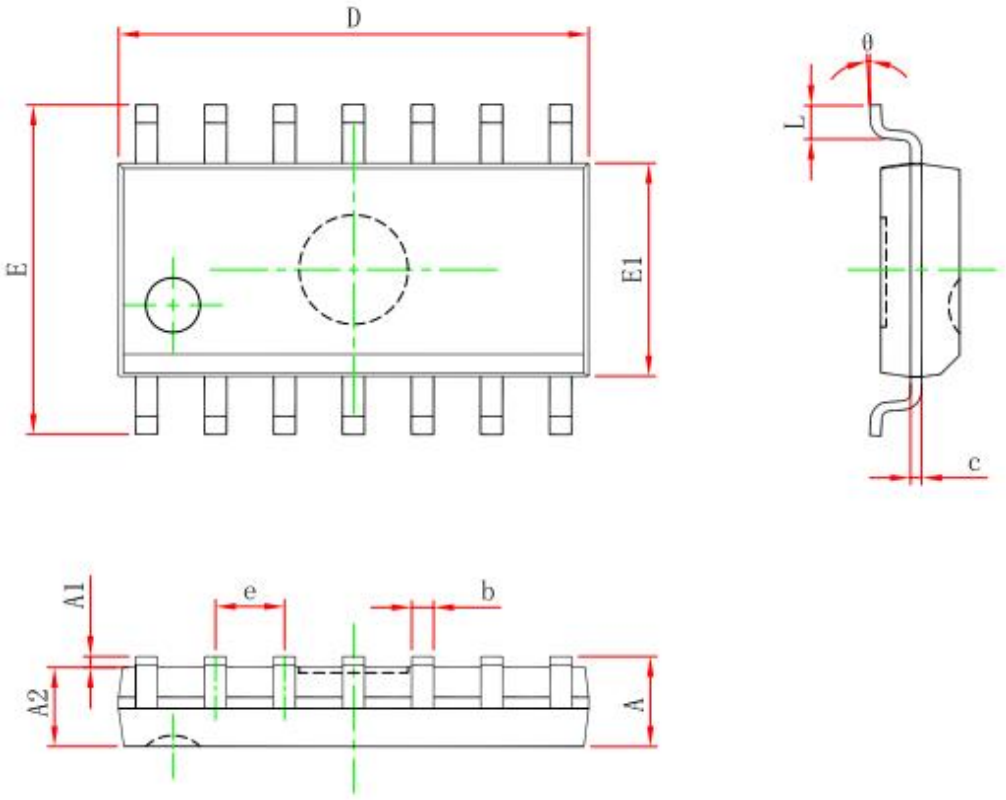
7.2 14PIN package size

DIP14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.974	0.288	0.314
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

SOP14



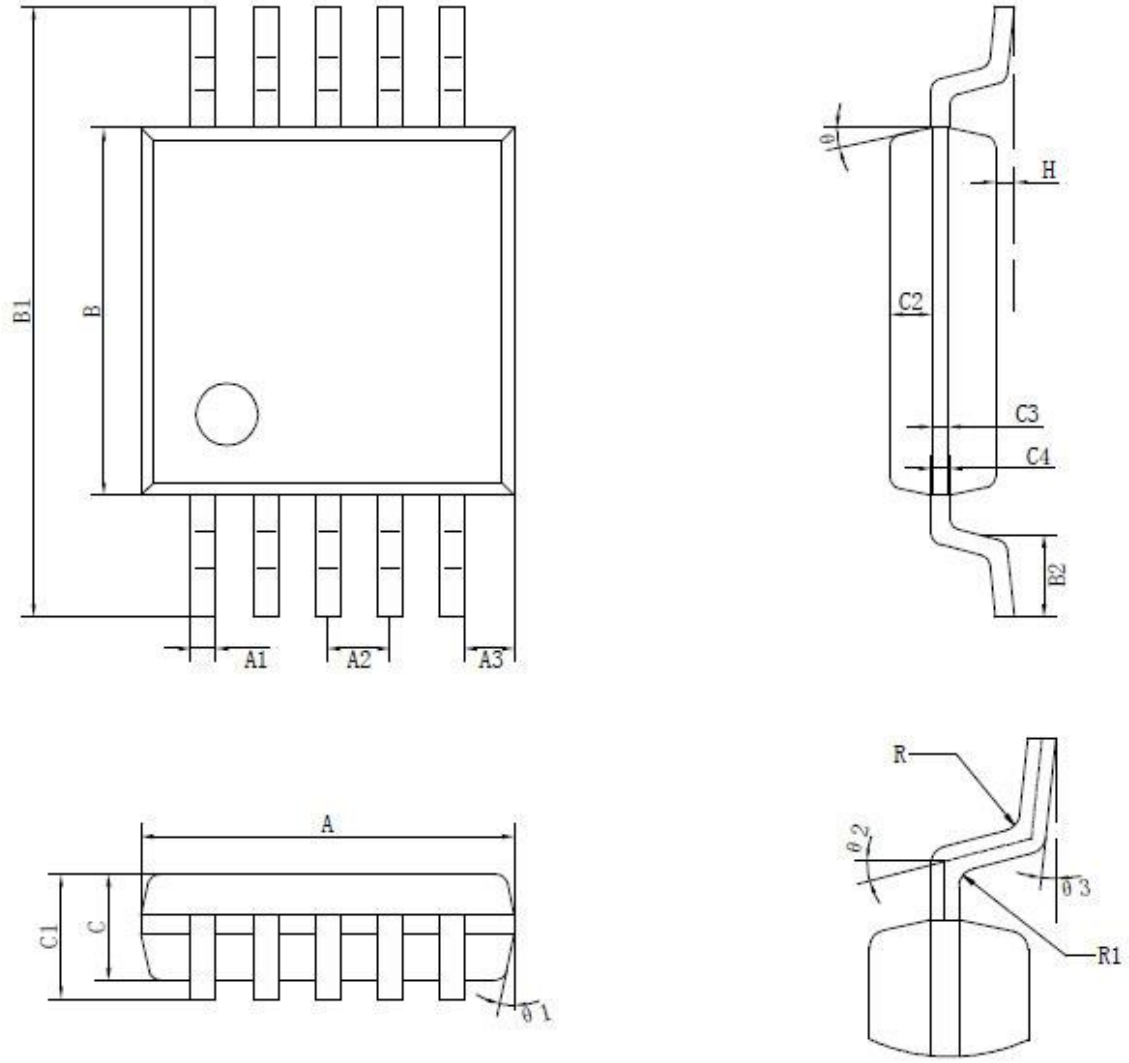
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	——	1.750	——	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	——	0.049	——
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

7.3 10PIN package size

MSOP10

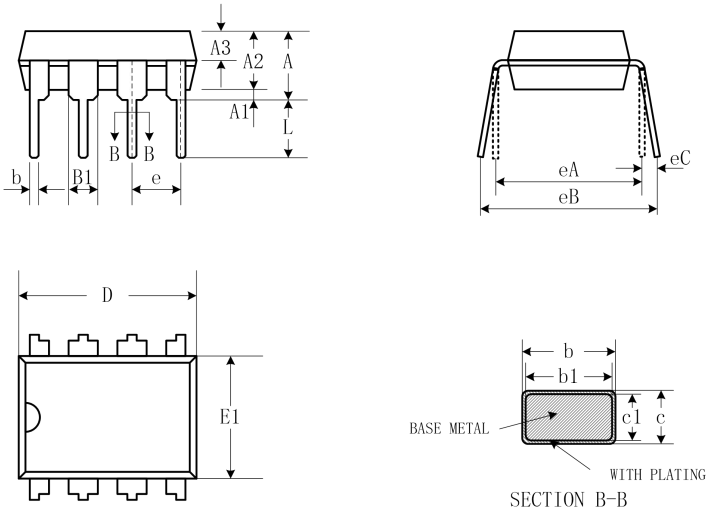
size / label	MAX(mm)	MIN(mm)	size / label	MIN(mm)	MAX(mm)
A	2.90	3.10	C3	0.152	
A1	0.18	0.25	C4	0.15	0.23
A2	0.50TYP		H	0.00	0.09
A3	0.40TYP		θ	15° TYP4	
B	2.90	3.10	θ1	12° TYP4	
B1	4.70	5.10	θ2	14° TYP	
B2	0.45	0.75	θ3	0° ~ 6°	
C	0.75	0.95	R	0.15TYP	
C1	--	1.10	R1	0.15TYP	
C2	0.328TYP				

* EISOP10 products share all data from this diagram, and the Diepad exposure is designed according to the lead frame



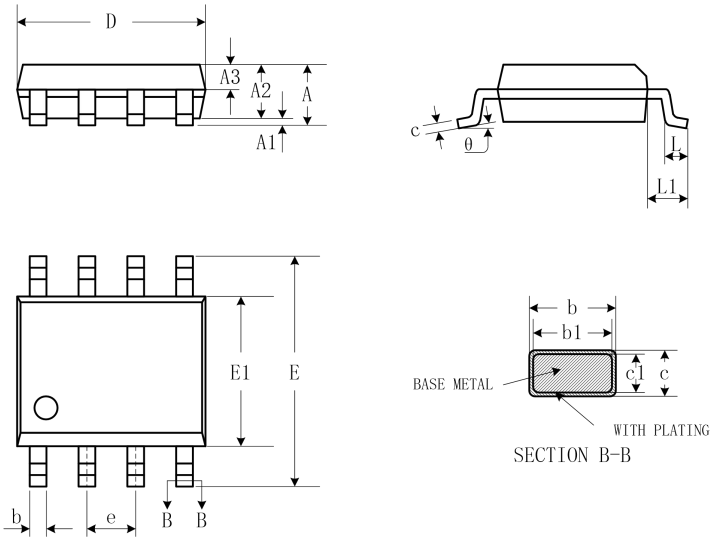
7.4 8PIN package size

DIP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	-	-
A2	3.10	3.30	3.50
A3	1.50	1.60	1.70
b	0.44	-	0.53
b1	0.43	0.46	0.48
B1	1.52 BSC		
c	0.25	-	0.31
c1	0.24	0.25	0.26
D	9.05	9.25	9.45
E1	6.15	6.35	6.55
e	2.54 BSC		
eA	7.62 BSC		
eB	7.62	-	9.50
eC	0	-	0.94
L	3.00	-	-

SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
L	0.50	0.65	0.80
L1	1.05 BSC		
Theta.	0	-	8 °