JZ8P2616

8-bit OTP Microcontroller

User Data Manual

Version V1.1

Revision History

Version Number	Modification Description	Remarks
V0.0	First Draft	
V1.0	Revised error descriptions, added model specifications, released the initial version	
V1.1	Revised error descriptions	

Notes:

1. To enter sleep mode, change the AD reference to VDD reference, that is, R1A7(ADCON1)=0x05; otherwise, power consumption will be high;

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1. Chip Introduction

1.1. Functional Features

CPU Configuration

- 2K×16-Bit OTP ROM
- 176×8-Bit SRAM
- 8-Level Stack Space
- 8-Level Programmable Voltage Reset (LVR)
  1.2V, 1.6V, 1.8V, 2.2V
  2.4V, 2.6V, 3.3V, 3.5V
- Operating current is < 3 mA (8MHz/5V)
- Working current is < 10 uA (36KHz/5V)
- Sleep current is < 1 uA (sleep mode)

I/O configuration

- 2 sets of 14 bidirectional IO ports: P5, P6
- Wake-up ports: P5, P6
- 14 programmable pull-up I/O pins
- 14 programmable pull-down I/O pins
- External interrupt: P60
- Reference voltage output: P65

Operating voltage

- Operating Voltage Range:
  V_{LVR}3.3V～5.5V|Fcpu=0～8MHz
  V_{LVR}2.2V～5.5V|Fcpu=0～4MHz
  V_{LVR}1.8V～5.5V|Fcpu=0～2MHz

Operating Frequency Range

- Internal IHRC Oscillation Circuit:
  32MHz/16MHz/8MHz/4MHz/1MHz
- Internal ILRC Oscillation Circuit: 36KHz
- Clock Cycle Division Selection:
  2T, 4T, 8T, 16T, 32T

Peripheral Module

- 14-channel 12Bit ADC (Analog-to-Digital Converter)
- 8 Bit Timer Counter TC0
- 3-channel 1 Group 10Bit-PWM (Two pairs of complementary)
- 4-channel 1 Group 10Bit-PWM (Two pairs of complementary)
- 1 Comparator CMP
- PWM7 can trigger AD sampling
- 2-channel RGB LED cascading controller (drives rainbow lights)

Interrupt sources

- TC0 Timer Interrupt
- TC1 Timer Interrupt
- TC2 Timer Interrupt
- External Interrupt
- P6 Port Input Change Interrupt
- P5 Port Input Change Interrupt
- ADC Conversion Complete Interrupt
- PWM7 Duty Cycle Match Interrupt
- CMP Status Change Interrupt

Features

- Programmable WDT Timer
- Four Operating Mode Switching

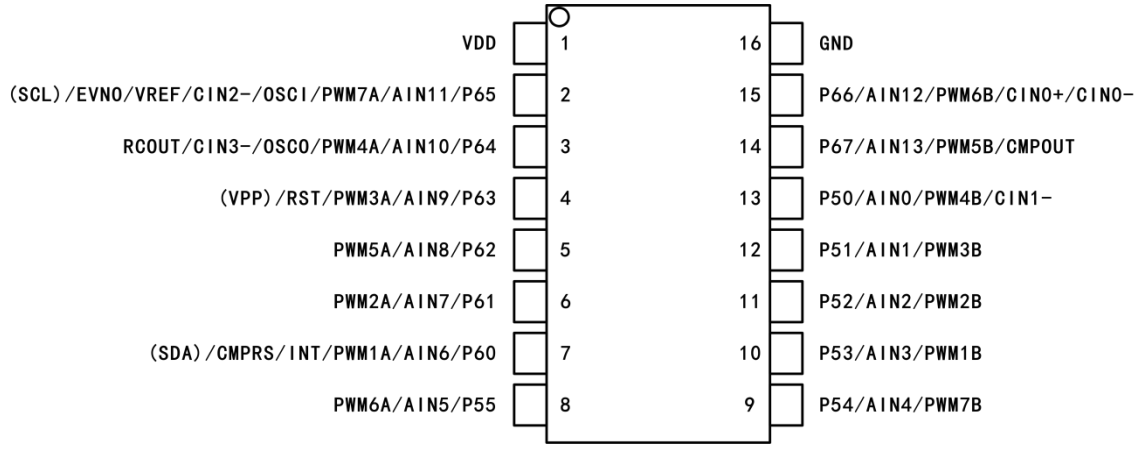
Package Type

- JZ8P2616-SOP16/ QFN16
- JZ8P2616-SOP14
- JZ8P2616-MSOP10
- JZ8P2616-SOP8

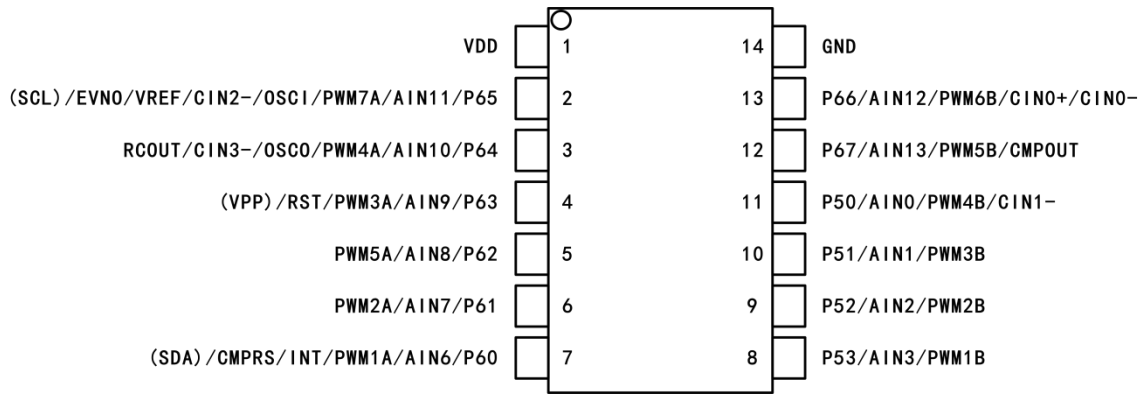
1.2. Model Description

PRODUCT	ROM	RAM	EEPROM	I/O	PWM	ADC	PACKAGE
JZ8P2616DE0	2K*16	176*8	-	14	7*10	14	SOP16
JZ8P2616Q16	2K*16	176*8	-	14	7*10	14	QFN16
JZ8P2616AC0	2K*16	176*8	-	12	7*10	12	SOP14
JZ8P2616MSOP10	2K*16	176*8	-	8	6*10	8	MSOP10
JZ8P2616C0	2K*16	176*8	-	6	6*10	6	SOP8

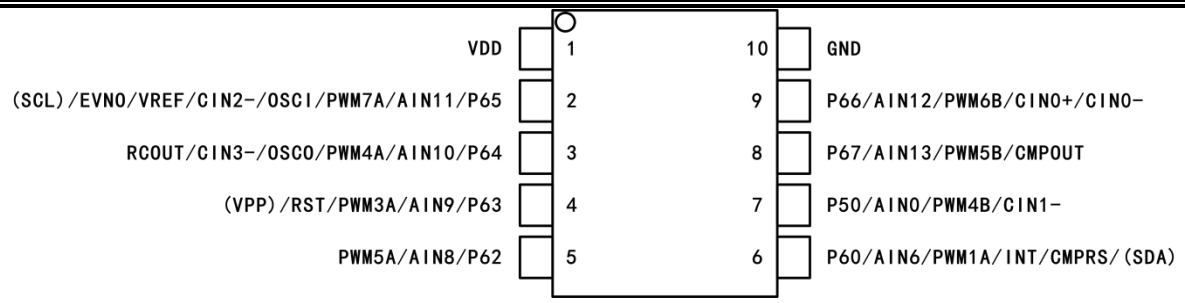
1.3. Pin assignment



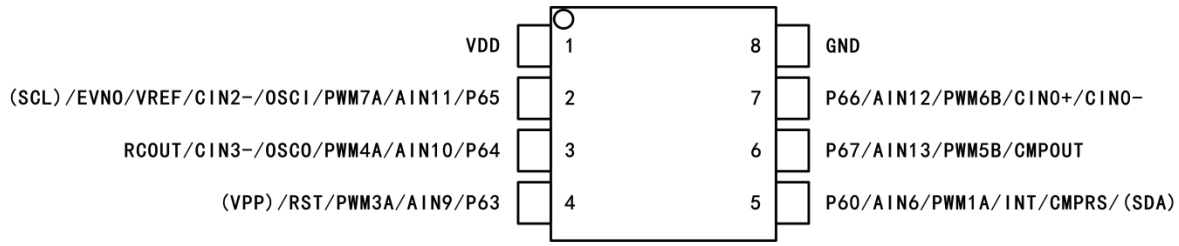
JZ8P2616-16PIN pinout



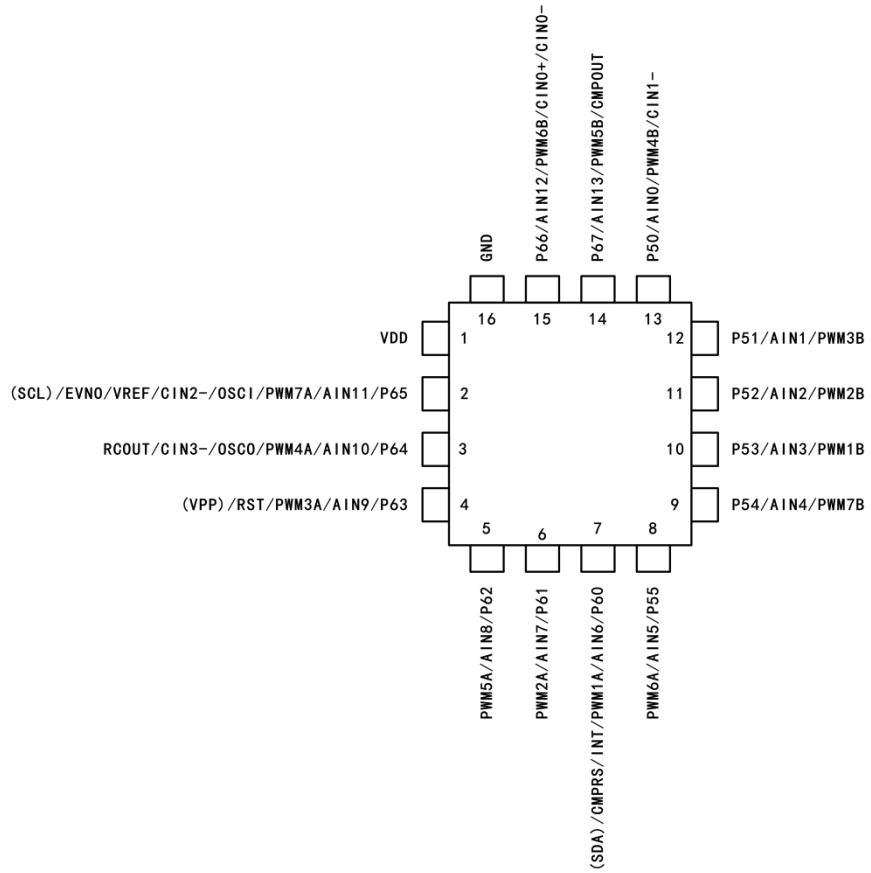
JZ8P2616-14PIN pinout



JZ8P2616-10PIN pinout



JZ8P2616-8PIN Pin Configuration



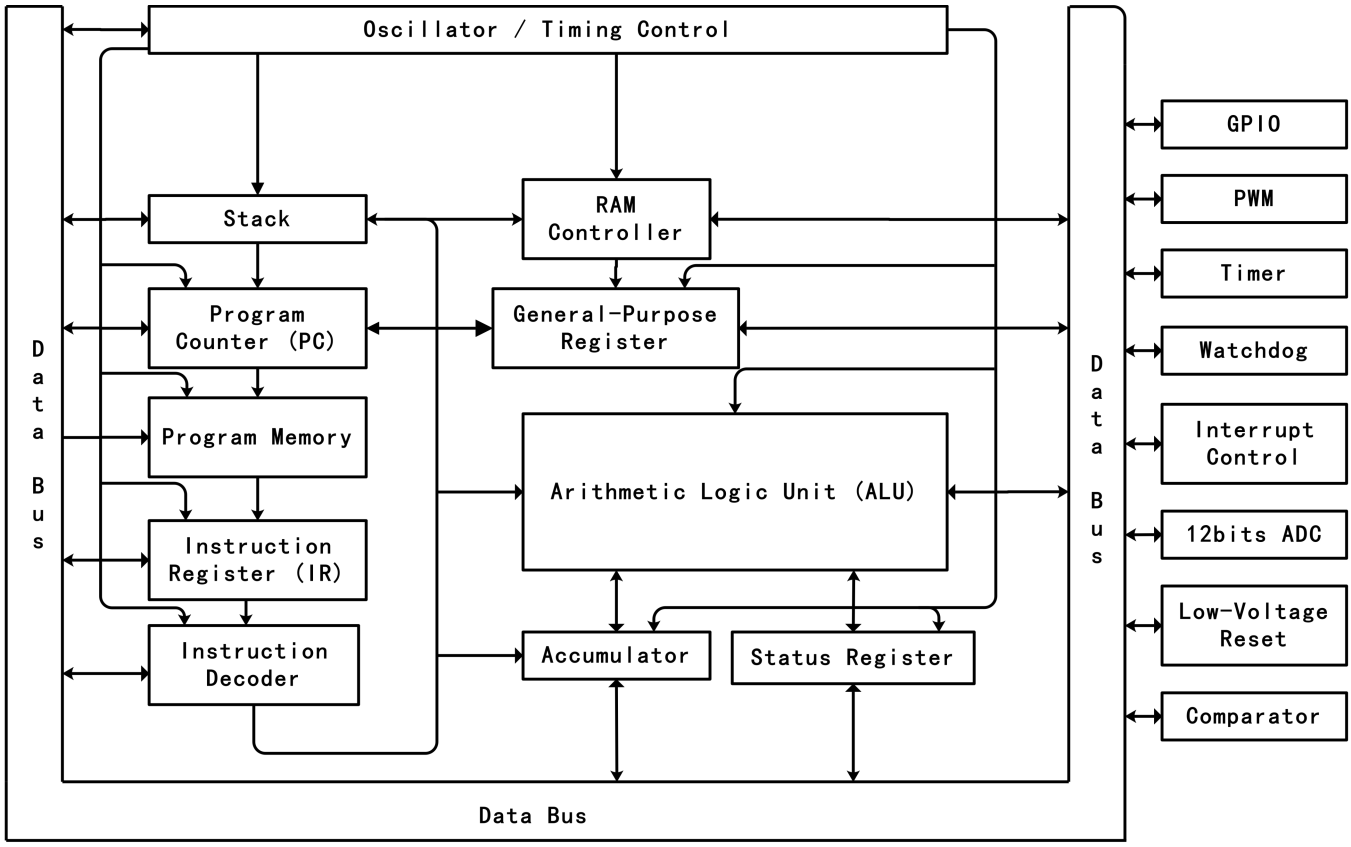
JZ8P2616-QFN16 Pin Configuration

1.4. Pin Description

Serial Number	Pin Name	I/O	Function Description
P50	P50	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN0	AN	Analog Input Channel
	PWM4B	O	PWM4B Output
	CIN1-	AN	Comparator Negative Input
P51	P51	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN1	AN	Analog Input Channel
	PWM3B	O	PWM3B Output
P52	P52	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN2	AN	Analog Input Channel
	PWM2B	O	PWM2B Output
P53	P53	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN3	AN	Analog Input Channel
	PWM1B	O	PWM1B Output
P54	P54	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN4	AN	Analog Input Channel
	PWM7B	O	PWM7B output
P55	P55	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN5	AN	Analog Input Channel
	PWM6A	O	PWM6A output
P60	P60	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN6	AN	Analog Input Channel
	PWM1A	O	PWM1A output
	INT	I	External interrupt INT input port
	CMPRS	I	CMP Comparator Voltage Divider Input Source
P61	P61	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN7	AN	Analog Input Channel
	PWM2A	O	PWM2A Output

P62	P62	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN8	AN	Analog Input Channel
	PWM5A	O	PWM5A Output
P63	P63	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN9	AN	Analog Input Channel
	PWM3A	O	PWM3A Output
	RST	I	External Reset Input Port
	VPP	I	Programming High Voltage Port
P64	P64	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN10	AN	Analog Input Channel
	PWM4A	O	PWM4A output
	CIN3-	I	Comparator Negative Input
	OSCO	I	Crystal oscillator port
	RCOUT	O	Internal instruction clock frequency output
P65	P65	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN11	AN	Analog Input Channel
	PWM7A	O	PWM7A output
	OSCI	I	Crystal oscillator port
	CIN2-	AN	Comparator Negative Input
	VREF	AN	ADC external reference voltage input
	EVNO	I	1/4 sampling voltage analog input channel
P66	P66	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN12	AN	Analog Input Channel
	PWM6B	O	PWM6B output
	CIN0-	AN	Comparator Negative Input
	CIN0+	AN	Comparator positive input port
P67	P67	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhancement
	AIN13	AN	Analog Input Channel
	PWM5B	O	PWM5B output
	CMPOUT	O	Comparator result output
	VDD	--	Power Supply
	GND	--	Ground

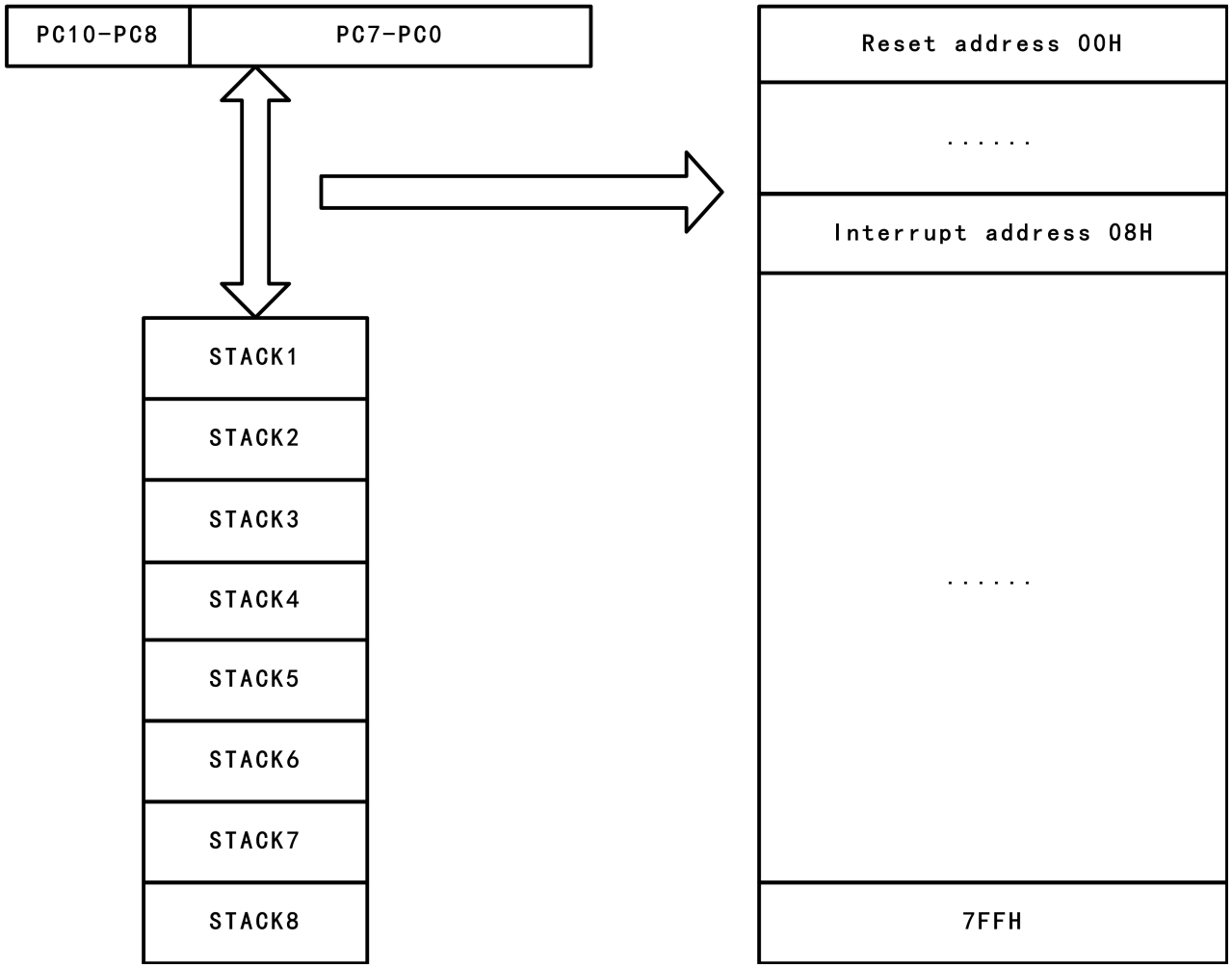
1.5. System Block Diagram



System Circuit Block Diagram

2. Central Processing Unit

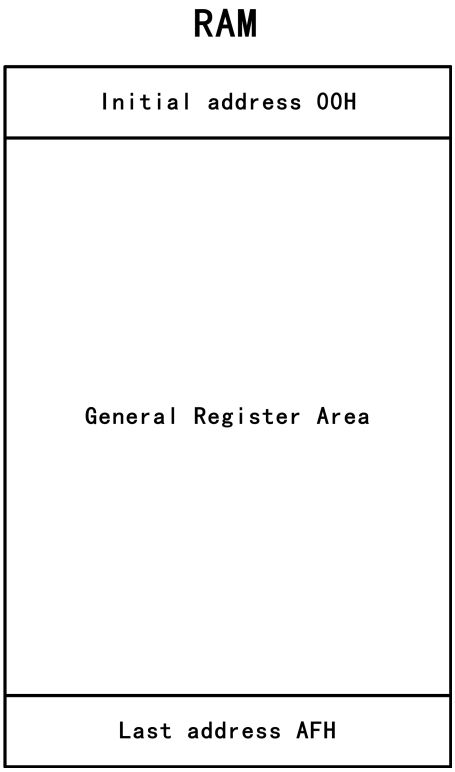
2.1. Program Storage Area Structure



Program Storage Area Structure Diagram

2.2. Data Storage Area

2.2.1. Data Storage Area Structure



Data Storage Area

2.2.2. Overview of Special Function Registers

Address	0X18_	0X19_	0X1A_	0X1B_	0X1C_	0X1D_	0X1E_	0X1F_
0	RSR	P5PH	P5AE	TC1CON				
1	PCH	P6PH	P6AE	TC1PRDL				
2	PCL			PWM1DTL	PWM7DTL			
3	STATUS	P5PD	ADATH	PWM2DTL	PWM7CON			
4	TC0CON	P6PD	ADATL	PWM3DTL				
5	TC0C		ADCON0	TC1PRDTH				
6	TBRDH		ADCON1			INTE0		
7	TBRDL	P6OD		PWMCON1				
8	CPUCON			TC2CON	CMPCON0			
9	IHRCCAL			TC2PRDL	CMPCON1			
A (10)	P5			PWM4DTL		INTF0		
B (11)	P6			PWM5DTL				
C(12)		P5IWE		PWM6DTL				
D(13)	P5CON	P6IWE	TPRE	TC2PRDTH				
E(14)	P6CON		EXINTCON					
F(15)			WDTCON	PWMCON2				IAR

2.3. Special System Register

2.3.1. Indirect Addressing

The data memory can be addressed directly or indirectly, and indirect addressing operations can be achieved through the IAR register.

The RSR register is used in conjunction with the R1FF register to implement indirect addressing operations. Users can place the address corresponding to a certain SRAM into the RSR register, and then access the indirect addressing register R1FF; at this point, the address will point to the SRAM corresponding to the address in RSR.

IAR is not an actual existing register; its main function is to serve as a pointer for indirect addressing. Any instruction that uses R1FF (IAR) as a pointer will actually correspond to the data pointed to by R180 (RAM Selection Register) RSR<7:0>.

Example: Indirect Addressing Clear RAM (0x00～0xAF)

```
    MOV    A,@0X00
    MOV    RSR,A       // The indirect addressing pointer points to 00H
    CLR    IAR         // Clear the data pointed to by the address 00H
    INC    RSR         // Address +1
    MOV    A, RSR
    XOR    A, @0XAF
    JBTS   STATUS, 2
    JMP    $-5         // Jump back 5 instructions, continuously clear until RSR
                       // points to AFH
    CLR    0XFF        // Clear the data pointed to by the address FFH
```

2.3.1.1. R180/RSR (RAM select register)

0X180	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSR	RSR<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

RSR<7:0> is used to select the SRAM address in indirect addressing mode (addressing range: 0X00－0XAF).

The RSR register is used in conjunction with the R1FF register to implement indirect addressing operations. Users can place the address corresponding to a certain SRAM into the RSR register, and then access the indirect addressing register R1FF; at this point, the address will point to the SRAM corresponding to the address in RSR.

2.3.1.2. R1FF/IAR (Indirect Addressing Register)

0X1FF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAR	IAR<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

The Indirect Addressing Register is not an actual register; its main function is to serve as a pointer for indirect addressing. Any instruction using R1FF as a pointer actually points to the data in the SRAM indicated by RSR<7:0> at address R180 (RAM Select Register).

2.3.2. Lookup Table

2.3.2.1. Jump Table

The program counter (PC) controls the execution order of the program instructions and can address the entire ROM range. The PC automatically increments by 1 after executing an instruction, always pointing to the address of the next instruction. When performing operations such as jumps, conditional jumps, PCL assignments, subroutine calls, interrupt triggers, and returns, the PC automatically loads relevant addresses instead of just the next instruction address.

The jump table allows for multi-address jumping functionality, where the new PCL value is obtained by adding the values of PCL and ACC for multi-address jumps. For example, if ACC=1, it indicates that the current address is PCL+1. It is important to note that jumps should not exceed the range to avoid functionality issues.

Example 1: Jump table returns value 0X4F

```
MOV    A,@0X03
ADD    PCL,A
RETL   @0X3F //0
RETL   @0X06 //1
RETL   @0X5B //2
RETL   @0X4F //3
RETL   @0X66 //4
```

Example 2: Jump program LOOP2

```
MOV    A,@0X02
ADD    PCL, A
JMP    LOOP0  //0
JMP    LOOP1  //1
JMP    LOOP2  //2
JMP    LOOP3  //3
```

2.3.2.1.1. R181/PCH (Program Counter High Byte Register)

0X181	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCH	-	-	-	-	-	PC<10:8>		
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

2.3.2.1.2. R182/PCL (Program Counter Low Byte Register)

0X182	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCL	PC<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

The program counter (PC) is a pointer used to record the instructions that the CPU needs to process during each instruction cycle. During the CPU operation cycle, the PC advances the instruction pointer to the program memory, and then the pointer increments by 1 to enter the next cycle. The JZ8P2616 has an 11-bit wide program counter (PC), with its low byte coming from the read/write PCL register and its high byte coming from the readable PCH register.

The stack is used to record the instruction pointer returned by the program. When a subroutine is called, the PC pushes the instruction pointer onto the stack. When executing the return instruction, the stack sends the instruction pointer back to the PC, continuing the original process. The JZ8P2616 has an 8-level stack that occupies neither program storage space nor data storage space, and the stack pointer cannot be read or written.

The program counter (PC) and the stack are described in detail as follows:

(1) The register PC and the built-in 8-level stack are both 11 bits wide, used for addressing the 2K×16Bit MTP ROM.

(2) Generally, the PC increments by one; on reset, all bits of the PC are cleared to zero.

(3) The "JMP" instruction allows loading an 11-bit address directly, then pushes PC+1 onto the stack. Therefore, the JMP instruction allows the PC to jump to any position in the program.

(4) The "CALL" instruction allows loading an 11-bit address into the PC, then pushes PC+1 onto the stack. Thus, the entry address of the subroutine can be located at any position in the program.

(5) Executing the "RET" instruction sends the top data from the stack to the PC.

(6) Executing the "ADD PCL,A" instruction adds a relative address to the current PC, with each bit from the ninth bit onward incrementing sequentially.

(7) Executing the "MOV PCL,A" instruction loads an address from the "A" register into the low 8 bits of the PC, while the ninth bit and above remain unchanged.

(8) Any instruction that writes a value to PCL (excluding the "ADD PCL,A" instruction) (e.g., "MOV PCL,A", "BTC PCL,1") keeps the ninth and tenth bits of the PC unchanged.

(9) The operation of the stack is similar to that of a circular buffer, meaning that after pushing data onto the stack 8 times, the data pushed during the 9th operation will overwrite the data from the 1st operation, and the data from the 10th operation will overwrite the data from the 2nd operation, and so on.

2.3.3. ROM Area Lookup

The TBRDH and TBRDL registers can be used with the TBRD instruction to query data from the ROM area address. The high 8 bits of the queried data are saved to a custom register, while the low 8 bits are stored in the ACC.

Example 1: The 16-bit data queried from ROM address 0X00F3 is 0X339E

```
    MOV    A,@0x00
    MOV    TBRDH,A
    MOV    A,@0xF3
    MOV    TBRDL,A
    TBRD   reg_tempH      // High 8 bits saved to reg_tempH,low 8 bits saved
                          // to ACC
    MOV    reg_tempL,A    // ACC value saved to reg_tempL
Table:
    ORG    0X00F0         // Fixed ROM program starting address is 0X00F0
    DW     0X00F3         // 0
    DW     0X1103         // 1
    DW     0X22BC         // 2
    DW     0X339E         // 3
    DW     0X444E         // 4
```

Example 2: Unknown address, query data 0X1103 based on label

```
    MOV    A,@Table/256   // High byte of address data
    MOV    TempH,A        // Save high 8 bits of data in TempH
    MOV    A,@Table+1     // Low byte of address data
    MOV    TempL,A        //The lower 8 bits of the data are stored in TempL
    Table:
    DW     0X00F3 // 0
```

```
DW      0X1103 // 1
DW      0X22BC // 2
DW      0X339E // 3
DW      0X444E // 4
```

2.3.3.1. R186/TBRDH (Lookup Pointer High Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	PWM4_LEDEN	PWM1_LEDEN	-	VDD_POWER	-	RBIT<10:8>		
Read/Write	R/W	R/W	R	R/W	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<2:0>: RBIT<10:8> - TBRD Pointer Address High 3 Bits. (bit4 must be 1)

2.3.3.2. R187/TBRDL (Lookup Pointer Low Register)

0X187	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDL	RBIT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: RBIT<7:0>-TBRD pointer address low 8 bits, RBIT<7:0> is used to select the low 8 bits of the look-up ROM address in the table lookup method.

2.3.4. Status Register

2.3.4.1. R183/STATUS (Status Flag Register)

0X183	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	RST	GIE	-	T	P	Z	DC	C
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	1	1	X	X	X

Bit<7>: RST - Reset or Wake-up Flag Bit

0: Other reset types

1: Wake-up by pin state change

Bit<6>: GIE - Interrupt Enable Flag

0: Masked by DIT instruction or hardware interrupt

1: Interrupt enabled by EIT/RTI instruction

Bit<5>: Not used

Bit<4>: T-time overflow bit

0: WDT overflow

1: Executing "SLEEP" and "CWDT" instructions or low-voltage reset

Bit<3>: P-power down flag

0: Executing "SLEEP" instruction

1: Power-on reset or executing "CWDT" instruction

Events affecting T/P are shown in the table below:

Type	RST	T	P
Power-on Reset	0	1	1
Press RESET in Working Mode	0	Hold	Hold
RESET Wakeup	0	1	0
WDT Overflow in Working Mode	0	0	Hold
WDT Overflow Wakeup	0	0	0
Port Input Change Wakeup	1	1	0
Execute CWDT Instruction	Hold	1	1
Execute SLEEP Instruction	Hold	1	0

Bit<2>: The Z (zero) flag is set to "1" when the result of an arithmetic or logical operation is zero.

0: When the result of arithmetic or logical operations is not 0

1: When the result of arithmetic or logical operations is 0

Bit<1>: DC-Auxiliary Carry Flag

0: No carry occurs in the low four bits during addition; / borrowing occurs in the low four bits during subtraction

1: Carry occurs in the low four bits during addition; / no borrowing occurs in the low four bits during subtraction

Bit<0>: C-Carry Flag

0: No carry occurs in the high four bits during addition; / borrowing occurs in the high four bits during subtraction

1: Carry occurs in the high four bits during addition; / no borrowing occurs in the high four bits during subtraction

2.3.5. Power Domain

VDD provides power domain selection to enhance anti-interference; users can configure whether to enable enhanced anti-interference capability.

2.3.5.1. R186/TBRDH (Power Domain Selection Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	PWM4_LEDEN	PWM1_LEDEN	-	VDD_POWER	-	RBIT<10:8>		
Read/Write	R/W	R/W	R	R/W	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<4>: VDD_POWER - VDD Power Domain Interference Selection (bit4 must be 1)

0: Disable

1: Enable

3. I/O Ports

JZ8P2616 has 2 sets of bidirectional I/O ports, with a total of 14 inputs and 14 outputs, most of which can be reused for other functions.

14 programmable pull-up I/O pins: P50～P55, P60～P67;

14 programmable pull-down I/O pins: P50～P55, P60～P67;

14 selectable pull current enhancing I/O pins: P50～P55, P60～P67;

14 selectable sink current enhancing I/O pins: P50～P55, P60～P67;

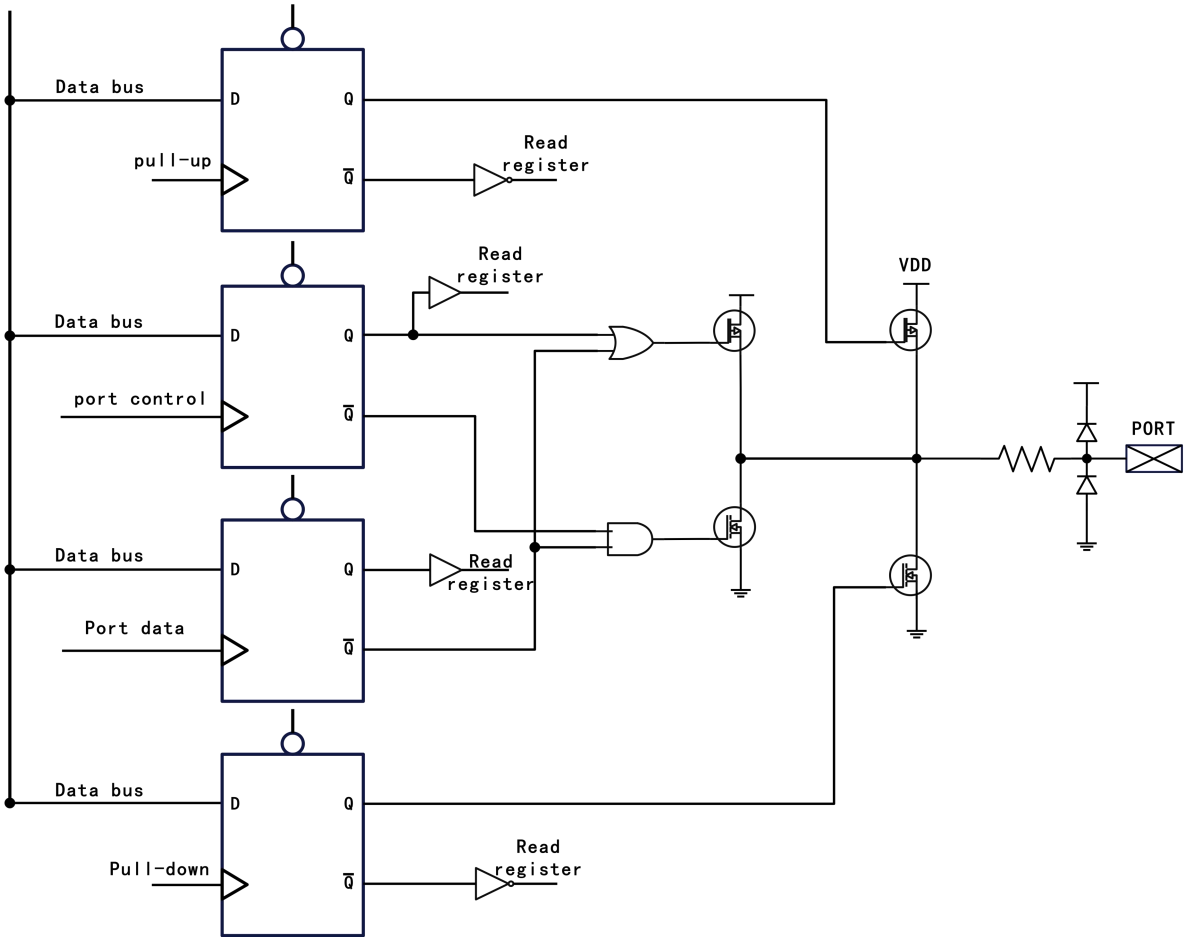
14 programmable wake-up I/O pins: P50 to P55, P60 to P67;

14 programmable analog ports: P50 to P55, P60 to P67;

8 programmable open-drain I/O pins: P60 to P67;

3.1. GPIO internal structure diagram

The following internal structure diagram is for reference only and does not represent the actual circuit.



IO control register/data register/pull-up/pull-down structure circuit

3.2. P5 port

The P5 port is an 8-bit wide bidirectional port. The corresponding direction control register is P5CON. Setting a bit in P5CON to 1 (=1) configures the corresponding pin as an input. Clearing a bit in P5CON (=0) configures the corresponding P5 pin as an output.

The data register corresponding to the P5 port is PORT5. When the port is configured as an input, reading the PORT5 register reads the state of the pins; when the port is an output, reading the PORT5 register reads the data from P5.

The registers related to the P5 port include PORT5, P5CON, P5PH, P5PD, P5IWE, P5AE, etc.

3.2.1. R18A/P5 (P5 data register)

0X18A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5	-	-	P5<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 port data control

3.2.2. R18D/P5CON (P5 control register)

0X18D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5CON	-	-	P5CON<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port input/output control bits:

0: Output

1: Input

3.2.3. R190/P5PH (P5 pull-up control register)

0X190	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PH	-	-	P5PH<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port pull-up control bit:

0: Enable

1: Disable

3.2.4. R193/P5PD (P5 pull-down control register)

0X193	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PD	-	-	P5PD<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port pull-down control bit:

0: Enable

1: Disable

3.2.5. R19C/P5IWE (P5 input change interrupt, wake-up enable register)

0X19C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5IWE	-	-	P5IWE<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 port input change wake-up control bits:

0: Disable

1: Enable

3.2.6. R1A0/P5AE (P5 analog port enable register)

0X1A0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5AE	-	-	P5AE<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 port analog selection control bits:

0: Port set to GPIO

1: Port set to analog input

3.3. P6 port

P6 port is an 8-bit wide bidirectional port. The corresponding direction control register is P6CON. Setting a bit of P6CON to 1 (=1) will configure the corresponding pin as input. Clearing a bit of P6CON to 0 (=0) will configure the corresponding P6 pin as output.

The data register corresponding to port P6 is PORT6. When the port is an input port, reading the PORT6 register retrieves the state of the pins. When the port is

an output port, reading the PORT6 register retrieves the data from port P6.

The registers related to the P6 port include PORT6, P6CON, P6PH, P6PD, P6OD, P6IWE, and P6AE.

3.3.1. R18B/P6 (P6 Data Register)

0X18B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6	P6<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 Port Data Control

3.3.2. R18E/P6CON (P6 Control Register)

0X18E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6CON	P6CON<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 Port Input/Output Control Bits:

0: Output

1: Input

3.3.3. R191/P6PH (P6 Pull-Up Control Register)

0X191	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PH	P6PH<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port pull-up control bits:

0: Enable

1: Disable

3.3.4. R194/P6PD (P6 pull-down control register)

0X194	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PD	P6PD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port pull-down control bits:

0: Enable

1: Disable

3.3.5. R197/P6OD (P6 open-drain control register)

0X197	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6OD	P6OD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 port drain open circuit output control bit:

0: Disable

1: Enable

3.3.6. R19D/P6IWE (P6 Input Change Interrupt, Wakeup Enable Register)

0X19D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6IWE	P6IWE <7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 Port Input Change Wakeup Control Bits:

0: Disable

1: Enable

3.3.7. R1A1/P6AE (P6 Analog Port Enable Register)

0X1A1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6AE	P6AE <7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 Port Analog Selection Control Bits:

0: Port set to GPIO

1: Port set to analog input

3.4. Port Input Change Wakeup

JZ8P2616 includes 14 programmable port input change wakeup I/O: P50 to P55, P60 to P67. The chip can enter sleep mode or idle mode by executing the "SLEEP" instruction. At this time, the CPU does not execute instructions. Port input change wakeup can proceed with the original process (execute DI before SLEEP) or execute the corresponding interrupt jump (execute EI before SLEEP) through program selection. The corresponding interrupt enable control must be turned on, and after port input change wakeup, it jumps to the interrupt service routine.

Port State Change Query Wakeup Settings:

1. Set the port input change wake-up pin as input;
2. The internal pull-up or pull-down for the wake-up pin can be selected as needed;
3. Enable port input change wake-up control P5IWE/P6IWE;
4. Execute the DI instruction and do not enter the interrupt address pin;
5. Execute the "SLEEP" instruction; IDLE=0 to enter sleep mode or IDLE=1 to enter idle mode;
6. After waking up, execute the next instruction of SLEEP;

Port status change interrupt mode wake-up settings:

1. Set the port input change wake-up pin as input;
2. The internal pull-up or pull-down for the wake-up pin can be selected as needed;
3. Enable port input change wake-up control P5IWE/P6IWE;
4. Enable port input change interrupt P5ICIE/P6ICIE;
5. Execute the "EI" instruction and wait to enter the interrupt address pin;
6. Execute the "SLEEP" instruction; IDLE=0 to enter sleep mode or IDLE=1 to enter idle mode;
7. After waking up, it will enter the interrupt address, and after exiting the interrupt, it will execute the next instruction of SLEEP;

3.5. Schmitt-trigger parameters of the port

The Schmitt characteristics of JZ8P2616 port are as follows (for reference only):

Port	SMT	
P50～P55	0.23*VDD	0.51*VDD
P60～P67	0.23*VDD	0.51*VDD

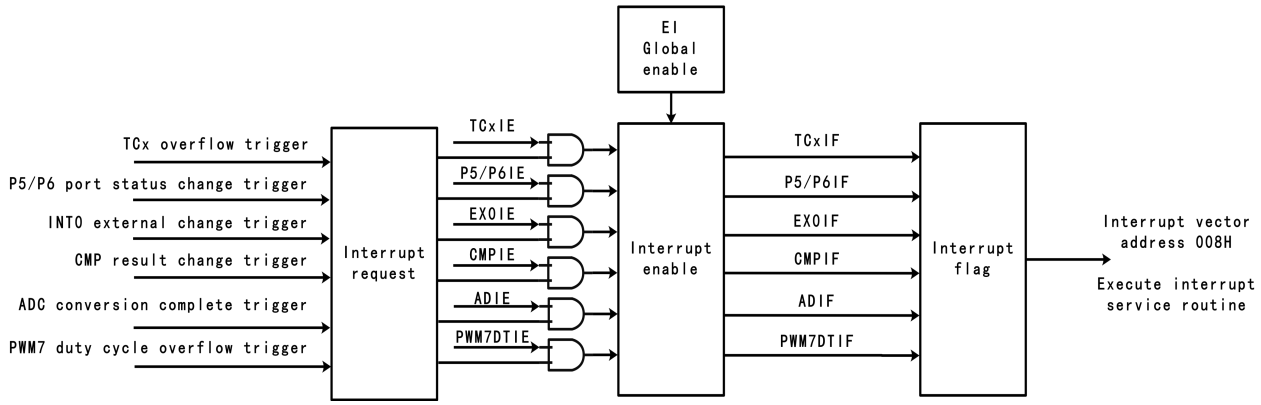
The above parameters are for reference only. Please refer to the actual measurement data of the target prototype.

4. Interrupt

The JZ8P2616 has 9 interrupt sources. Regardless of which interrupt is used, the global interrupt must be enabled, which means the "EI" instruction must be used. The interrupt vector address is fixed at 008H. Below are the characteristics of each interrupt:

Interrupt sources	Enable Conditions	Interrupt Flag
TC0 Overflow Interrupt	EI + TC0IE=1	TC0IF
TC1 Overflow Interrupt	EI + TC1IE=1	TC1IF
TC2 Overflow Interrupt	EI + TC2IE=1	TC2IF
P5 port input change interrupt	EI + P5ICIE=1	P5ICIF
P6 port input change interrupt	EI + P6ICIE=1	P6ICIF
INT external interrupt	EI + EX0IE=1	EX0IF
CMP Comparison Complete Interrupt	EI + CMPIE=1	CMPIF
ADC Conversion Complete Interrupt	EI + ADIE=1	ADIF
PWM7 Duty Cycle Overflow Interrupt	EI + PWM7DTIE=1	PWM7DTIF

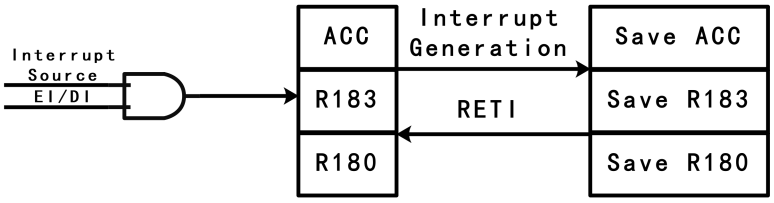
R1DA is the interrupt flag register, which records the interrupt flag bits after an interrupt request is generated by a specific interrupt. R1D6 is the interrupt enable control register, where the permission to enable or disable interrupts is set in these two registers. The overall interrupt enablement is done through the "EI" instruction, while conversely, the overall interrupt disablement is done through the "DI" instruction. When an interrupt occurs, the execution of the next instruction will start from the interrupt vector address 008H. The corresponding interrupt flag bits must be cleared before exiting the interrupt service routine to avoid erroneous interrupt actions.



Interrupt Principle Schematic

4.1. Interrupt Context Protection

During the interrupt response process, the hardware has a built-in interrupt protection feature that saves the contents of ACC, R183, and R180 until exiting the interrupt service routine, at which point the saved values are reloaded into ACC, R183, and R180. This is to avoid any instructions that may change the values of ACC, R183, and R180 while executing the interrupt subroutine, which could lead to errors when returning to the main program. As shown in the following diagram:



Interrupt Context Protection Schematic

4.2. Interrupt-Related Registers

4.2.1. R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	-	INTWE	INTIF	INTIE	INTEDG	INTEN	INTGATE	CMPGATE
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: Unused

Bit<5>: INTIF - External Interrupt Flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<4>: INTIE - External Interrupt Enable

0: Disable

1: Enable

Bit<3>: INTEDG - External Interrupt Trigger Edge Selection

0: Falling edge

1: Rising Edge

Bit<2>: INTEN - P60 External Interrupt Enable Bit

0: Disable

1: Enable

4.2.2. R1D6/INTE0 (Interrupt Enable Control Register)

0X1D6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE0	PWM7DTIE	ADIE	CMPIE	P6ICIE	P5ICIE	TC2IE	TC1IE	TC0IE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM7DTIE - PWM7 duty cycle match interrupt enable bit

0: Disable

1: Enable

Bit<6>: ADIE - AD conversion complete interrupt enable bit

0: Disable

1: Enable

Bit<5>: CMPIE - CMP comparator result change interrupt enable bit

0: Disable

1: Enable

Bit<4>: P6 ICIE - P6 port change interrupt enable bit

0: Disable

1: Enable

Bit<3>: P5 ICIE - P5 port change interrupt enable bit

0: Disable

1: Enable

Bit<2>: TC2IE - TC2 period match interrupt enable bit

0: Disable

1: Enable

Bit<1>: TC1IE - TC1 period match interrupt enable bit

0: Disable

1: Enable

Bit<0>: TC0IE - TC0 Overflow Interrupt Enable Bit

0: Disable

1: Enable

4.2.3. R1DA/INTF0 (Interrupt Flag Register)

0X1DA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF0	PWM7DTIF	ADIF	CMPIF	P6ICIF	P5ICIF	TC2IF	TC1IF	TC0IF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM7DTIF - PWM7 Duty Cycle Interrupt Flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<6>: ADIF - Analog-to-Digital Conversion Complete Interrupt Flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<5>: CMPIF - Comparator Result Change Interrupt Flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<4>: P6 ICIF - P6 Port Change Interrupt Enable Bit

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<3>: P5 ICIF - P5 Port Change Interrupt Flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<2>: TC2IF - TC2 Period Match Interrupt Flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<1>: TC1IF - TC1 Period Match Interrupt Flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<0>: TC0IF - TC0 Overflow Interrupt Flag

0: No Interrupt Triggered

1: Interrupt Triggered

5. Reset

5.1. Overview of Reset Functionality

The JZ8P2616 system provides four types of reset methods:

- Power-On Reset (POR)
- RESET pin low-level input reset
- WDT watchdog overflow reset
- LVR low voltage reset

When any of the above resets occurs, all system registers are initialized to their reset values, the program stops running, and the program counter (PC) is set to zero. After the reset is completed, the system begins operation again from vector 0000H.

Each reset situation requires a certain response time, and the system reset mechanism ensures the reliable reset of the MCU. The time required to complete the reset varies for different types of oscillators. Consequently, both the rise time of VDD and the start-up time of different oscillators are not fixed. The start-up time for RC oscillators is the shortest, while that for crystal oscillators is relatively long. During the use of the user terminal, it is important to consider the application's requirements for power-on reset timing.

5.2. Power-On Reset (POR)

Power-on reset is closely related to LVR operation. The process of powering up the system presents a gradually rising curve, requiring a certain amount of time to reach normal level values.

- Power On: The system detects that the power voltage has risen and is waiting for it to stabilize;
- System Initialization: All system registers are set to their initial values;
- Oscillator Starts: The oscillator begins to provide the system clock;
- Execute Program: Power-up ends, and the program starts running;

Power-on reset time is determined by the "Reset Time" option in the OPTION, as shown in the table below:

PWRT and WDT	Reset Establishment Time
PWRT=WDT/2	3.5ms (following the watchdog reset time)
PWRT=WDT/2	14ms (following the watchdog reset time)
PWRT=WDT/2	57ms (following the watchdog reset time)
PWRT=WDT/2	228ms (following watchdog reset time)
PWRT ≠ WDT	350us (independent fixed reset time)

5.3. WDT watchdog reset

The watchdog reset is a protective setting for the system. Under normal conditions, the program will reset the watchdog timer. If an error occurs and the system enters an unknown state, the watchdog timer will overflow, and the system will reset. After the watchdog reset, the system restarts and returns to normal operating conditions.

- Watchdog timer status: The system checks if the watchdog timer has overflowed; if it has overflowed, the system will reset;
- System initialization: All system registers are set to their initialization default values;
- Oscillator Starts: The oscillator begins to provide the system clock;
- Execute Program: Power-up ends, and the program starts running;

Explanation of watchdog wakeup:

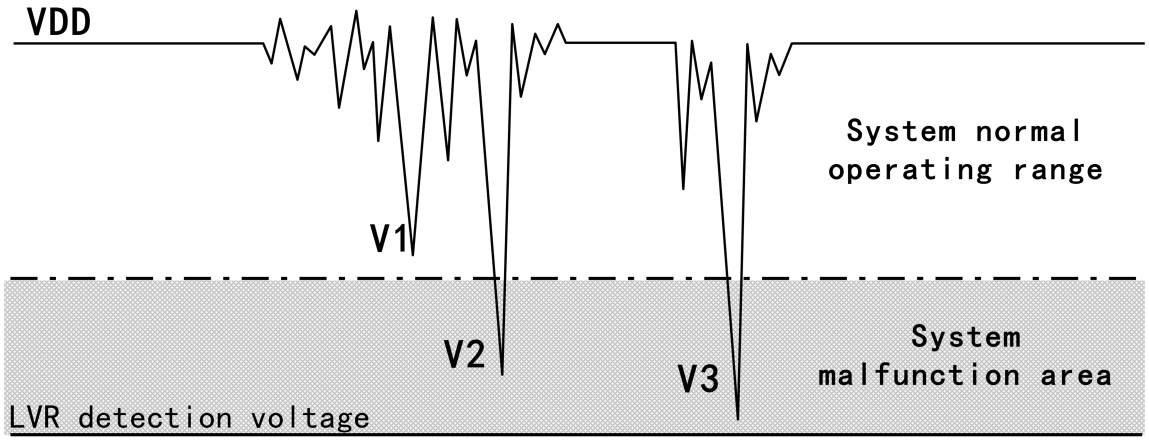
The watchdog reset can occur in both idle mode and sleep mode. After the system resets, the program starts executing from address 0X00. The user can check the overflow bit of R183 (STATUS) register Bit4; if it indicates WDT overflow, it can be determined that a watchdog reset has occurred, triggering the corresponding wakeup subroutine. Note that the watchdog wakeup is essentially a special application of the watchdog reset.

Notes on watchdog timer application:

- Checking the status of the I/O ports and RAM before resetting the watchdog can enhance the reliability of the program;
- You cannot reset the watchdog during an interruption, otherwise it will be unable to detect a runaway condition in the main program;
- The watchdog should only be cleared once in the main program. This architecture maximizes the protective function of the watchdog.

5.4. LVR low voltage reset

Power-on reset applies to situations where system voltage drops due to external factors (such as interference or changes in external load). Power loss can lead to abnormal system operation or execution errors in the program.



A voltage drop may cause the system to enter a dead zone. The system dead zone means that the power supply cannot meet the minimum operating voltage requirements of the system. The above diagram is a typical power-on reset schematic. In the diagram, VDD is seriously affected by interference, leading to a very low voltage value. The area above the dashed line indicates normal operation, while the area below the dashed line indicates an unknown working state, known as the dead zone. When VDD drops to V1, the system remains in a normal state; when VDD drops to V2 and V3, the system enters the dead zone, leading to potential errors. The following situations may cause the system to enter the dead zone:

In DC applications:

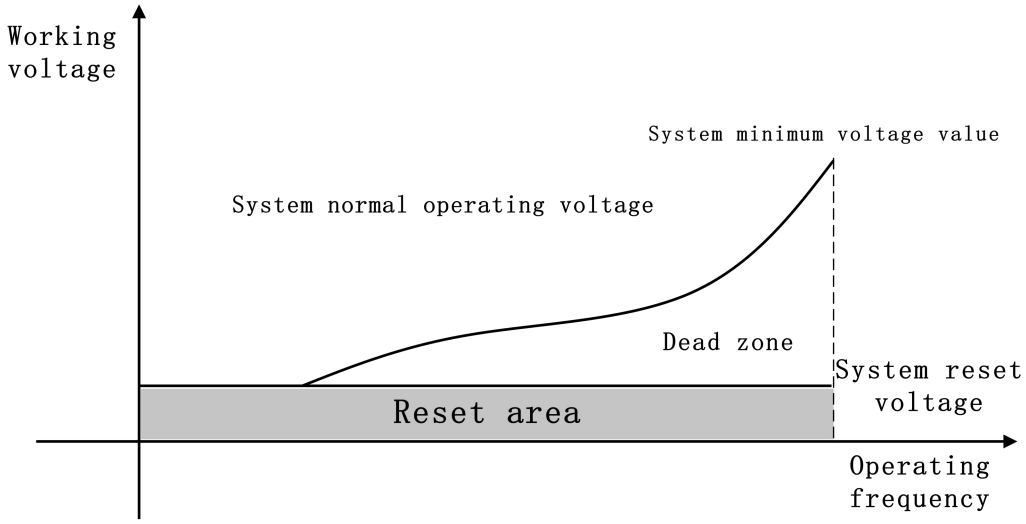
DC applications generally use battery power. When the battery voltage is too low or the microcontroller drives a load, the system voltage may drop and enter the dead zone. In this case, the power supply will not further decline to the LVR detection voltage, thus maintaining the system in the dead zone.

In AC applications:

When the system is powered by AC, the DC voltage value is affected by noise in the AC power supply. When the external load is too high, such as when driving a motor, the interference generated by the load also impacts the DC power supply. If VDD drops below the minimum operating voltage due to interference, the system may enter an unstable operating state. In AC applications, the power-up and power-down times are generally longer. The power-up sequence protects normal power-up, but the power-down process is similar to that in DC applications; after the AC power is turned off, the VDD voltage descends slowly and may enter the dead zone.

5.5. Relationship between operating frequency and LVR low voltage detection

To improve the performance of the system's power-on reset, it is essential to first clarify the minimum operating voltage value of the system. The system's minimum operating voltage is related to its execution speed, and different execution speeds will result in different minimum operating voltage values.



As shown in the figure above, the normal operating voltage range of the system is generally higher than the system reset voltage, which is determined by the low voltage detection (LVR) level. When the system's execution speed increases, the minimum operating voltage of the system also increases correspondingly. However, since the system reset voltage is fixed, there will be a voltage zone between the

system's minimum operating voltage and the system reset voltage where the system cannot operate normally and will not reset. This zone is referred to as the dead zone.

To avoid dead zone voltage, it is essential to select the appropriate LVR reset voltage point when choosing the operating frequency. As shown in the table below:

IRC frequency	Clocks division	LVR reset voltage point
IRC-16MHz	2 Clocks	LVR=3.3V
IRC-8MHz	2 Clocks	LVR=2.2V
IRC-4MHz	2 Clocks	LVR=1.8V
IRC-1MHz	2 Clocks	LVR=1.8V

Note: 1. Operating frequency = Instruction cycle frequency = IRC frequency / Clocks division;

2. The corresponding values of the operating frequency and LVR reset voltage point are merely recommended values. Users can appropriately adjust the reset voltage point based on specific application scenarios during use.

5.6. Related registers

5.6.1. R1AF/WDTCON (WDT Control Register)

0X1AF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	WDTPSR<1:0>		LVREN	RTCS	-	-	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R
Reset Value	1	0	0	0	0	0	0	0

Bit<7>: WDTE - WDT watchdog enable control

0: Disable

1: Enable

Bit<6:5>: WDTPSR<1:0> - WDT prescaler selection bits:

WDTPSR<1>	WDTPSR<0>	WDT prescaler factor
0	0	1:4
0	1	1:8
1	0	1:16
1	1	1:32

Bit<4>: LVREN-LVR Enable Control

0: Enable

1: Disable

Bit<2:0>: Unused

6. System Clock and Operating Mode

6.1. System Clock

The JZ8P2616 integrates three types of oscillators: high-speed RC oscillator IHRC, low-speed RC oscillator ILRC, and an external crystal oscillator. The system clock can switch between high-speed and low-speed oscillators via the R188/CPUCON register.

6.1.1. Internal IHRC Oscillator

The JZ8P2616 features an integrated IHRC high-speed oscillator, offering configurable IHRC frequency functionality. The default frequency is 8 MHz, and the IHRC frequency can be fine-tuned using the IHRCCAL register.

The IHRC oscillator includes five frequency values: 1M/4M/8M/16M/32MHz. By setting the configuration bits of OPTION, the IHRC operating frequency can be selected. Below are their corresponding relationships:

RCM	IRC frequency
1M	IHRC frequency selected as 1 MHz
4M	The IHRC frequency is selected as 4MHz
8M	The IHRC frequency is selected as 8MHz
16M	The IHRC frequency is selected as 16MHz
32M	The IHRC frequency is selected as 32MHz

The JZ8P2616 provides multiple frequency division options for the instruction clock, which can be selected in the OPTION, suitable for more occasions. See the table below:

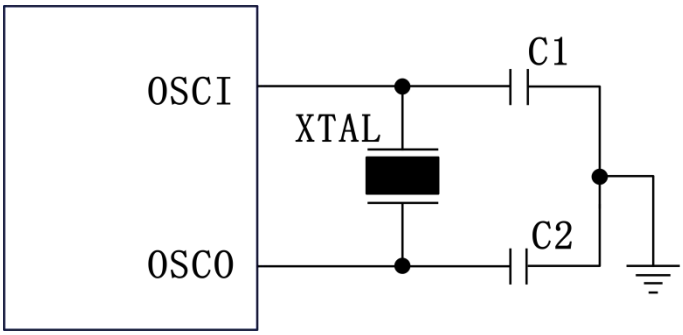
Clocks	Clocks division
2clock	Divided frequency is 2clock
4clock	Divided frequency is 4clock
8clock	Divided frequency is 8clock
16clock	Divided frequency is 16clock
32clock	Divided frequency is 32clock

6.1.2. Internal ILRC oscillator

JZ8P2616 has a built-in ILRC low-speed oscillator that provides a stable 36KHz low-speed clock.

6.1.3. External crystal oscillator

JZ8P2616 has a built-in LXT crystal oscillator startup circuit. In most applications, the OSCO and OSCI pins can be connected to a crystal or ceramic resonator to generate oscillation. The circuit diagram is as follows, and the recommended values for C1 and C2 are in the table. Due to the different characteristics of each resonator, users should refer to its specifications to select appropriate values for C1 and C2.



Crystal oscillator application circuit

Capacitance selection reference for crystal or ceramic oscillators:

Oscillator mode	Frequency mode	Frequency	C1(pF)	C2(pF)
Low-speed crystal oscillator	LXT	32.768KHz	5-30	5-30

Note: The above data is for reference only; actual testing shall prevail.

6.1.4. Clock Module Application Instructions

- The internal oscillator is the most commonly used oscillation mode, which eliminates the need for external circuitry.
- When using an external clock input, the clock signal must be input from OSCI, and OSCO can be left floating.
- Due to different external conditions, the clock frequency in various oscillation modes may have slight variations, so a reasonable selection should be made according to needs.

6.2. Operating Modes

The JZ8P2616 can operate in four different operating modes with varying clock frequencies. These modes control the operation of the oscillator, execution of the program, and functional loss of the analog circuit.

- High-Speed Mode: The system clock selects the internal high-speed clock, and the low-speed clock operates normally;
- Low-Speed Mode: The system clock selects the internal low-speed clock, and the high-speed clock pauses operation;
- Idle Mode: The system clock operates normally, while other parts of the system enter sleep mode (TC0 can select the system clock to continue working and can wake up the system), and can also be awakened via P5IWE, P6IWE, INTWE, ADCWE, CMPWE;
- Sleep Mode: All functions pause, and the system enters sleep mode, which can be awakened by TC0 (external input clock/RTC mode), TC1 (RTC mode), P5IWE, P6IWE, INTWE, CMPWE;

Function Modules	High-Speed Mode	Low-Speed Mode	Idle Mode	Sleep Mode
IHRC	Run	Stop	Run	Stop
ILRC	Run	Run	Run	Stop
CPU	Execute	Execute	Stop	Stop
TC0	Operational	Operational	Operational	Operational (P62 input clock/RTC)
TC1	Operational	Operational	Operational	Operational (RTC)
TC2	Operational	Operational	Operational	Stop
Interrupt	All valid	All valid	All valid (TC0 select system clock)	TC0IE, TC1IE, P5ICIE, P6ICIE, INTIE, CMPIE
wake-up function	-	-	TC0WE (TC0 select system clock can wake up), TC1WE, TC2WE P5IWE, P6IWE, INTWE, ADCWE, CMPWE	TC0WE, TC1WE, P5IWE, P6IWE, INTWE, CMPWE
Watchdog	WDT option	WDT option	WDT option control	WDT option

6.2.1. High-Speed Mode

High-speed mode is the system's high-speed clock operating mode, with the system clock source provided by a high-speed RC oscillator. The program is executed. After a power-on reset or any reset trigger, the system enters high-speed mode to execute the program. In high-speed mode, the high-speed oscillator operates normally, with maximum power consumption.

- The program is executed, and all functions can be controlled;
- The system rate is high-speed;
- Both the high-speed oscillator and the internal low-speed oscillator operate normally;
- High-speed mode can switch to low-speed mode;
- Entering sleep mode from high-speed mode will return to high-speed mode upon awakening;
- Entering idle mode from high-speed mode will return to high-speed mode upon awakening;

6.2.2. Low-Speed Mode

Low-speed mode is the system's low-speed clock operating mode. The system clock source is provided by a low-speed ILRC oscillator. Low-speed mode is controlled by the CLKMD bit in the CPU mode control register. When CLKMD=0, the system operates in high-speed mode; when CLKMD=1, the system enters low-speed mode. After entering low-speed mode, the system cannot automatically disable the high-speed RC oscillator; it must be disabled via SPTHX=1 to reduce power consumption.

- The program is executed, and all functions can be controlled;
- The system rate is low-speed;
- The internal low-speed oscillator is functioning normally, while the high-speed oscillator has stopped working.
- Low-speed mode can switch to high-speed mode;
- Transitioning from low-speed mode to sleep mode, it returns to low-speed mode upon waking up;
- Transitioning from low-speed mode to idle mode, it returns to low-speed mode upon waking up;

6.2.3. Idle Mode

Idle mode is another ideal state. In sleep mode, all functions and hardware devices are disabled, but in idle mode, the system clock remains operational. The power consumption in idle mode is greater than that in sleep mode. In idle mode, no programs are executed, but the wakeup-capable TC0, TC1, TC2, P5IWE, P6IWE, INTWE, ADCWE, CMPWE continue to operate normally. The clock source for timers TC0, TC1, TC2 is the system clock that is still functioning. Whether to enter idle mode is determined by the system clock and the IDLE bit in the status control register; when IDLE=1, it executes SLEEP and then enters idle mode.

- The program stops executing, and all functions are disabled;
- The modules with wakeup functionality are operational;
- The system clock is functioning normally;
- Transitioning from high-speed mode to idle mode, it returns to high-speed mode upon waking up;
- Transitioning from low-speed mode to idle mode, it returns to low-speed mode upon waking up;
- The wake-up methods in idle mode are P5IWE, P6IWE, INTWE, ADCWE, CMPWE;
- TC0, TC1, and TC2 functions remain active in idle mode;

6.2.4. Sleep Mode

Sleep mode is the ideal state of the system, where no programs are executed and the oscillator stops working. The entire chip's power consumption is below 1uA. Sleep mode can be awakened by TC0 (P62 input clock/RTC), TC1 (RTC), P5IWE, P6IWE, INTWE, and CMPWE. When entering sleep mode from high-speed mode or low-speed mode, it will return to the corresponding mode upon being awakened. The entry into sleep mode is controlled by the system clock and the IDLE bit of the status control register. When IDLE=0, executing SLEEP will enter sleep mode.

- The program stops executing, and all functions are disabled;
- All oscillators, including external high-speed oscillators, internal high-speed oscillators, and internal low-speed oscillators, stop working;
- Power consumption is below 1uA;
- Entering sleep mode from high-speed mode, it returns to high-speed mode when awakened;

- Entering sleep mode from low-speed mode, it returns to low-speed mode when awakened;
- The wake-up methods in sleep mode are TC0 (P62 input clock/RTC), TC1 (RTC), P5IWE, P6IWE, INTWE, and CMPWE;

6.2.5. Related registers

6.2.5.1. R188/CPUCON (CPU Mode Control Register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	ADCWE	CMPWE	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: ADCWE - ADC wake-up enable bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<6>: CMPWE - CMP Wakeup Enable Bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<5>: TC2WE - TC2 Wake-up Enable Bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<4>: TC1WE - TC1 Wake-up Enable Bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<3>: TC0WE - TC0 Wake-up Enable Bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<2>: STPHX - High-Speed Clock Control Bit

0: High-speed clock operates normally

1: Stop high-speed clock

Bit<1>: CLKMD - System Clock Control Bit

0: System clock uses High-Speed Oscillator (IHRC) clock

1: System clock uses Low-Speed Oscillator (ILRC) clock

When the system enters low-speed mode from high-speed mode, first set CLKMD=1, then set STPHX=1;

When the system transitions from low-speed mode to high-speed mode, first set STPHX=0, then set CLKMD=0.

Bit<0>: IDLE - idle mode enable bit

0: The system enters sleep mode when executing the SLEEP instruction

1: The system enters idle mode when executing the SLEEP instruction, and the system clock continues to operate normally

TC0 and PWM can continue to operate in idle mode if the system clock is selected, and can wake up the system.

6.2.5.2. R189/IHRCCAL (IHRC frequency fine-tuning register)

0X189	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IHRCCAL	-	IHRCCAL<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	X	X	X	X	X	X	X

IHRC high-speed oscillator frequency fine-tuning

6.2.5.3. R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	-	INTWE	INTIF	INTIE	INTEDG	INTEN	INTGATE	CMPGATE
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<6>: INTWE - INT wake-up enable bit

0: Disable

1: Enable

7. Timer Counter

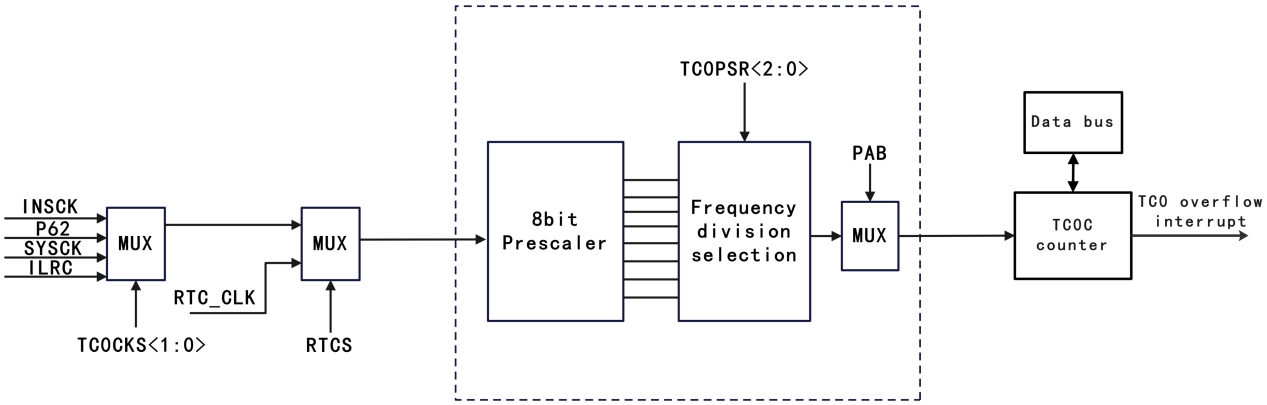
7.1. TC0 Timer Counter

The JZ8P2616 provides an 8-bit timer counter as the TC0 prescaler. The TC0PTEN bit in the TC0CON register determines whether to prescale, and the TC0PSR<2:0> three bits determine the prescale ratio.

TC0 is an 8-bit up counter that operates as long as there is a clock. The clock source can be the instruction clock, system clock, or low-speed clock. It can also select an external clock (input via the P62 pin, with optional triggering edge) or an external crystal oscillator clock. The arrival of the clock increments the counter by 1.

TC0 counter overflow can generate an interrupt signal.

In IDLE mode, the TC0 overflow interrupt can wake up the circuit, and after waking up, it can choose to enter the interrupt or continue executing the original program. In sleep mode, when TC0 is set to the P62 external input clock/RTC clock, it can interrupt on overflow and wake up the circuit.



TC0 Block Diagram

7.1.1. TC0 Timer Setting Instructions

1. Initialize the TC0C register;
2. Set the value of the TC0CON register (choose clock source and prescale ratio);
3. To use as a counter, the TC0 signal source should be selected as the external input signal in the TC0CON register;

4. After all configurations are set up, finally set TC0EN in the TC0CON register to enable the timer counter;
5. If interrupt functionality is required, set TC0IE (Bit0) in the INTE register to 1 and execute the EI instruction;
6. The system will automatically save ACC, STATUS, and RSR data during the interrupt service routine. After executing the RETI instruction, the data will be automatically restored, and the TC0 interrupt flag must be cleared before exiting the interrupt;

7.1.2. TC0 Timer Calculation Description

The TC0 timing function assigns an initial value to the timer by writing to the TC0C register, and the timer starts counting from the initial value until it overflows and generates an interrupt.

TC0 Timing Time Calculation Formula (Choosing Internal System Clock):

$$\text{TC0 Timing duration} = (1/\text{Fosc}) \times (\text{TC0 prescaler}) \times (256 - \text{TC0 initial value})$$

Example:

Fosc = 8 MHz, TC0 Prescaler Selection = 8, TC0 Initial Value = 156;

$$\text{TC0 Timing duration} = (1/8) \times (8) \times (256 - 156) = 100\ \text{us}$$

TC0 Timing Time Calculation Formula (Choosing External Input Clock):

$$\text{TC0 Timing duration} = (1/\text{External input clock}) \times (\text{TC0 prescaler}) \times (256 - \text{TC0 initial value})$$

Example:

External Input Clock = 1 MHz, TC0 Prescaler Selection = 4, TC0 Initial Value = 156;

$$\text{TC0 Timing duration} = (1/1) \times (4) \times (256 - 156) = 400\ \text{us}$$

7.1.3. TC0 Idle Mode Wake-up Instructions

In idle mode, the system instructions stop executing, modules with wake-up functionality and the system clock work normally, while other functions are disabled.

TC0 can wake up from idle mode by setting the Bit 3 of the R188/CPUCON register TC0WE to 1. With IDLE = 1 plus the SLEEP instruction, the system enters idle mode, and the TC0 timer works normally (selecting the system clock). When the TC0 timer

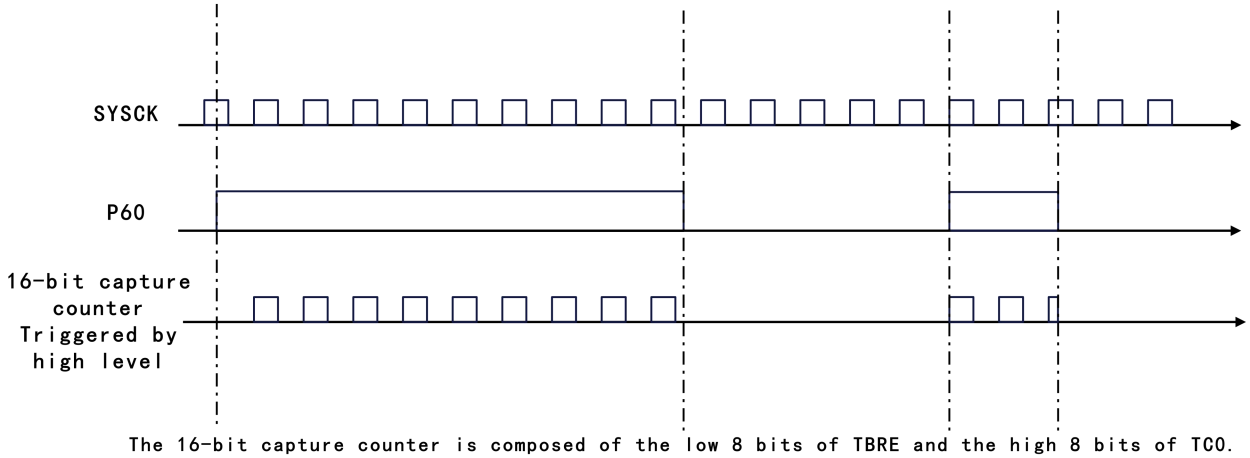
overflows, the system is awakened. If TC0IE and EI are enabled, it will enter an interrupt after waking up; if DI is executed, it will execute the next instruction upon waking up.

When the clock source is chosen as P62 external clock/RTC clock, enabling TC0WE=1 and directly executing the SLEEP sleep instruction can also wake up the system.

7.1.4. TC0 Capture Mode

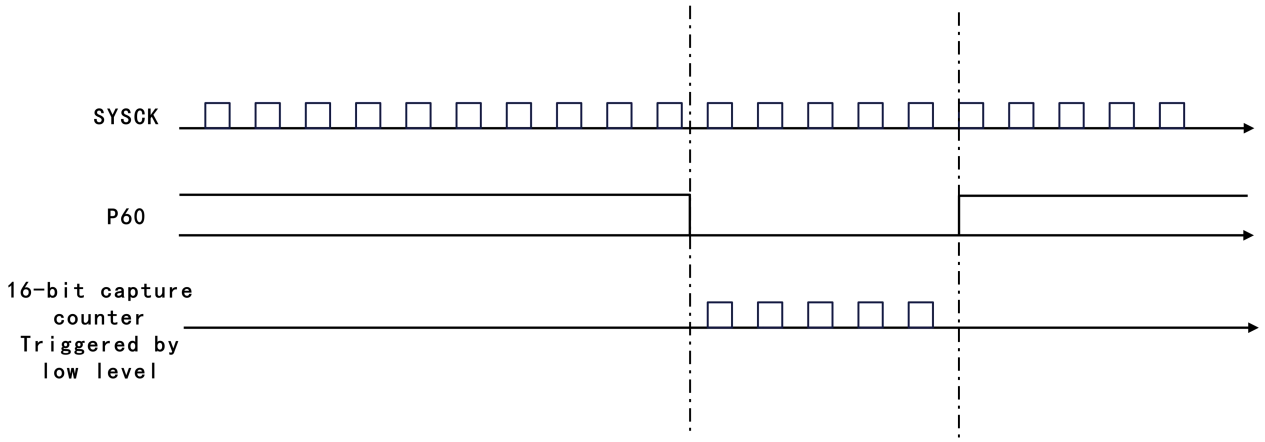
The JZ8P2616 provides level capture functionality on the P60 port. By multiplexing the TC0 8-bit prescaler TPRE (as the low 8 bits of the level capture counter) and the 8-bit counter TC0C (as the high 8 bits of the level capture counter), a 16-bit level capture counter is formed. Concurrently, with an external interrupt, a level change can trigger an interrupt, allowing the time of the previous level capture to be determined in the interrupt routine. The external interrupt can be selected by the triggering edge of the 0X1AE/EXINTCON register INTEDG.

Explanation of the high level capture functionality on the P60 port. First, set the 0X1AE/EXINTCON register INTGATE =1 to select external interrupt level control for the TC0 counter, while selecting INTEDG =0 for the external interrupt falling edge trigger feature. Enable the external interrupt, select the TC0 clock source as the system clock in the TC0CON register, and finally enable TC0EN=1. When the P60 port is high, the TC0 prescaler and counter start counting with the clock being the system clock. When the P60 port is low, the TC0 prescaler and counter stop counting, and the port's falling edge triggers an external interrupt. The counting values from the R185/TC0C and R1AD/TPRE registers can be read in the interrupt routine to calculate the level duration.



The 16-bit capture counter is composed of the low 8 bits of TBRE and the high 8 bits of TC0.

The low level capture on the P60 port is similar to that of the high level. First, set the 0X1AE/EXINTCON register INTGATE =1 to select external interrupt level control for the TC0 counter, and enable INTEDG=1 for the external interrupt rising edge trigger feature. Enable the external interrupt, select the TC0 clock source as the system clock in the TC0CON register, and finally enable TC0EN=1. When the P60 port is low, the TC0 prescaler and counter start counting with the clock being the system clock. When the P60 port is high, the TC0 prescaler and counter stop counting, and the port's rising edge triggers an external interrupt. The counting values from the R185/TC0C and R1AD/TPRE registers can be read in the interrupt routine to calculate the level duration.



The 16-bit capture counter is composed of the low 8 bits of TBRE and the high 8 bits of TC0.

7.1.5. TC0 Related Registers

7.1.5.1. R184/TC0CON (TC0 Control Register)

0X184	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CON	TC0EN	TC0CKS<1:0>		TC0EDG	TC0PTEN	TC0PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC0EN - TC0 timer count enable bit

0: Disable TC0

1: Enable TC0

Bit < 6:5 >: TC0CKS<1:0> - TC0 signal source selection bit

00: Instruction clock

01: External input signal (P62)

10: System Clock

11: ILRC Clock (Low-Speed Oscillator)

Bit<4>: TCOEDG - TCO Signal Edge Selection Bit

0: TCO Pin Signal Changes from High to Low to Add 1

1: TCO Pin Signal Changes from Low to High to Add 1

Bit<3>: TCOPTEN - Prescaler Enable Bit

0: Disable TCO Prescaler

1: Enable TCO Prescaler

Bit<2:0>: TCOPSR<2:0> - TCO Prescaler Selection Control Bit:

TCOPSR<2>	TCOPSR<1>	TCOPSR<0>	TCO Division Factor
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

7.1.5.2. R185/TCOC (TCO 8-bit Counter Register)

0X185	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCOC	TCOC<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.1.5.3. R1AD/TPRE(TCO Pre-divider)

0X1AD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TPRE	TPRE<7:0>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

7.1.5.4. R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	-	INTWE	INTIF	INTIE	INTEDG	INTEN	INTGATE	CMPGATE
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: Unused

Bit<5>: INTIF - External Interrupt Flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<4>: INTIE - External Interrupt Enable

0: Disable

1: Enable

Bit<3>: INTEDG - External Interrupt Trigger Edge Selection

0: Falling edge (P60 is high TC0 count when external interrupt capture)

1: Rising edge (P60 is low TC0 count when external interrupt capture)

Bit<2>: INTEN - P60 External Interrupt Enable Bit

0: Disable

1: Enable

Bit<1>: INTGATE - TC0 external interrupt capture gate enable bit

0: Disable

1: Enable

7.1.5.5. R1AF/WDTCON (RTC clock control register)

0X1AF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	WDTPSR<1:0>		LVREN	RTCS	-	-	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R
Reset Value	1	0	0	0	0	0	0	0

Bit<3>: RTCS - TC0 clock source selects RTC clock

0: TC0 clock is selected by TC0CKS<1:0>

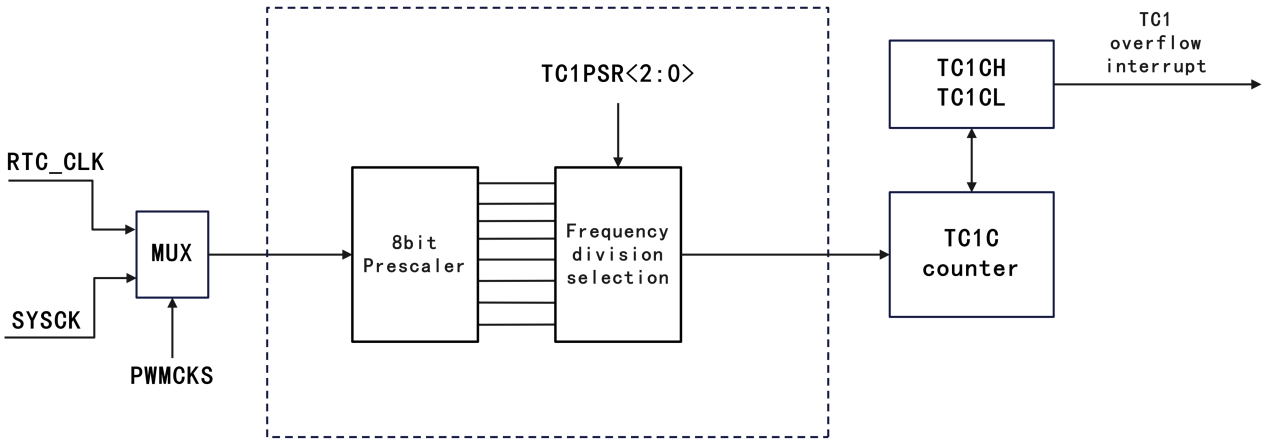
1: Select RTC clock

7.2. TC1 timer counter

TC1 timer counter provides an 8-bit prescaler, and the three bits TC1PSR<2:0> in the TC1CON register determine the prescale ratio. In TC1 mode, each time TC1EN is enabled, the prescaler register is cleared.

TC1 is a 10-bit up counter. The TC1 timer must be enabled with TC1EN to operate. The clock source can be the system clock or an external crystal oscillator clock, and with each clock cycle, the counter increments by 1. When the TC1 count value matches the TC1PRD setting, an overflow occurs. If TC1IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service routine.

In IDLE mode, the TC1 interrupt can wake up the circuit. After waking, it can choose to enter the interrupt or continue executing the original program, as referenced by input changes on the port to wake up.



TC1 Structure Block Diagram

7.2.1. TC1 Timer Setting Instructions

1. Assign an initial value to the TC1PRD<9:0> register;
2. Set the TC1CON register and configure the prescale ratio as needed;
3. Enable the TC1IE interrupt in the R1D6/INTE register and execute the EI instruction;
4. Enable TC1EN to start the TC1 timer counting;
5. The system will automatically save ACC, STATUS, and RSR data during the execution of the interrupt service routine. After executing the RETI

instruction, the data will automatically restore, and the TC1 interrupt flag must be cleared before exiting the interrupt;

7.2.2. TC1 Timing Calculation Description

The TC1 timing function starts counting from the initial value 0x01 by writing a value to TC1PRD<9:0>. The timer continues to count until the timer count matches the value of TC1PRD<9:0>, at which point it triggers an overflow interrupt service routine.

TC1 timing calculation formula:

$$\text{TC1 Timing duration} = (1/\text{Fosc}) \times (\text{TC1 Prescaler}) \times (\text{TC1PRD})$$

Example:

Fosc = 16 MHz, TC1 prescaler selection = 16 prescaler, TC1PRD value = 512;

$$\text{TC1 Timing duration} = (1/16) \times (16) \times (512) = 512\text{us}$$

7.2.3. TC1 idle mode wake-up description

TC1 can wake up from idle mode by enabling the TC1WE bit (Bit4) in the R188/CPUCON register. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC1 timer functions normally. When the TC1 timer overflows, the system is awakened. If TC1IE and EI are enabled, it will enter an interrupt upon waking; if DI is executed, it will execute the next instruction after waking.

7.2.4. TC1 related registers

7.2.4.1. R1B0/TC1CON (TC1 control register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GATE	TC1CKS	TC1PTEN	TC1PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC1EN-TC1/PWM123 counter enable control

0: Disable

1: Enable

Bit<6>: TC21EN-TC1/PWM123, TC2/PWM4567 counter simultaneous enable control bit

0: Disable

1: Enable

Bit<4>：TC1CKS-TC1 clock selection

0：System clock

1：RTC clock

Bit<3:0>：TC1PTEN，TC1PSR2～TC1PSR0 prescaler selection bits：

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	TC1 division factor
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

7.2.4.2. R1B1/TC1PRDL (TC1 timer counter low 8 bits register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.2.4.3. R1B5/TC1PRDTH (TC1 timer counter high 2 bits register)

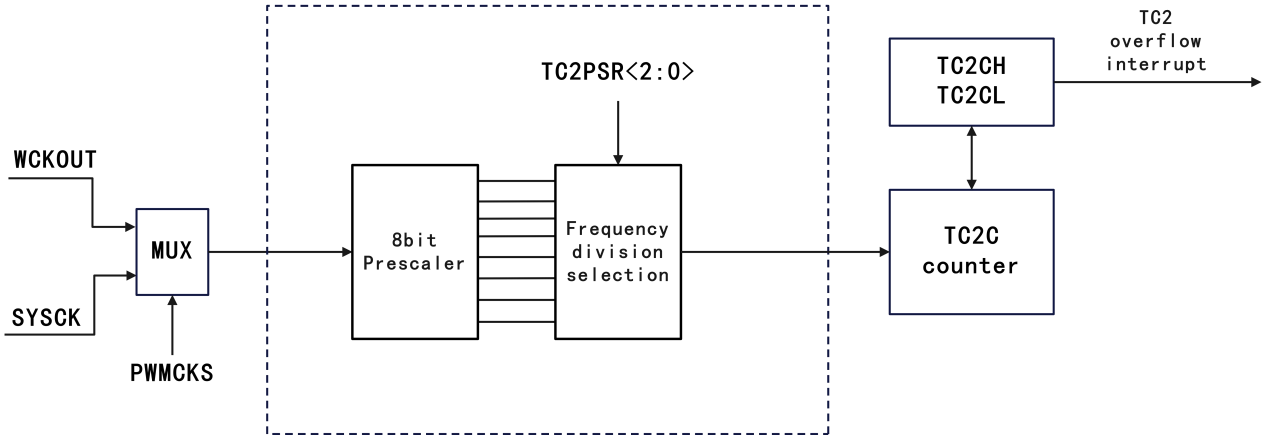
0X1B5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<9:8>		PWM3DT<9:8>		PWM2DT<9:8>		PWM1DT<9:8>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.3. TC2 Timer Counter

The TC2 timer counter provides an 8-bit prescaler, and the three bits TC2PSR<2:0> in the TC2CON register determine the prescale ratio. In TC2 mode, every time TC2EN is enabled, the prescaler register is cleared.

TC2 is a 10-bit up counter. The TC2 timer must have TC2EN enabled to operate, with the clock source being either the system clock or a low-speed clock. With each clock cycle, the counter increments by 1. The TC2 count value will generate an overflow when it matches the TC2PRD set value. If TC2IE and EI are enabled, the system will jump to the corresponding interrupt vector address and execute the interrupt service routine.

In IDLE mode, the TC2 interrupt can wake up the circuit, allowing it to either enter interrupt mode or continue executing the original program, depending on input port changes for wake-up.



TC2 Block Diagram

7.3.1. TC2 Timer Configuration Instructions

1. Assign an initial value to the TC2PRD<9:0> register;
2. Set the TC2CON register and configure the prescaler as needed;
3. Enable the R1D6/INTE register, turn on the TC2IE interrupt enable, and execute the EI instruction;
4. Enable TC2EN and start the TC2 timer counting;
5. The system will automatically save ACC, STATUS, and RSR data when executing the interrupt service routine. After executing the RETI instruction, the data

will be automatically restored. Before exiting the interrupt, the TC2 interrupt flag must be cleared;

7.3.2. TC2 Timer Calculation Explanation

The TC2 timing function works by writing a value to TC2PRD<11:0>. The timer starts counting from the initial value 0x01 and will continue until the timer count matches the TC2PRD<11:0> value, at which point an overflow will trigger the execution of the interrupt service routine.

TC2 Timing Calculation Formula:

$$\text{TC2 Timing duration} = (1/\text{Fosc}) \times (\text{TC2 Prescaler}) \times (\text{TC2PRD})$$

Example:

Fosc = 16 MHz, TC2 prescaler selection = 16 prescale, TC2PRD value = 512;

$$\text{TC2 Timing duration} = (1/16) \times (16) \times (512) = 512\text{us}$$

7.3.3. TC2 Idle Mode Wakeup Explanation

TC2 can wake up from idle mode by enabling bit 5 TC2WE in the R188/CPUCON register. When IDLE = 1 plus the SLEEP instruction, the system enters idle mode, and the TC2 timer operates normally. After the TC2 timer overflows, the system is awakened. If TC2IE and EI are enabled, the system will enter an interrupt after waking up; if DI is executed, it will proceed to execute the next instruction after waking up.

7.3.4. TC2 Related Registers

7.3.4.1. R1B8/TC2CON (TC2 Control Register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC2EN - TC2/PWM4567 Counter Enable Control

0: Disable

1: Enable

Bit<4>: TC2CKS - TC2 Clock Selection

0: System clock

1: Low Speed Clock

Bit<3:0>: TC2PTEN, TC2PSR2 ~ TC2PSR0 prescaler selection bits:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 Division Factor
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

7.3.4.2. R1B9/TC2PRDL (TC2 Timer Counter Low 8-bit Register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.3.4.3. R1BD/TC2PRDTH (TC2 Timer Counter High 2-bit Register)

0X1BD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD<9:8>		PWM6DT<9:8>		PWM5DT<9:8>		PWM4DT<9:8>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

8. PWM Pulse Width Modulation

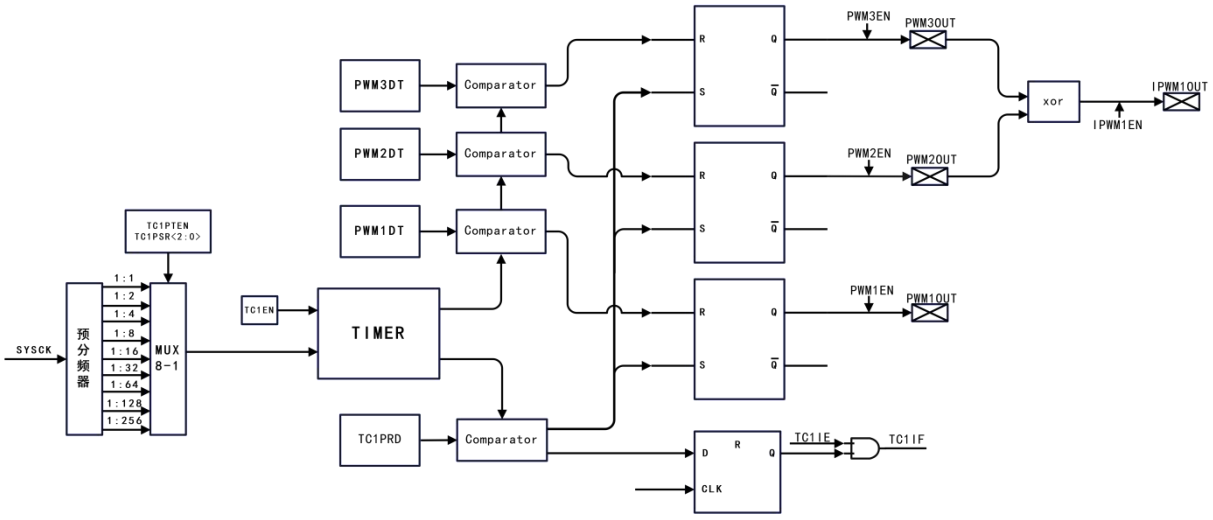
The JZ8P2616 provides two sets of 10-bit TC1 and TC2 counters. The two sets of counters can be divided into a total of seven PWM channels. PWM1-3 share TC1 counters, while PWM4-7 share TC2 counters to generate pulse width modulation signals. The PWM output waveform is determined by the period and duty cycle, with a transmission rate equal to the reciprocal of the period. PWMINV controls the inversion of the outputs PWM6, PWM5, and PWM4. The chip provides complementary outputs with dead time, generating IPWM1 by XORing PWM2 and PWM3, and using PWM1 as the dead-time complementary signal. (IPWM4 is the same as IPWM1)

PWM has a period overflow interrupt, which can jump to interrupt after enabled.

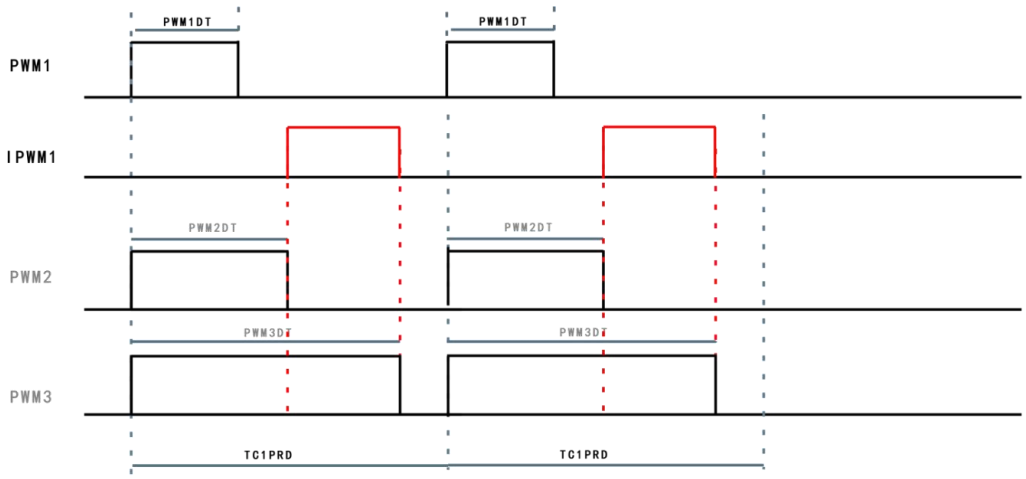
In IDLE mode, TC1 and TC2 can wake up the system by selecting TC1CKS=0 and TC2CKS=0 in the TC1 and TC2 control registers, and enabling TC1WE and TC2WE in the CPU mode control register.

8.1. PWM Internal Structure and Timing

The following internal structure diagram is for reference only and does not represent the actual circuit.



PWM Working Structure Circuit



3-path Common Period PWM and IPWM Timing Description

8.2. PWM Cycle and Duty Cycle

PWM provides a 10-bit clock counter with an 8-bit programmable pre-divider, serving as the baud rate clock generator for the PWM module. The counter function can be enabled by setting the TCxEN bit in the PWM control register. The pre-divider setting for the counter can be controlled using the TCxPSR<2:0> control bits. PWMxEN and IPWMxEN enable the PWM function and PWM complementary function, respectively.

The PWM period is set by writing values to the TCxPRDL (low 8 bits) and TCxPRDTH (high 2 bits) period registers. When the counter value equals the PRD value, the following events occur in the next increment cycle:

- Counter reset;
- Corresponding PWM output pin set to high;
- Generate PWM period overflow interrupt (if enabled);
- PWM duty cycle latched from PWMxDTL/TCxPRDTH register to DT/TIMER compare register;

PWM period calculation formula:

$$\text{PWM period} = (\text{TCxPRD}) \times (1/\text{Fosc}) \times (\text{PWM prescaler})$$

Example:

TCXPRD=100, Fosc=16MHz, PWM pre-divider selection=2 divider;

$$\text{PWM period} = (100) \times (1/16) \times (2) = 12.5\ \text{us}$$

PWM duty cycle is written to the PWM duty cycle register. When the counter value overflows and resets to zero, the value of PWMxDT is latched into the DT/TIMER compare register. When the value of the DT/TIMER compare register equals the TIMER counter value, the PWM output pin is set to low. The value of PWMxDT can be written at any time, but the value of the DT/TIMER compare register is written only during period overflow:

PWM duty cycle calculation formula:

$$\text{PWM duty} = (\text{PWMxDT}) \times (1/\text{Fosc}) \times (\text{PWM prescaler})$$

Example:

PWMxDT=50, Fosc=16MHz, PWM prescaler selection=2 prescaler;

$$\text{PWM duty} = (50) \times (1/16) \times (2) = 6.25\ \text{us}$$

8.3. PWM Idle Mode Wake-up Description

In idle mode, CPU instruction execution stops, while modules with wake-up functionality and the system clock continue to operate normally, and other functions are disabled.

PWM can wake up from idle mode by setting TC1WE/TC2WE wake-up enable, selecting the clock source as the system clock (SYSCK). Set the corresponding period or duty cycle interrupt enable, set IDLE (R188) to 1, and use the SLEEP instruction to enter idle mode, allowing the PWM timer to operate normally.

When the corresponding interrupt condition is met, the system wakes up. If EI is enabled, it will enter an interrupt after waking up; if DI is enabled, it will execute the next instruction after waking up.

8.4. PWM Comparator Gating Description

The gating function of PWM1 is controlled by the PWM1GATE in the TC1CON register. When PWM1GATE=1, the PWM1 output is controlled by the comparator result, and when CMP_FLAG=0, it outputs the PWM waveform.

The gating function of PWM4 or PWM4, PWM5/PWM6 complementary dead zone is controlled by PWM4GATE<0> in the TC2CON register. When PWM4GATE<0>=1, the output of PWM4 or the complementary dead zone between PWM4 and PWM5/PWM6 is controlled by the comparator result, and when CMP_FLAG=0, it outputs the PWM waveform.

8.5. IPWM Waveform and Buzzer Setting Description

The IPWM waveform is not simply inverted; instead, by enabling IPWM1EN, the outputs of PWM2 and PWM3 are XORed before outputting. If IPWM1EN is enabled at this time, it can select the output control bit from P61/P52 through PWM2; it can also select the output control bit from P51/P63 through PWM3. Additionally, it supports simultaneous outputs of the IPWM1 waveform from two ports.

Similarly, enabling IPWM4EN outputs the result of XORing PWM5 and PWM6. It allows the selection control bit to choose output from P62/P67 through PWM5; it can also choose output from P55/P66 through PWM6. At the same time, it supports outputting the IPWM4 waveform from both ports simultaneously.

The PWM module also features a buzzer function. Users can enable PWM output to the buzzer via the BZXEN (R1B7, R1BF) control bit. The buzzer can be selected through PWM1S (R1B7) and PWM4S (R1BF) for output from ports P60/P66 and P50/P64, respectively. It is important to note that to enable the buzzer, PWM1EN and PWM4EN must be set to zero, and the corresponding output ports must be configured as outputs.

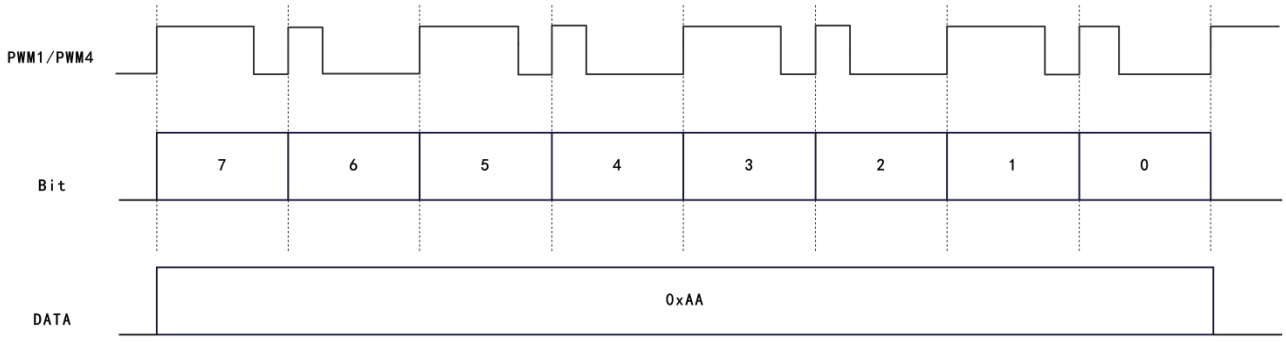
8.6. PWM7DT interrupt and ADC triggering explanation

PWM7DT provides the functionality of an interrupt triggered by the duty cycle. After enabling PWM7DTIE (R1D6) and executing the EI instruction, the interrupt program can be entered according to the configured PWM7 duty cycle.

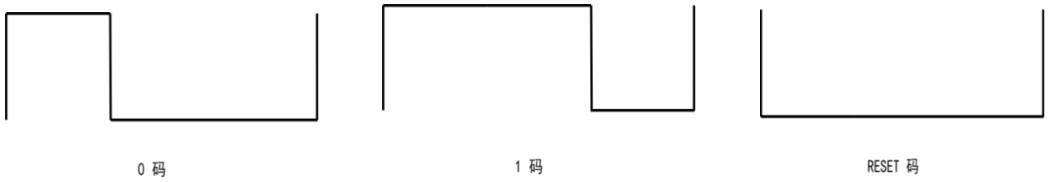
The ADC can be configured to trigger conversion enabled by the PWM7 duty cycle. By setting ADCGATE (R1A7) to 1, the ADC conversion will be triggered on the falling edge of the PWM7 duty cycle.

8.7. Single-wire cascade of LEDs

JZ8P2616 supports two channels of single-wire cascade LED driving, outputting cascade control timing through the PWM1 and PWM4 ports. The timing diagram for the cascade LED driving is shown below:



Single-wire cascade LED timing explanation



PWM1 and PWM4 are two independent channels of single-wire cascade LED driving control. When using PWM1 as the LED driving control, the high-level time for the 0 code type is set by the PWM1 duty cycle register, and the high-level time for the 1 code type is set by the PWM2 duty cycle register. The cycle of the code data is set by the TC1PRD cycle register. After enabling PWM1_LEDEN (R186) + TC1EN, the transmission of 8-bit cascade data begins, which is output from the PWM1 port. Once the transmission of 8-bit cascade data is completed, TC1EN automatically resets to zero, and resetting TC1EN will initiate the transmission of the next 8-bit cascade data.

When using PWM4 as the LED driving control, the high-level time for the 0 code type is set by the PWM4 duty cycle register, and the high-level time for the 1 code type is set by the PWM5 duty cycle register. The cycle of the code data is set by the TC2PRD cycle register. After enabling PWM4_LEDEN (R186) + TC2EN, the transmission of 8-bit cascade data begins, which is output from the PWM4 port. Once the transmission

of 8-bit cascade data is completed, TC2EN automatically resets to zero, and resetting TC2EN will initiate the transmission of the next 8-bit cascade data.

8.8. PWM-related registers

8.8.1. R186/TBRDH (LED Cascade Control Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	PWM4_LEDEN	PWM1_LEDEN	-	VDD_POWER	-	RBIT<10:8>		
Read/Write	R/W	R/W	R	R/W	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM4_LEDEN - PWM4 LED Cascade Control Bit

0: Disable

1: Enable

Bit<6>: PWM1_LEDEN - PWM1 LED Cascade Control Bit

0: Disable

1: Enable

Note: Bit 4 must be 1

8.8.2. R1B0/TC1CON (TC1 control register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GATE	TC1CKS	TC1PTEN	TC1PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC1EN - TC1/PWM123 Counter Enable Control

0: Disable

1: Enable

Bit<6>: TC21EN-TC1/PWM123, TC2/PWM4567 counter simultaneous enable control bit

0: Disable

1: Enable

Bit<5>: PWM1GATE - PWM1 or Dead Zone Complementary Gate Output Enable Control Bit

0: No restriction

1: The PWM1 output is controlled by the comparator result. When CMPOUT = 0, the PWM waveform is output. When CMPOUT = 1, the PWM1 output is held at a low level.

Bit<4>: TC1CKS-TC1 clock selection

0: System clock

1: RTC clock

Bit<3:0>: TC1PTEN, TC1PSR2～TC1PSR0 prescaler selection bits:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	TC1 division factor
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

8.8.3. R1B1/TC1PRDL (TC1/PWM123 Period Low 8-bit Register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM2, PWM3) cycle low 8 bits

8.8.4. R1B2/PWM1DTL(PWM1 duty cycle low 8-bit register)

0X1B2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DTL	PWM1DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM1 duty cycle low 8-bit

8.8.5. R1B3/PWM2DTL(PWM2 duty cycle low 8-bit register)

0X1B3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2DTL	PWM2DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM2 duty cycle low 8-bit

8.8.6. R1B4/PWM3DTL(PWM3 duty cycle low 8-bit register)

0X1B4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM3DTL	PWM3DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM3 duty cycle low 8 bits

8.8.7. R1B5/TC1PRDTH (TC1/PWM123 period high 2 bits and duty cycle high 2 bits register)

0X1B5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<9:8>		PWM3DT<9:8>		PWM2DT<9:8>		PWM1DT<9:8>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM2, PWM3) period high 2 bits and PWM1, PWM2, PWM3 duty cycle high 2 bits

8.8.8. R1B7/PWMCON1 (PWM control register 1)

0X1B7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON1	BZ1EN	PWM3S	PWM2S	PWM1S	IPWM1EN	PWM3EN	PWM2EN	PWM1EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ1EN - BZ1 waveform output enable control bit

0: Disable

1: Enable (BZ1EN=1 must be set, PWM1EN=0, and P60/P66 must be configured as output to output BZ1 waveform)

Bit<6>: PWM3S - PWM3 output selection control bit

0: PWM3 outputs from P63

1: PWM3 outputs from P51

Bit<5>: PWM2S - PWM2 output selection control bit

0: PWM2 outputs from P61

1: PWM2 output from P52

Bit<4>: PWM1S - PWM output selection control bit

0: PWM1 output from P60

1: PWM1 output from P53

Bit<3>: IPWM1EN - IPWM1 enable control bit

0: Disable

1: Output PWM2 XOR PWM3

（Select output port based on PWM2EN (P52/P61) or PWM3EN (P51/P63)）

Bit<2>: PWM3EN - PWM3 enable control bit

0: Disable

1: Enable output of PWM3 waveform

(The corresponding port must be set to output to output the PWM3 waveform)

Bit<1>: PWM2EN - PWM2 enable control bit

0: Disable

1: Enable output of PWM2 waveform

(The corresponding port must be set as output to output the PWM2 waveform)

Bit<0>: PWM1EN - PWM1 enable control bit

0: Disable

1: Enable output of PWM1 waveform

(The corresponding port must be set as output to output the PWM1 waveform, and BZ1EN=0)

8.8.9. R1B8/TC2CON (TC2 Control Register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC2EN - TC2/PWM4567 Counter Enable Control

0: Disable

1: Enable

Bit<6>: PWM4GATE<1> - PWM4 gate output enable control bit 1

0: No restriction

1: PWM4 output is controlled by external interrupt EXINT; when EXINT=1, output PWM, otherwise output low level

Bit<5>: PWM4GATE<0> - PWM4 gate output enable control bit 0

0: No restriction

1: PWM4 output is controlled by comparator result; when CMPOUT=0, output PWM, otherwise output low level

Bit<4>: TC2CKS - TC2 Clock Selection

0: System clock

1: Low Speed Clock

Bit<3:0>: TC2PTEN, TC2PSR2 ~ TC2PSR0 prescaler selection bits:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 Division Factor
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

8.8.10. R1B9/TC2PRDL(TC2/PWM4567 Low 8-bit Register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 (PWM4, PWM5, PWM6, PWM7) Low 8-bit Period

8.8.11. R1BA/PWM4DTL(PWM4 Duty Cycle Low 8-bit Register)

0X1BA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM4DTL	PWM4DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM4 Low 8-bit Duty Cycle

8.8.12. R1BB/PWM5DTL(PWM5 Duty Cycle Low 8-bit Register)

0X1BB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM5DTL	PWM5DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM5 Low 8-bit Duty Cycle

8.8.13. R1BC/PWM6DTL (PWM6 duty cycle low 8-bit register)

0X1BC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM6DTL	PWM6DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM6 duty cycle low 8 bits

8.8.14. R1BD/TC2PRDTH (TC2/PWM456 period high 2 bits and duty cycle high 2 bits register)

0X1BD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD<9:8>		PWM6DT<9:8>		PWM5DT<9:8>		PWM4DT<9:8>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 (PWM4, PWM5, PWM6) period high 2 bits and PWM4, PWM5, PWM6 duty cycle high 2 bits

8.8.15. R1BF/PWMCON2 (PWM control register 2)

0X1BF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON2	BZ2EN	PWM6S	PWM5S	PWM4S	IPWM4EN	PWM6EN	PWM5EN	PWM4EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ2EN - BZ2 waveform output enable control bit

0: Disable

1: Output BZ2 waveform (BZ2EN=1 and PWM4EN=0 must be set, P50/P64 must be set to output to provide BZ2 waveform)

Bit<6>: PWM6S - PWM6 output selection control bit

0: PWM6 outputs from P55

1: PWM6 outputs from P66

Bit<5>: PWM5S-PWM5 output selection control bit

0: PWM5 outputs from P62

1: PWM5 outputs from P67

Bit<4>: PWM4S-PWM4 output selection control bit

0: PWM4 outputs from P64

1: PWM4 outputs from P50

Bit<3>: IPWM4EN-IPWM4 enable control bit

0: Disable

1: Output PWM5 XOR PWM6

(Select output port according to PWM5EN (P62/P67) or PWM6EN (P55/P66))

Bit<2>: PWM6EN-PWM6 enable control bit

0: Disable

1: Output PWM6 waveform enable

(The corresponding port must be set to output in order to output the PWM6 waveform)

Bit<1>: PWM5EN - PWM5 enable control bit

0: Disable

1: Enable output of PWM5 waveform

(The corresponding port must be set to output in order to output the PWM5 waveform)

Bit<0>: PWM4EN - PWM4 enable control bit

0: Disable

1: Enable output of PWM4 waveform

(The corresponding port must be set to output in order to output the PWM4 waveform, and BZ2EN=0)

8.8.16. R1C2/PWM7DTL (PWM7 duty cycle low 8-bit register)

0X1C2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM7DTL	PWM7DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

8.8.17. R1C3/PWM7CON (PWM7 Control Register)

0X1C3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM7CON	PWMINV<6:4>			PWM_PULSEEN	PWM7S	PWM7EN	PWM7DT<9:8>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:5>: PWMINV<6:4> — PWM6/PWM5/PWM4 Output Inversion Control Bit

0: No Inversion

1: Inversion

Bit<4>: PWM_PULSEEN—PWM7 duty cycle single trigger enable bit

0: Disable

1: Enable

Bit<3>: PWM7S-PWM7 output selection control bit

0: PWM7 output from P65

1: PWM7 output from P54

Bit<2>: PWM7EN-PWM7 enable control bit

0: Disable

1: Enable PWM7 waveform output

(The corresponding port needs to be set as output to output PWM7 waveform)

Bit<1:0>: PWM7DT<9:8>-PWM7 duty cycle high 2 bits

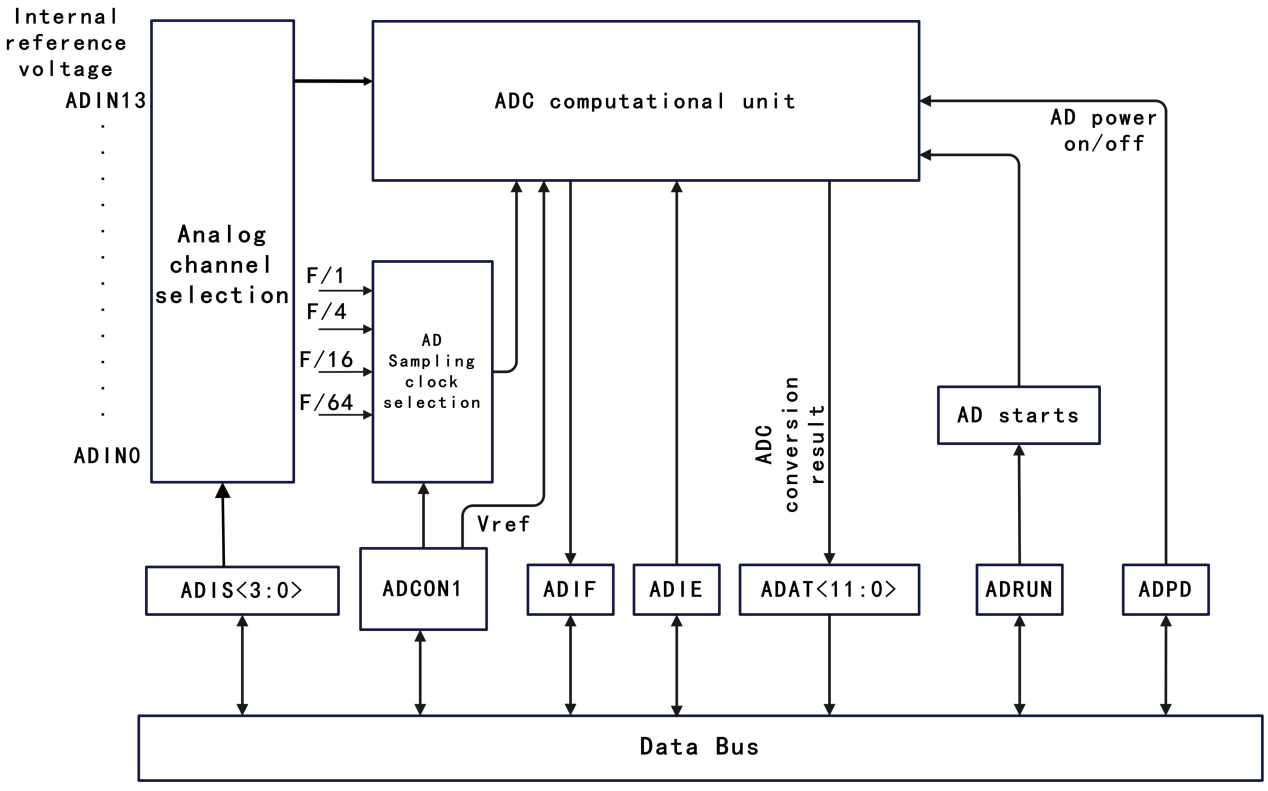
9. ADC Analog-to-Digital Conversion

JZ8P2616 ADC module provides a 12-bit precision SAR AD converter, including 18 analog channels.

The ADC converter uses successive approximation analog-to-digital conversion, storing the results in the R1A3/ADATH0, R1A4/ADATL, and R1A5/ADATH1 result registers. Channel selection, internal/external reference voltage sources, sampling clock, ADC start, and ADC power consumption are controlled by the ADCON0 and ADCON1 control registers.

AD conversion completion can trigger an interrupt or can be determined by querying the ADRUN bit in R1A7/ADCON1.

If the AD wake-up function is enabled, the completion of AD conversion can wake the device from sleep mode or idle mode.



AD Conversion Function Diagram

AD Conversion Time:

The time to convert 1 bit in AD is defined as TAD. A complete 12-bit ADC conversion requires 16 TAD cycles. The TAD timing specification must be strictly followed to

ensure normal sampling and accurate results. The required time settings also vary with different reference voltages and different VDD, so refer to the following table to set a reasonable divider.

Reference Voltage/V	Operating Voltage/V	Fastest Divider Setting Fosc=16MHz	Conversion Time/us
VDD	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64
4	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64
3	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64
2	4.0～5.5	Fosc/16	64
	2.7～4.0	Fosc/64	64

Calculation of AD sampling voltage value:

$$\text{ADC sampling voltage} = \frac{\text{Sampled value}}{4096} * \text{Reference voltage}$$

Example: Reference voltage is internal reference 3V, sampling value is 0x800=2048

$$\text{ADC sampling voltage} = \frac{2048}{4096} * 3 = 1.5\text{V}$$

9.1. ADC power supply voltage detection description

By configuring the ADCON0(R1A6) register, the channel selection bit ADIS<4:0>=01110 selects 1/4VDD as the sampling channel, and VREF<2:0> selects the reference voltage, obtaining the conversion result through ADC conversion. It can be derived as follows for the voltage value of VDD:

$$\text{Conversion result} = \left(\frac{\text{VDD}}{4}/\text{VREF}\right) \times 4096$$

then

$$\text{VDD} = (\text{Conversion result}/4096) * 4 * \text{VREF}$$

9.2. ADC analog-to-digital conversion setup description

1. ADC input port enablement and analog channel selection, set R1A0/P5ADE, R1A1/P6ADE, R1A6/ADCON1 registers;
2. Set the ADC reference voltage source, clock pre-scaler, and reference voltage selection by configuring registers R1A6/ADCON0 and R1A7/ADCON1;

3. If interrupt functionality is required, set ADIE=1 and execute the "EI" instruction;
4. Set "ADEN=1" to start the ADC power supply voltage;
5. Select IDLE/SLEEP mode as needed, and configure the ADC wake-up function, ADCWE=1;
6. Set "ADRUN=1" to start AD conversion;
7. Wait for an interrupt or for ADRUN to be cleared to 0. If an AD interrupt occurs, clear ADIF to 0 when exiting the interrupt program;
8. Save the conversion result. If multiple AD conversions are needed, jump back to step 7;

9.3. P65 Port External 1/4 Voltage Detection Instructions

The JZ8P2616 has a built-in channel for collecting an external voltage using a 1/4 voltage divider resistor. A high voltage can be input from the P65 port, and the value after the voltage divider should be less than the ADC reference voltage, allowing normal sampling. The high voltage value can be deduced through calculation:

$$\text{P65 Voltage} = \frac{\text{Sampled value}}{4096} * \text{Reference voltage} * 4$$

Example: VDD=5V, with a reference voltage of the internal reference as 4V, the sample value is 0x800=2048

$$\text{P65 Voltage} = \frac{2048}{4096} * 4 * 4 = 8\text{V}$$

9.4. ADC Related Registers

9.4.1. R1A3/ADATH0 (ADC Data High 8-bit Register)

0X1A3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATH0	ADAT< 11:4 >							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: ADAT<11:4> - AD Conversion Result High 8 Bits

9.4.2. R1A4/ADATL (ADC Data Low 8-bit Register)

0X1A4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATL	ADAT<7:0>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: ADAT<7:0> - AD Conversion Result Low 8 Bits

9.4.3. R1A5/ADATH1 (ADC high 4-bit data register)

0X1A5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATH1	-	-	-	-	ADAT<11:8>			
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit<7:4>: unused

Bit<3:0>: ADAT<11:8> - high 4 bits of AD conversion result

9.4.4. R1A6/ADCON0 (ADC Control Register 0)

0X1A6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON0	ADIS<4:0>					VCMPS	EXTVS	VREFOUT
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:3>: ADIS<4:0> - AD input channel selection

ADIS<4>	ADIS<3>	ADIS<2>	ADIS<1>	ADIS<0>	Channel selection
0	0	0	0	0	AIN0/P50
0	0	0	0	1	AIN1/P51
0	0	0	1	0	AIN2/P52
0	0	0	1	1	AIN3/P53
0	0	1	0	0	AIN4/P54
0	0	1	0	1	AIN5/P55
0	0	1	1	0	AIN6/P60
0	0	1	1	1	AIN7/P61
0	1	0	0	0	AIN8/P62
0	1	0	0	1	AIN9/P63
0	1	0	1	0	AIN10/P64
0	1	0	1	1	AIN11/P65
0	1	1	0	0	AIN12/P66

0	1	1	0	1	AIN13/P67
0	1	1	1	0	0.25*（VDD or P65）
0	1	1	1	1	GND
1	1	1	1	1	TEST（User Disabled）

Bit<2>：VCMPS-ADC Comparison Voltage Source Selection

0：Select VREF

1：Select VDD (Recommended to select VDD for reference)

Bit<1>：EXTVS - Sampling Channel via 1/4 Resistor Voltage Divider Source Selection

0：Select VDD as 1/4 Resistor Voltage Divider Source

1：Select P65 as 1/4 Resistor Voltage Divider Source

Bit<0>：VREFOUT - ADC's VREF Output Enable Control Bit

0: Disable

1: Enable (configure P65 as an analog input, can output VREF voltage)

9.4.5. R1A7/ADCON1 (ADC Control Register 1)

0X1A7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON1	ADRUN	ADEN	ADPSR<1:0>		ADCGATE	VREF<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	1

Bit<7>: ADRUN

0: No sampling or sampling finished

1: ADC starts sampling

Bit<6>: ADEN

0: ADC disabled (turns off ADC in sleep mode; otherwise, power consumption occurs)

1: ADC enabled

Bit<5:4>: ADPSR<1:0> - ADC clock prescaler selection (Fosc is the system clock frequency)

ADPSR<1>	ADPSR<0>	ADC clock
0	0	Fosc/16
0	1	Fosc/4
1	0	Fosc/64
1	1	Fosc/1

Bit<3>: ADCGATE - ADC gate control select bit

0: Gate control disabled, enabled by software ADCEN

1: Gate control enabled, ADC sampling enabled by the falling edge of PWM7 duty

cycle

Bit<2:0>: VREF<2:0> - Reference voltage selection

VREF<2>	VREF<1>	VREF<0>	Reference voltage
0	0	0	VBG1.2V
0	0	1	Reference 2V
0	1	0	Reference 3V
0	1	1	Reference 4V
1	0	0	EXVREF
1	0	1	VDD

10. CMP Comparator

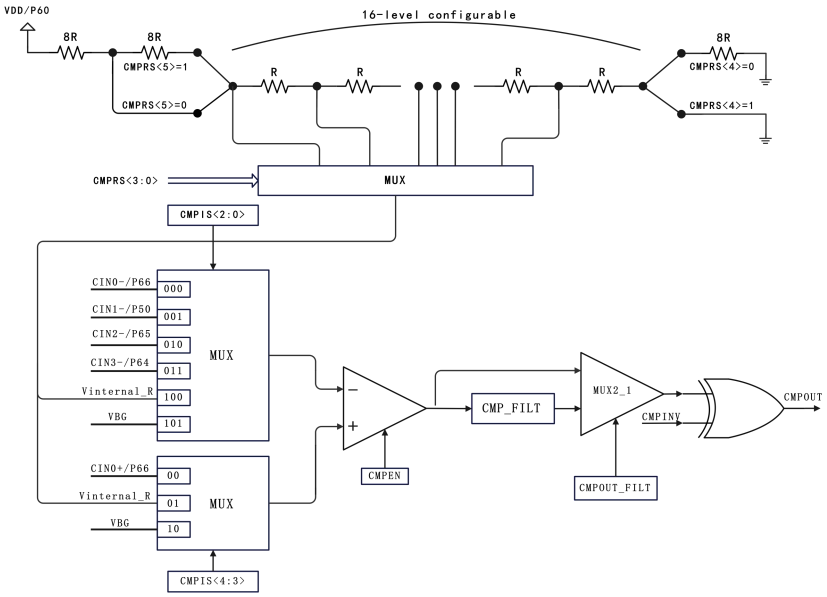
The JZ8P2616 includes a hardware comparator that can compare any two of the following three options: input pins, internal reference voltage V_internal R, and the built-in Bandgap (1.2V). One of these is selected as the positive input, and another as the negative input. The negative input of the comparator can be P66, P50, P65, P64, a voltage divider resistor (selected by CMPRS<5:0>), or VBG. The positive input of the comparator can be P66, a voltage divider resistor (selected by CMPRS<5:0>), or VBG. (The same port cannot serve as both positive and negative inputs simultaneously, and the voltage divider input source cannot serve as both positive and negative at the same time.)

The voltage divider resistor can be configured through the CMPCON control register to select the input voltage source as either P60 or VDD.

The output result of the comparator can be directed to the P67 output through the CMPOE bit of the CMPCON1 (1C9) register, with support for inverting the output. The chip supports digital filtering of the output results, which can be selected in OPTION.

The comparator supports triggering interrupts on output result changes. Enabling CMPIE can generate interrupt signals.

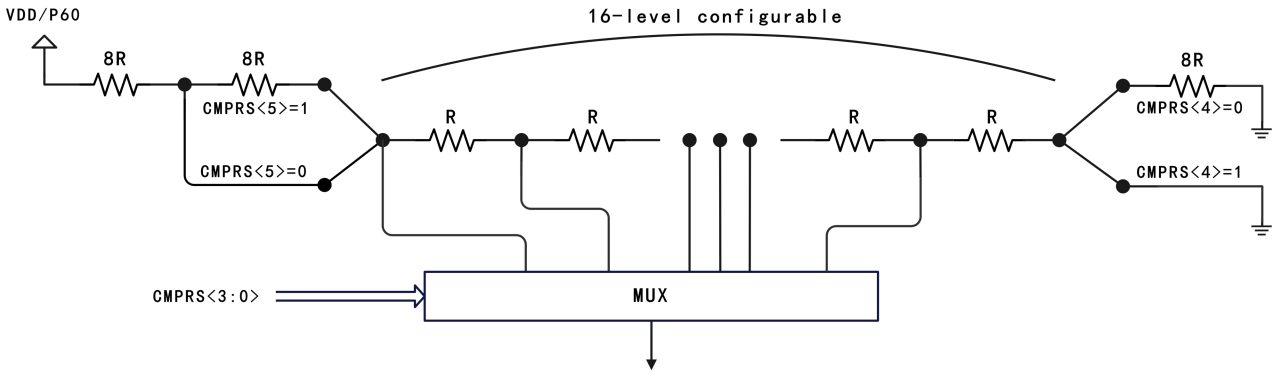
The comparator supports waking up from output result changes. Enabling CMPWE can wake up from idle mode and sleep mode. In idle and sleep modes, enabling CMPEN will activate the low-speed oscillator, which increases sleep power consumption.



Comparator Schematic Description

10.1. Voltage of Voltage Divider Resistor V_internal R

The output voltage V_internal R is composed of a series of resistors, which can generate reference voltages at different levels. CMPRS<5:0> jointly determine the magnitude of V_internal R, where CMPRS<5> and CMPRS<4> select the maximum and minimum values of V_internal R. CMPRS<3:0> is used to select the desired voltage level, which is divided into 16 equal parts based on the average of the maximum and minimum values of V_internal R, selected by CMPRS<3:0>.



Comparator Calibration Schematic

Example 1: CMPRS<5>=0, CMPRS<4>=0

Value Range: $V_{internal\ R} = (3/4) * VDD \sim (1/4) * VDD + (1/32) * VDD$

Calculation Formula: $V_{internal\ R} = (1/4) * VDD + \frac{(n+1)}{32} * VDD$

Example 2: CMPRS<5>=0, CMPRS<4>=1

Value Range: $V_{internal\ R} = (2/3) * VDD \sim (1/24) * VDD$

Calculation Formula: $V_{internal\ R} = \frac{(n+1)}{24} * VDD$

Example 3: CMPRS<5>=1, CMPRS<4>=0

Value Range: $V_{internal\ R} = (3/5) * VDD \sim (1/5) * VDD + (1/40) * VDD$

Calculation Formula: $V_{internal\ R} = (1/5) * VDD + \frac{(n+1)}{40} * VDD$

Example 4: CMPRS<5>=1, CMPRS<4>=1

Value Range: $V_{internal\ R} = (1/2) * VDD \sim (1/32) * VDD$

Calculation Formula: $V_{internal\ R} = \frac{(n+1)}{32} * VDD$

n=CMPRS<3:0>

10.2. Comparator Configuration

When using the comparator, enable CMPEN (this will activate ILRC for filtering the output result CMPOUT, increasing power consumption). Set CMPIS<5:0> to choose the positive and negative input sources, and designate the positive and negative terminals as inputs. The same terminal cannot serve as both positive and negative input simultaneously, and the voltage divider resistor input source cannot serve as both positive and negative at the same time.

If the resistor divider is selected as the input source, set the register CMPRS<5:0> as needed to select the desired divider resistor output voltage V_internal R for comparison.

Example 1:

Select P66 as the negative input and set the voltage of V_internal R as (18/32)*VDD for the positive input. Choose the configuration where CMPRS<5>=0 and CMPRS<4>=0, with CMPRS<3:0>=4b' 1001 (n=9) to obtain

V_internal R = (1/4)*VDD + [(9+1)/32]*VDD = (18/32)*VDD

Once the configuration is complete, enable Bit7 CMPEN of the CMPCON0 (R1EA) control register to start the comparator comparison. The comparison result can be output through P67 by configuring Bit7 CMPOE of the CMPCON1 (R1C9) control register (P67 should be set as output). The output result can also be inverted by configuring Bit7 CMPINV of the CMPCON1 register.

10.3. RFC resistor frequency conversion

The JZ8P2616 has a built-in RFC resistor frequency conversion function. By using the comparison result from the comparator to control TC0 capturing, it enables time counting for external voltage changes.

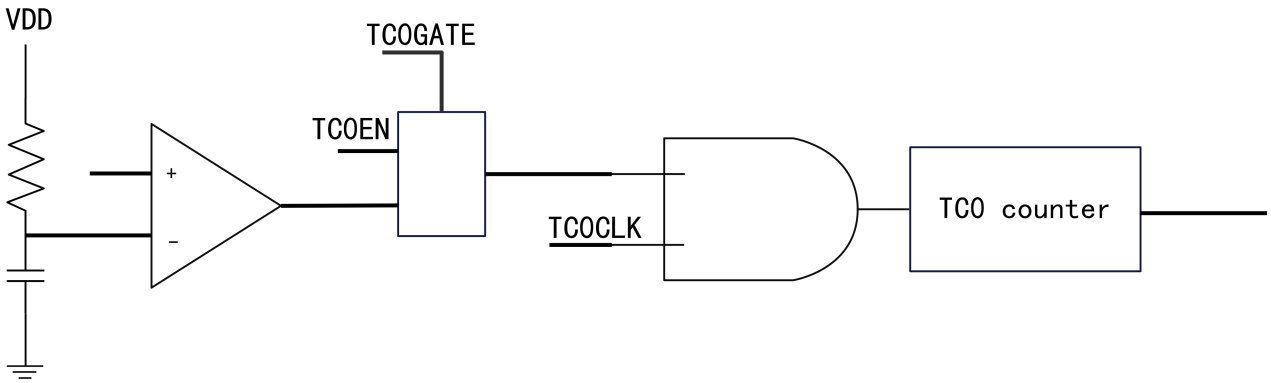
RFC principle:

The change in RFC port voltage affects the output result of the comparator. When enabling the CMPGATE bit of the R1C3 register, TC0 counting is controlled by the output

result CMPOUT of the comparator. When the RFC port voltage is lower than the comparator's positive voltage, counting starts at TC0 when CMPOUT=1; when the RFC port voltage is higher than the comparator's positive voltage, counting stops at TC0 when CMPOUT=0. The counted value of TC0 records the time taken for the RFC port voltage to charge to the preset voltage value (comparator's positive voltage).

Application Steps:

1. Set the PxAE register to select the analog port of the comparator;
2. Set the CMPCON0 and CMPCON1 registers to configure the positive input source of the comparator to a fixed voltage and set the negative input source of the comparator to an external port (as illustrated).
3. Set the port output of the comparator's negative input source to low level to discharge the port capacitor.
4. Clear the initial value of the TC0 timer.
5. Set the port of the comparator's negative input source to an analog input port and start sampling the voltage at the RFC port.
6. Read the TC0 count value and calculate the charging time of the RFC port.



RFC Structure Diagram

10.4. CMP Related Registers

10.4.1. R1AE/EXINTCON (Comparator Gating Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	-	INTWE	INTIF	INTIE	INTEDG	INTEN	INTGATE	CMPGATE
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<0>: CMPGATE - TC0 Comparator Output Flag Capture Gating Enable Bit

0: Disable

1: Enable

10.4.2. R1C8/CMPCON0 (CMP Control Register 0)

0X1C8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON0	CMPEN	CMPOUT	CMPRS<5:0>					
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPEN - CMP enable control bit

0: Disable

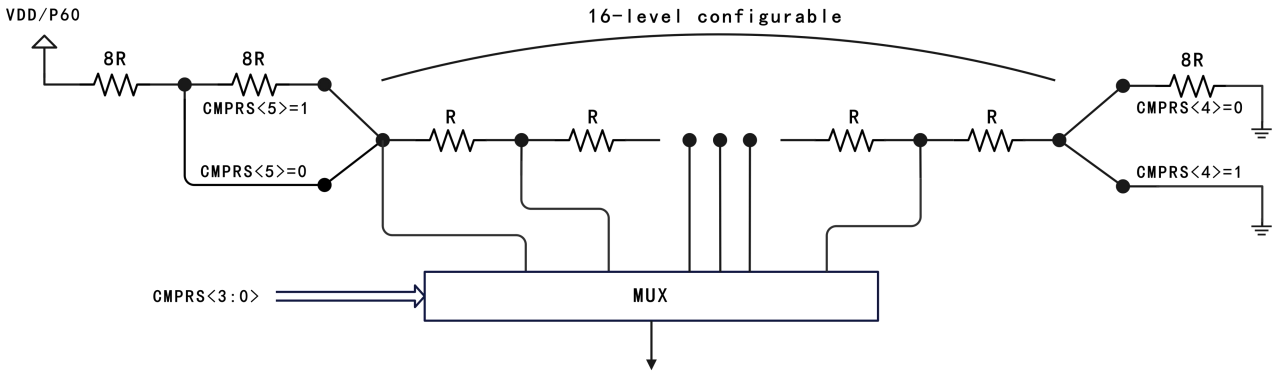
1: Enable

Bit<6>: CMPOUT - CMP result output bit

0: The positive voltage of the comparator is less than the negative voltage

1: The positive voltage of the comparator is greater than the negative voltage

Bit<5:0>: CMPRS<5:0> - Comparator trim bits



When CMPCON1 register = 0x0D, the positive terminal selects resistor divider, and the negative terminal selects VBG (1.2V). Different resistor divider ranges CMPRS<5:0> correspond to different detection voltages, as shown in the table below (the gray part of the detection voltage is prohibited for use):

CMPRS	Detection Voltage	CMPRS	Detection Voltage	CMPRS	Detection Voltage	CMPRS	Detection Voltage
00H	4.27V	10H	28.80 V	20H	5.33V	30H	38.40 V
01H	3.84V	11H	14.40 V	21H	4.80V	31H	19.20 V
02H	3.49V	12H	9.60 V	22H	4.36V	32H	12.80 V
03H	3.20V	13H	7.20 V	23H	4.00V	33H	9.60 V
04H	2.95V	14H	5.76 V	24H	3.69V	34H	7.68 V
05H	2.74V	15H	4.80 V	25H	3.43V	35H	6.40 V
06H	2.56V	16H	4.11 V	26H	3.20V	36H	5.49 V
07H	2.40V	17H	3.60 V	27H	3.00V	37H	4.80 V
08H	2.26V	18H	3.20 V	28H	2.82V	38H	4.27 V
09H	2.13V	19H	2.88 V	29H	2.67V	39H	3.84 V
0AH	2.02V	1AH	2.62 V	2AH	2.53V	3AH	3.49 V
0BH	1.92V	1BH	2.40 V	2BH	2.40V	3BH	3.20 V
0CH	1.83V	1CH	2.22 V	2CH	2.29V	3CH	2.95 V
0DH	1.75V	1DH	2.06 V	2DH	2.18V	3DH	2.74 V
0EH	1.67V	1EH	1.92 V	2EH	2.09V	3EH	2.56 V
0FH	1.60V	1FH	1.80 V	2FH	2.00V	3FH	2.40 V

10.4.3. R1C9/CMPCON1(CMP Control Register 1)

0X1C9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON1	CMPOE	CMPINV	CMPIS<5:0>					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPOE - Comparator result output enable

0: P67 as GPIO

1: Comparator result output from P67

Bit<6>: CMPINV - CMPOUT output result inversion

0: No Inversion

1: Inversion

Bit<5>: CMPIS<5> - Voltage source selection for voltage divider input

0: VDD

1: P60

Bit<4:3>: CMPIS<4:3> - Comparator positive input source selection

CMPIS<4>	CMPIS<3>	Positive Voltage Input Source
0	0	CIN0+/P66
0	1	Resistive Voltage Divider
1	0	VBG

Bit<2:0>: CMPIS<2:0> - Negative Input Source Selection for Comparator

CMPIS<2>	CMPIS<1>	CMPIS<0>	Negative Voltage Input Source
0	0	0	CIN0-/P66
0	0	1	CIN1-/P50
0	1	0	CIN2-/P65
0	1	1	CIN3-/P64
1	0	0	Resistive Voltage Divider
1	0	1	VBG

11. OPTION Configuration Table

CODE OPTION	Option	Function Description
Watchdog	Enable	Watchdog WDT Enable
	Disable	Watchdog WDT Disable
Clocks division	2 Clocks	Instruction Clock Division Selection 2 Clocks
	4 Clocks	Instruction clock division selection 4 Clocks
	8 Clocks	Instruction clock division selection 8 Clocks
	16 Clocks	Instruction clock division selection 16 Clocks
	32 Clocks	Instruction clock division selection 32 Clocks
Oscillation mode	IRC mode	Select the internal IHRC oscillator for the main clock
	LXT mode	Select external low-speed crystal oscillator for main clock
IRC frequency	1M	IRC frequency selection 1M
	4M	IRC frequency selection 4M
	8M	IRC frequency selection 8M
	16M	IRC frequency selection 16M
	32M	IRC frequency selection 32M (2clock selection is prohibited)
Low voltage reset option	Enable: LVR always	Default LVR function is always enabled
	Enabled: Software Control	LVR enable bit is software adjustable
Low Voltage Reset	LVR=1.2V	Low voltage reset point selection 1.2V
	LVR=1.6V	Low voltage reset point selection 1.6V
	LVR=1.8V	Low voltage reset point selection 1.8V
	LVR=2.2V	Low voltage reset point selection 2.2V
	LVR=2.4V	Low Voltage Reset Point Selection 2.4V
	LVR=2.6V	Low voltage reset point selection 2.6V
	LVR=3.3V	Low voltage reset point selection 3.3V
	LVR=3.5V	Low voltage reset point selection 3.5V
OTP paging selection	Use 2K	OTP ROM selection 2K storage space
	Use front 1K	OTP ROM selection front 1K storage space
	After using 1K	After selecting OTP ROM, 1K storage space
P63 reset pin pull-up	Enable	P63 reset pin hardware pull-up enabled
	Disable	P63 reset pin hardware pull-up disabled

P63 port	GPIO	P63 port as general input/output port
	RST	P63 port as external reset pin
Reset time	PWRT=3.5ms, WDT=7.1ms	Reset establishment time = 3.5ms, WDT overflow time (4 frequency division) = 7.1ms
	PWRT = 14ms, WDT = 28ms	Reset establishment time = 14ms, WDT overflow time (4 frequency division) = 28ms
	PWRT = 57ms, WDT = 114ms	Reset establishment time = 57ms, WDT overflow time (4 frequency division) = 114ms
	PWRT = 228ms, WDT = 455ms	Reset establishment time = 228ms, WDT overflow time (4 frequency division) = 455ms
	PWRT = 350us, WDT = 7.1ms	Reset establishment time = 350us, WDT overflow time (4 frequency division) = 7.1ms
	PWRT = 350us, WDT = 28ms	Reset establishment time = 350us, WDT overflow time (4 prescale) = 28ms
	PWRT = 350us, WDT = 114ms	Reset establishment time = 350us, WDT overflow time (4 prescale) = 114ms
	PWRT = 350us, WDT = 455ms	Reset establishment time = 350us, WDT overflow time (4 prescale) = 455ms
RTC	Enable	RTC function enable
	Disable	RTC function disable
Pull-up current drive enhancement	Enable	Port pull-up current drive enhancement function enable
	Disable	Port current drive enhancementfunction prohibited
Current Drive Enhancement	Enable	Port Current Drive Enhancement Enable
	Disable	Port Current Drive Enhancement Disable
CMP_FILT	Enable	Comparator Result Digital Filtering Enable
	Disable	Comparator Result Digital Filtering Disable
Comparator Hysteresis	Disable	Comparator Hysteresis Voltage Disable
	20mV	Comparator Hysteresis Voltage is 20mV
	40mV	Comparator hysteresis voltage is 40mV
	60mV	Comparator hysteresis voltage is 60mV
Package pin configuration	16pin	Chip package pin choice 16 pins
	14pin	Chip package pin choice 14 pins
	10pin	Chip package pin selection 10 pins
	8pin	Chip package pin selection 8 feet

12. Instruction set

Instruction	Instruction action	Flag bit effects
ADD A,R	A+R→A	Z,C,DC
ADD R,A	A+R→R	Z,C,DC
AND A,R	A&R→A	Z
AND R,A	A&R→R	Z
CLRA	0→A	Z
CLR R	0→R	Z
INVA R	/R→A	Z
INV R	/R→R	Z
DA	A register adjusted to BCD value	C
DECA R	R-1→A	Z
DEC R	R-1→R	Z
DJA R	R-1→A, skip if zero	-
DJ R	R-1→R, skip if zero	-
INCA R	R+1→A	Z
INC R	R+1→R	Z
IJA R	R+1→A, skip if zero	-
IJ R	R+1→R, skip if zero	-
MOV R,A	A→R	-
MOV A,R	R→A	Z
MOV R,R	R→R	Z
OR A,R	A∨R→A	Z
OR R,A	A∨R→R	Z
SUB A,R	R-A→A	Z,C,DC
SUB R,A	R-A→R	Z,C,DC
XOR A,R	A⊕R→A	Z
XOR R,A	A⊕R→R	Z
BTC R,b	0→R(b)	-
BTS R,b	1→R(b)	-
JBTC R,b	if R(b)=0, skip	-

JBTS R,b	if R(b)=1, skip	-
LCR R	R(n)→R(n+1),R(7)→C, C→R(0)	C
LCA R	R(n)→A(n+1),R(7)→C, C→A(0)	C
RCR R	R(n)→R(n-1),R(0)→C, C→R(7)	C
RCA R	R(n)→A(n-1),R(0)→C, C→A(7)	C
SWAP R	R(0-3) ↔ R(4-7)	-
SWAPA R	R(0-3)→A(4-7),R(4-7)→A(0-3)	-
ADD A,k	A+k→A	Z,C,DC
AND A,k	A&k→A	Z
MOV A,k	k→A	-
OR A,k	A∨k→A	Z
SUB A,k	k-A→A	Z,C,DC
XOR A,k	A⊕k→A	Z
CALL k	PC+1→[SP], (Page,k)→PC	-
DI	Interrupt Disable	-
EI	Enable Interrupt	-
JMP k	K (Page,k)→PC	-
NOP	No Operation	-
RET	[Stack Top]→PC	-
RETI	[Stack Top] → PC, Enable Interrupts	-
RETL k	k→A,[top of stack]→PC	-
SLEEP	0→WDT, oscillator stops oscillating (sleep mode)	T,P
CWDT	0→WDT	T,P
TBRD R	Machine code bit7～0 to ACC Machine code bit15～8 to R (general purpose register)	-

13. Electrical Characteristics

13.1. Limit Parameters

Operating Temperature..... -40℃～85℃
Storage Temperature..... -65℃～125℃
Input Voltage..... Vss-0.3V～Vdd+0.5V
Output Voltage..... Vss-0.3V～Vdd+0.5V
Operating Voltage..... 1.8V-5.5V

13.2. DC Electrical Characteristics

(VDD =5V, Operating Temperature =25℃, unless otherwise specified)

Symbol	Parameter Description	Condition	Minimum	Typical	Maximum	Unit
IRC1	IRC1 (after calibration)	OPTION select 32MHz	-	32	-	MHz
IRC2	IRC2 (after calibration)	OPTION select 16MHz	-	16	-	MHz
IRC3	IRC3 (after calibration)	OPTION select 8MHz	-	8	-	MHz
IRC3	IRC3 (after calibration)	OPTION select 4MHz	-	4	-	MHz
IRC4	IRC4 (after calibration)	OPTION select 1MHz	-	1	-	MHz
IOH1	High-level output drive	Ioh=4.4V	7	9	11	mA
IOH2	High level output drive	Ioh=4.4V	21	23	25	mA
IOL1	Low level output drive	Iol=0.6V	15	17	19	mA
IOL2	Low level output drive	Iol=0.6V	38	40	42	mA
RPH	Pull-up resistor	Pull-up enabled,	-	55	-	KΩ
RPD	Pull-down resistor	Pull-down enabled,	-	55	-	KΩ
Isb1	Shutdown current 1	Input connected to VDD, output floating	-	0.4	1	μA
Isb2	Shutdown Current 2	Input connected to VDD, output floating, WDT enabled	-	-	10	μA
Isb3	Shutdown Current 3	Input connected to VDD, output floating, ADC enabled	-	110	-	μA
Isb4	Shutdown Current 4	Input connected to VDD, output floating, CMP enabled	-	9	-	μA
Iop1	Operating Current 1 (VDD=5V)	IRC=32MHz 4clock	-	2.7	-	mA
Iop2	Operating Current 2 (VDD=5V)	IRC=16MHz 2clock	-	2.5	-	mA
Iop3	Operating Current 3 (VDD=5V)	IRC=8MHz 2clock	-	1.3	-	mA
Iop4	Working current 4 (VDD=5V)	IRC=4MHz 2clock	-	0.7	-	mA
Iop5	Working current 5 (VDD=5V)	IRC=1MHz 2clock	-	0.3	-	mA
LVR	Low voltage reset (1M 32CLOCK)	Select LVR reset point	-15%	Vlvr	+15%	V

13.3. AD conversion characteristics

(VDD = 5V, VSS = 0V, Operating temperature = 25° C)

Symbol	Parameter Description	Condition	Minimum	Typical	Maximum	Unit
V_{DD}	ADC operating	-	2.5	-	5.5	V
I_{VDD}	ADC operating	VDD=VREF=5V	-	110	-	uA
V_{AIN}	Analog input	-	V_{SS}	-	V_{REF}	V
EXVREF	External	-	2.0	-	V_{DD}	V
V_{REF}	Reference voltage output	VBG, 2V, 3V, 4V	-	±2	±3	%
T_{AD}	Conversion Clock Cycle	VDD=2.5～5.5V	1	-	-	us
T_{CN}	AD Conversion Time	VDD=2.5～5.5V	-	16	-	T AD
RN	Resolution	-	-	12	-	Bit
VDDmin	Minimum supply	-	-	VREF+0.5	-	V
E_{IL}	Integral error	V_{DD}=V_{REF}=5V	-	±8.0	-	LSB
E_{DL}	Differential		-	±4.0	-	LSB
E_{OFF}	Offset Error		-	±5.0	-	LSB
E_{GN}	Gain Error		-	±2.0	-	LSB

Note: The errors are derived from evaluation and are not tested during production

13.4. Comparator Characteristics

(VDD = 5V, VSS = 0V, Ta = 25℃)

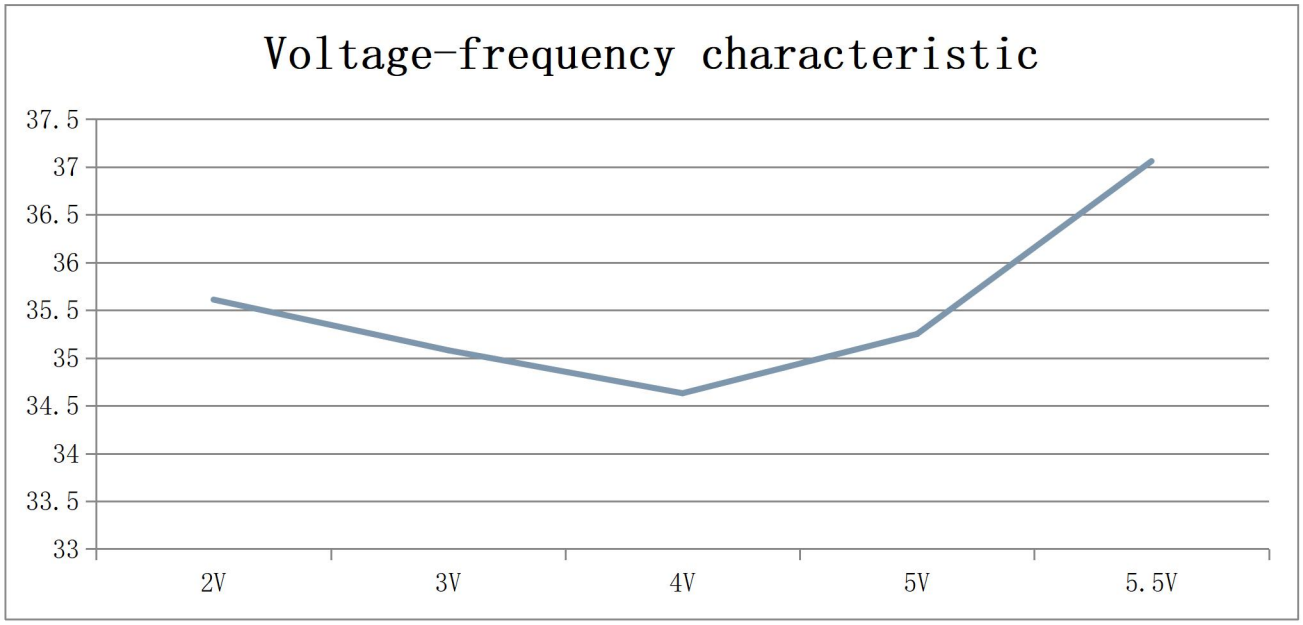
Symbol	Parameters	Minimum	Typical	Maximum	Unit	Condition
V_{DD}	Operating Voltage Range	1.8	-	5.5	V	25℃
Vos	Comparator Hysteresis Voltage	-	20	-	mV	25℃
		-	40	-	mV	
		-	60	-	mV	
Tr	Comparator Response Time	-	50	-	ns	25℃, VDD=5V Disable Digital Filtering
		-	360	-	ns	
		-	60	-	us	25℃, VDD=5V Digital Filtering Enable

13.5. Characteristic Curve Graph

The curves listed in this chapter are for design reference only. Some of the data provided may exceed the specified operating range of the chip. To ensure the normal operation of the chip, please strictly adhere to the electrical characteristics description.

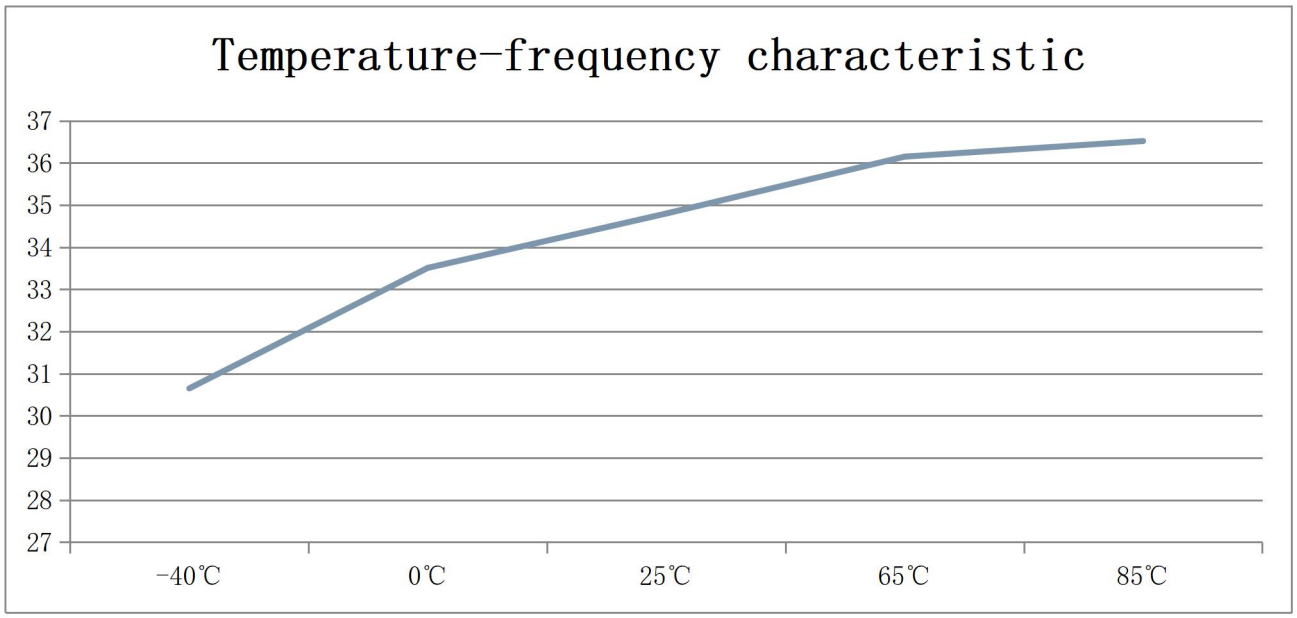
13.5.1. Internal Low-Speed Oscillator - Pressure Frequency Characteristic Curve

Under the condition of operating temperature at 25℃: (Unit: KHz)



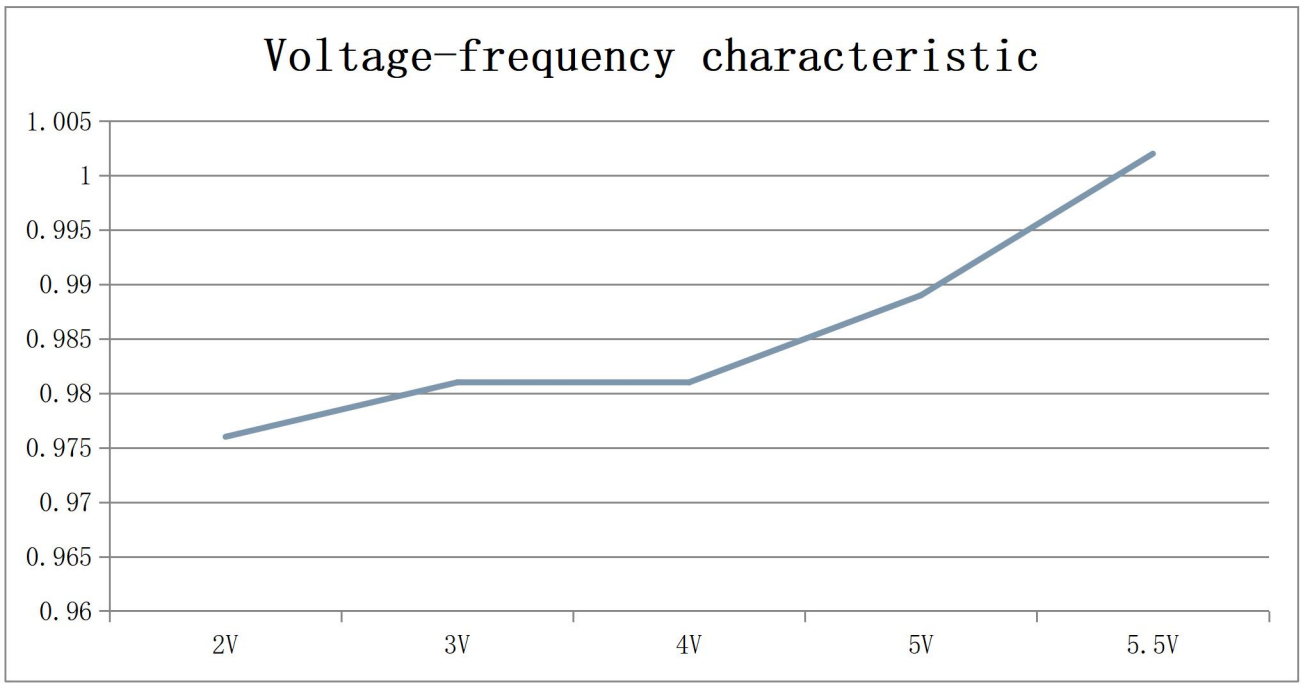
13.5.2. Internal Low-Speed Oscillator - Temperature Frequency Characteristic Curve

Under the condition of operating voltage at 5V: (Unit: KHz)



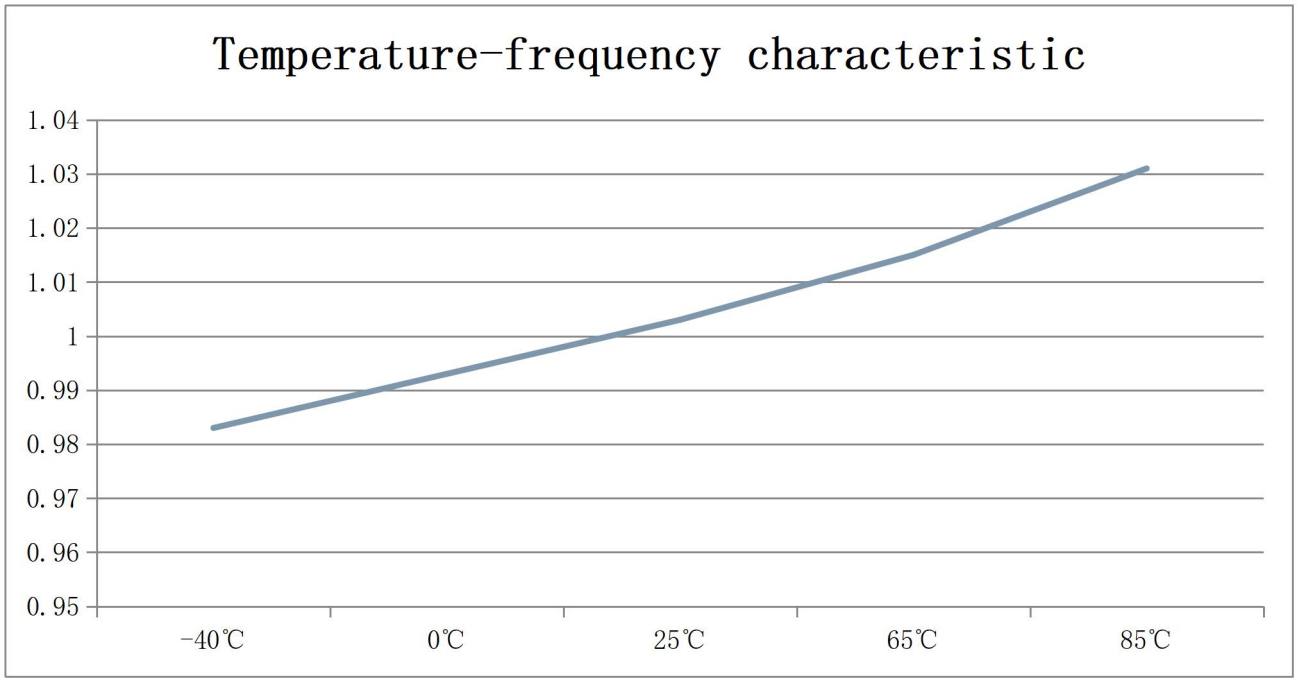
13.5.3. Internal 1MHz RC Oscillator - Pressure Frequency Characteristic Curve

Under the condition of operating temperature at 25℃: (Unit: MHz)



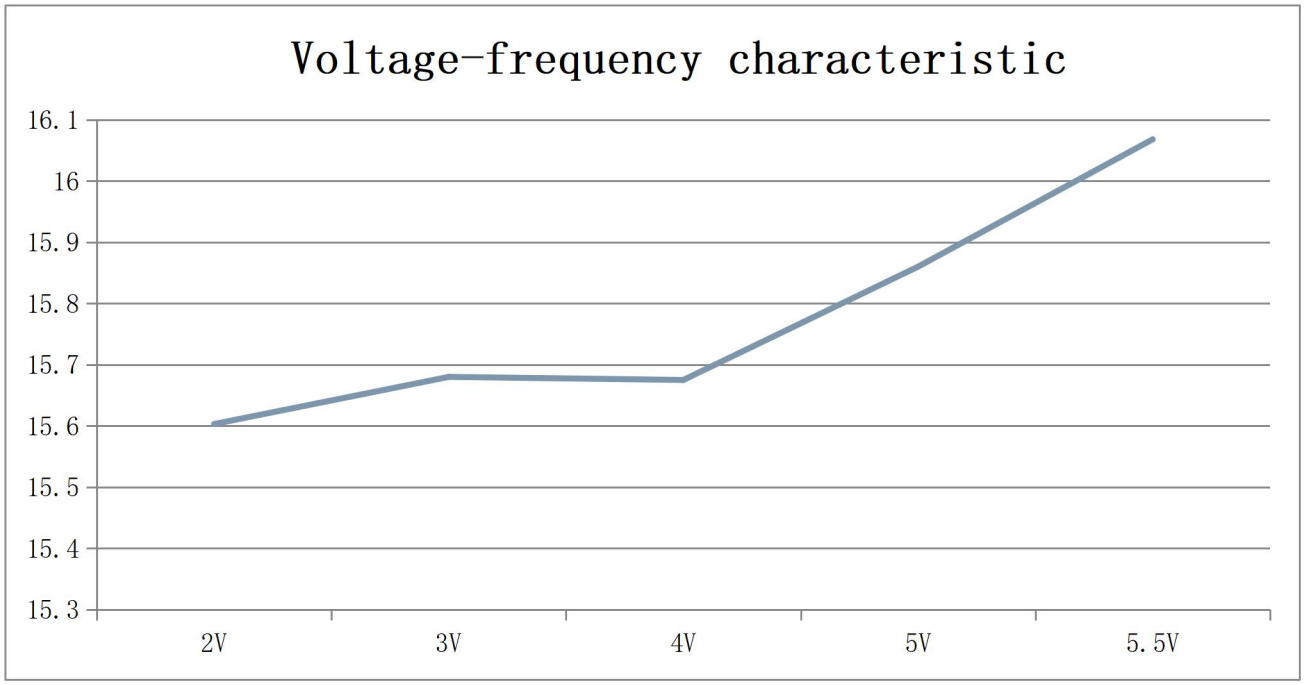
13.5.4. Internal 1MHz RC Oscillator - Temperature Frequency Characteristic Curve

Operating voltage at 5V condition: (unit MHz)



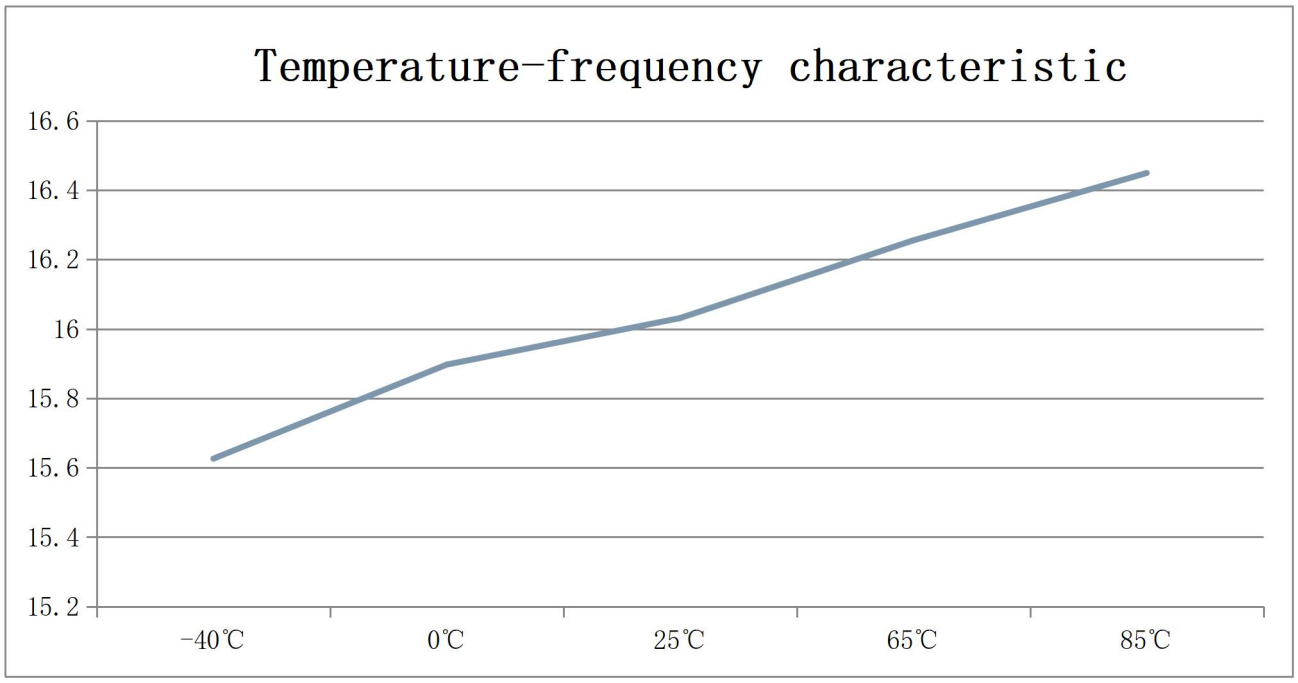
13.5.5. Internal 16MHz RC oscillator - frequency versus voltage characteristics curve

Under the condition of operating temperature at 25℃: (Unit: MHz)



13.5.6. Internal 16MHz RC oscillator - frequency versus temperature characteristics curve

Operating voltage at 5V condition: (unit MHz)



13.6. IHRC frequency trimming parameter description

Parameter description is for trend reference only, actual values may vary.

IHRCCAL tuning value (HEX)	Frequency (MHz)	Tuning deviation (IHRCCAL=0x7F)	IHRCCAL tuning value (HEX)	Frequency (MHz)	Tuning deviation (IHRCCAL=0x7F)
00	7.8685	-51.27%	80	14.7633	-8.56%
01	7.8989	-51.08%	81	14.8206	-8.21%
02	7.9306	-50.88%	82	14.8799	-7.84%
03	7.9615	-50.69%	83	14.9406	-7.46%
04	7.9946	-50.48%	84	14.9875	-7.17%
05	8.0244	-50.30%	85	15.0587	-6.73%
06	8.0567	-50.10%	86	15.1219	-6.34%
07	8.0900	-49.89%	87	15.1816	-5.97%
08	8.1230	-49.69%	88	15.2429	-5.59%
09	8.1554	-49.49%	89	15.3056	-5.20%
0A	8.1911	-49.27%	8A	15.3653	-4.83%
0B	8.2221	-49.08%	8B	15.4271	-4.45%
0C	8.2612	-48.83%	8C	15.4962	-4.02%
0D	8.2928	-48.64%	8D	15.5627	-3.61%
0E	8.3260	-48.43%	8E	15.6262	-3.22%
0F	8.3594	-48.23%	8F	15.6900	-2.82%
10	8.3979	-47.99%	90	15.7579	-2.40%
11	8.4313	-47.78%	91	15.8226	-2.00%
12	8.4694	-47.54%	92	15.8758	-1.67%
13	8.5057	-47.32%	93	15.9582	-1.16%
14	8.5400	-47.11%	94	16.0252	-0.75%
15	8.5790	-46.87%	95	16.0920	-0.33%
16	8.6136	-46.65%	96	16.1644	0.11%
17	8.6503	-46.42%	97	16.2341	0.55%
18	8.6891	-46.18%	98	16.3050	0.99%
19	8.7255	-45.96%	99	16.3822	1.46%
1A	8.7629	-45.73%	9A	16.4535	1.91%
1B	8.8015	-45.49%	9B	16.5289	2.37%
1C	8.8443	-45.22%	9C	16.6084	2.87%
1D	8.8817	-44.99%	9D	16.6874	3.35%
1E	8.9246	-44.73%	9E	16.7538	3.77%
1F	8.9603	-44.50%	9F	16.8327	4.25%
20	9.0002	-44.26%	A0	16.9115	4.74%
21	9.0346	-44.04%	A1	16.9946	5.26%
22	9.0782	-43.77%	A2	17.1022	5.92%
23	9.1206	-43.51%	A3	17.1442	6.18%

24	9.1629	-43.25%	A4	17.2501	6.84%
25	9.2062	-42.98%	A5	17.3241	7.30%
26	9.2536	-42.69%	A6	17.4032	7.79%
27	9.2929	-42.44%	A7	17.4754	8.23%
28	9.3373	-42.17%	A8	17.5911	8.95%
29	9.3862	-41.87%	A9	17.6619	9.39%
2A	9.4265	-41.62%	AA	17.7601	10.00%
2B	9.4737	-41.32%	AB	17.8608	10.62%
2C	9.5194	-41.04%	AC	17.9364	11.09%
2D	9.5634	-40.77%	AD	18.0114	11.55%
2E	9.6137	-40.46%	AE	18.1189	12.22%
2F	9.6657	-40.13%	AF	18.2237	12.87%
30	9.7111	-39.85%	B0	18.3181	13.45%
31	9.7610	-39.54%	B1	18.4032	13.98%
32	9.8052	-39.27%	B2	18.4694	14.39%
33	9.8555	-38.96%	B3	18.5649	14.98%
34	9.9056	-38.65%	B4	18.6502	15.51%
35	9.9545	-38.35%	B5	18.7591	16.19%
36	10.0069	-38.02%	B6	18.8554	16.78%
37	10.0607	-37.69%	B7	18.9598	17.43%
38	10.1097	-37.38%	B8	19.0521	18.00%
39	10.1618	-37.06%	B9	19.1623	18.68%
3A	10.2126	-36.75%	BA	19.2432	19.18%
3B	10.2720	-36.38%	BB	19.3453	19.82%
3C	10.3227	-36.07%	BC	19.4602	20.53%
3D	10.3786	-35.72%	BD	19.5515	21.09%
3E	10.4337	-35.38%	BE	19.6595	21.76%
3F	10.4836	-35.07%	BF	19.7762	22.49%
40	10.5419	-34.71%	C0	19.8803	23.13%
41	10.6021	-34.34%	C1	19.9999	23.87%
42	10.6584	-33.99%	C2	20.1009	24.50%
43	10.7153	-33.63%	C3	20.2071	25.15%
44	10.7758	-33.26%	C4	20.3154	25.82%
45	10.8314	-32.91%	C5	20.4301	26.54%
46	10.8925	-32.54%	C6	20.5520	27.29%
47	10.9519	-32.17%	C7	20.6728	28.04%
48	11.0149	-31.78%	C8	20.8597	29.20%
49	11.0798	-31.38%	C9	20.9218	29.58%
4A	11.1415	-30.99%	CA	21.0434	30.33%
4B	11.2065	-30.59%	CB	21.1664	31.10%
4C	11.2811	-30.13%	CC	21.2888	31.85%
4D	11.3397	-29.77%	CD	21.4206	32.67%
4E	11.4024	-29.38%	CE	21.5467	33.45%

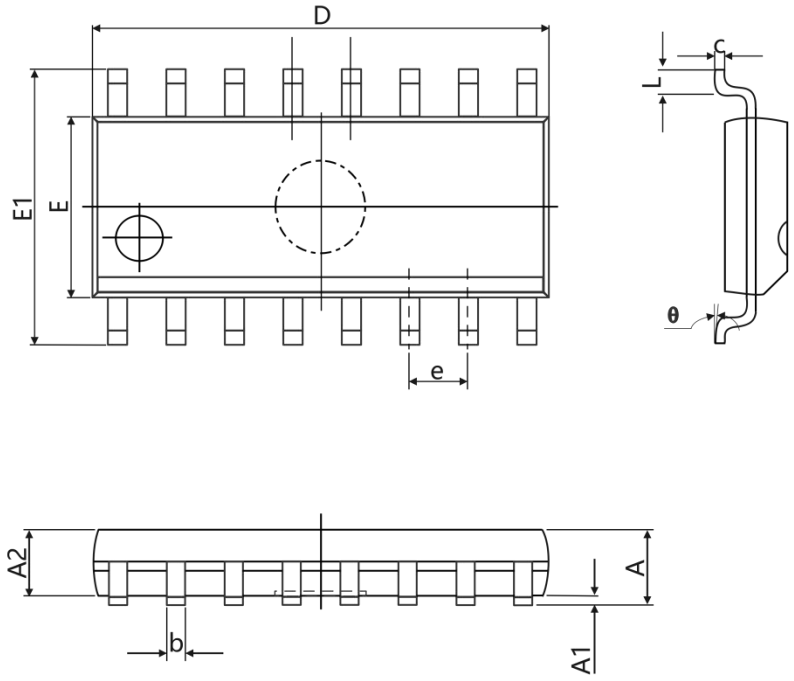
4F	11.4741	-28.93%	CF	21.6666	34.19%
50	11.5460	-28.49%	D0	21.7945	34.99%
51	11.6136	-28.07%	D1	21.9343	35.85%
52	11.6864	-27.62%	D2	22.0665	36.67%
53	11.7510	-27.22%	D3	22.2033	37.52%
54	11.8237	-26.77%	D4	22.3494	38.42%
55	11.8957	-26.32%	D5	22.4765	39.21%
56	11.9714	-25.85%	D6	22.6220	40.11%
57	12.0446	-25.40%	D7	22.7328	40.80%
58	12.1222	-24.92%	D8	22.9036	41.85%
59	12.1995	-24.44%	D9	23.0364	42.68%
5A	12.2718	-23.99%	DA	23.1816	43.58%
5B	12.3573	-23.46%	DB	23.3294	44.49%
5C	12.4258	-23.04%	DC	23.4603	45.30%
5D	12.5138	-22.50%	DD	23.6235	46.31%
5E	12.5884	-22.03%	DE	23.7779	47.27%
5F	12.6776	-21.48%	DF	23.9420	48.29%
60	12.7655	-20.94%	E0	24.1088	49.32%
61	12.8476	-20.43%	E1	24.2740	50.34%
62	12.9325	-19.90%	E2	24.4546	51.46%
63	13.0183	-19.37%	E3	24.6332	52.57%
64	13.1138	-18.78%	E4	24.7976	53.59%
65	13.2061	-18.21%	E5	24.9741	54.68%
66	13.2976	-17.64%	E6	25.1388	55.70%
67	13.3926	-17.05%	E7	25.3200	56.82%
68	13.4878	-16.46%	E8	25.4950	57.90%
69	13.5799	-15.89%	E9	25.6810	59.06%
6A	13.6794	-15.28%	EA	25.8604	60.17%
6B	13.7778	-14.67%	EB	26.0300	61.22%
6C	13.8836	-14.01%	EC	26.2191	62.39%
6D	13.9823	-13.40%	ED	26.4211	63.64%
6E	14.0871	-12.75%	EE	26.6126	64.83%
6F	14.1931	-12.09%	EF	26.8000	65.99%
70	14.3019	-11.42%	F0	27.0091	67.28%
71	14.4097	-10.75%	F1	27.1812	68.35%
72	14.5217	-10.06%	F2	27.3823	69.59%
73	14.6339	-9.36%	F3	27.6009	70.95%
74	14.7487	-8.65%	F4	27.7993	72.18%
75	14.8661	-7.93%	F5	27.9843	73.32%
76	14.9850	-7.19%	F6	28.2271	74.83%
77	15.1078	-6.43%	F7	28.4457	76.18%
78	15.2292	-5.68%	F8	28.6658	77.54%
79	15.3525	-4.91%	F9	28.9211	79.12%

7A	15.4803	-4.12%	FA	29.1583	80.59%
7B	15.6073	-3.34%	FB	29.3971	82.07%
7C	15.7431	-2.49%	FC	29.5810	83.21%
7D	15.8757	-1.67%	FD	29.8559	84.91%
7E	16.0069	-0.86%	FE	30.1299	86.61%
7F	16.1458	0.00%	FF	30.3641	88.06%

14. Package Size

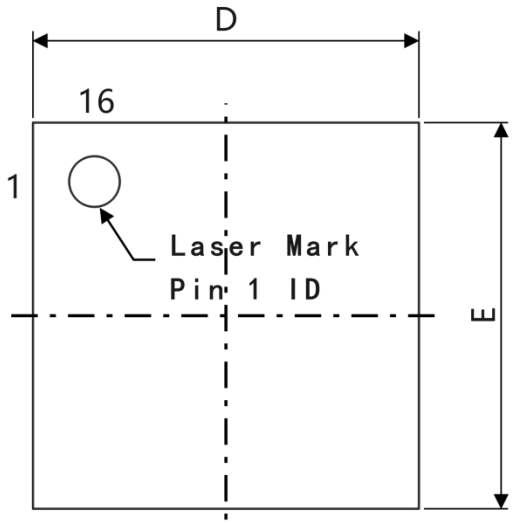
14.1. 16PIN Package Size

(Unit: mm)

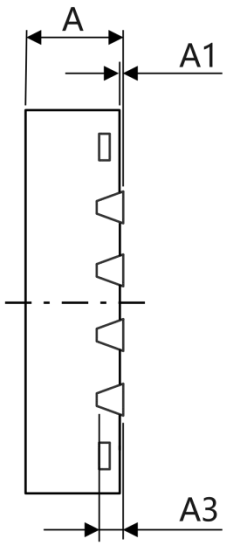


Symbol	Dimensions In Millimeter		Dimensions In Lnches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

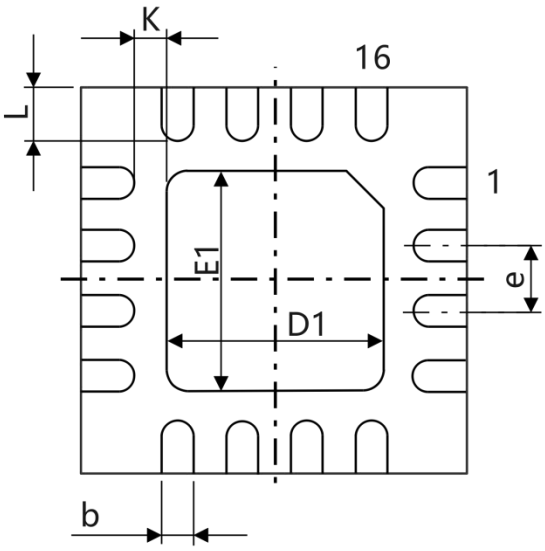
SOP16 Package Size



Top View



Side View

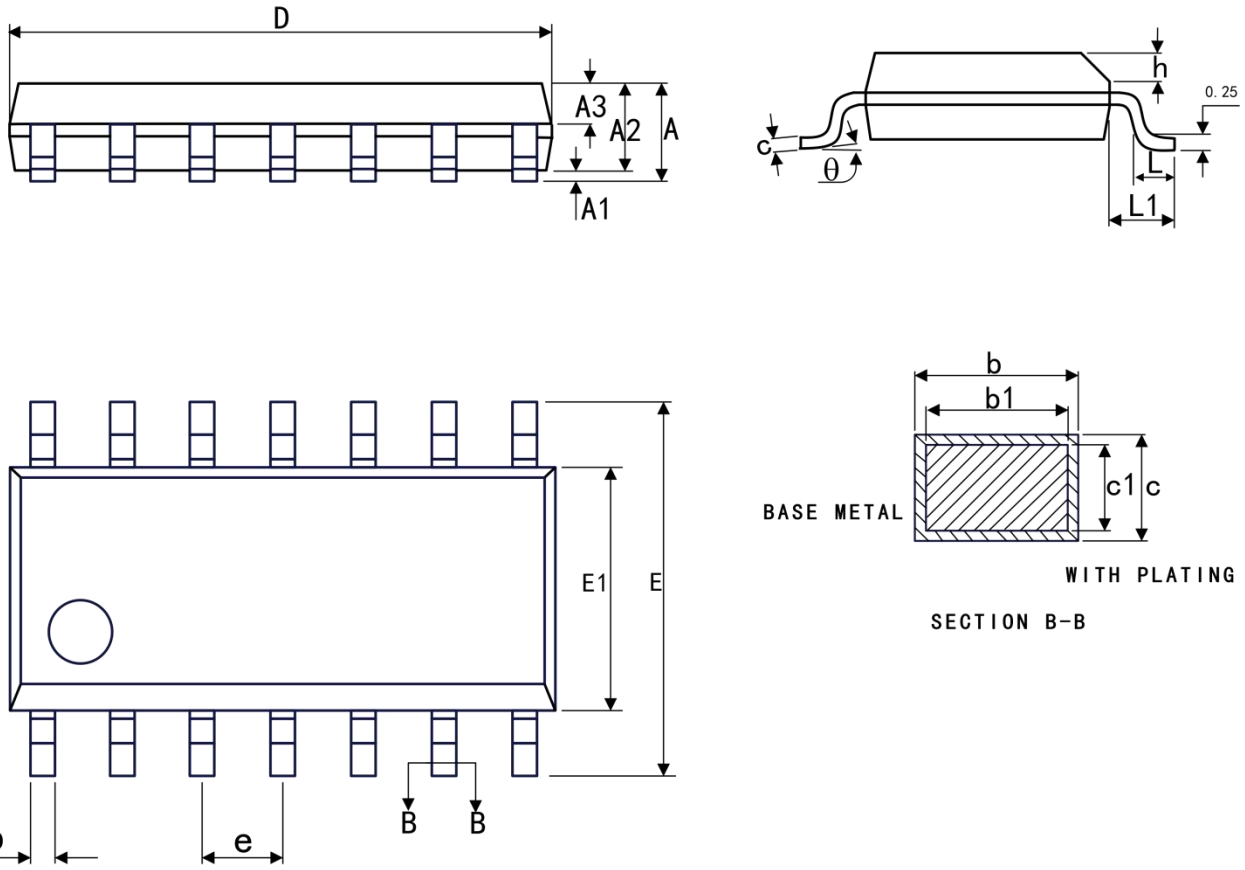


Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e	0.50TYP		
K	0.20	—	—
L	0.30	0.40	0.50

QFN16 Package Size

14.2. 14PIN Package Size

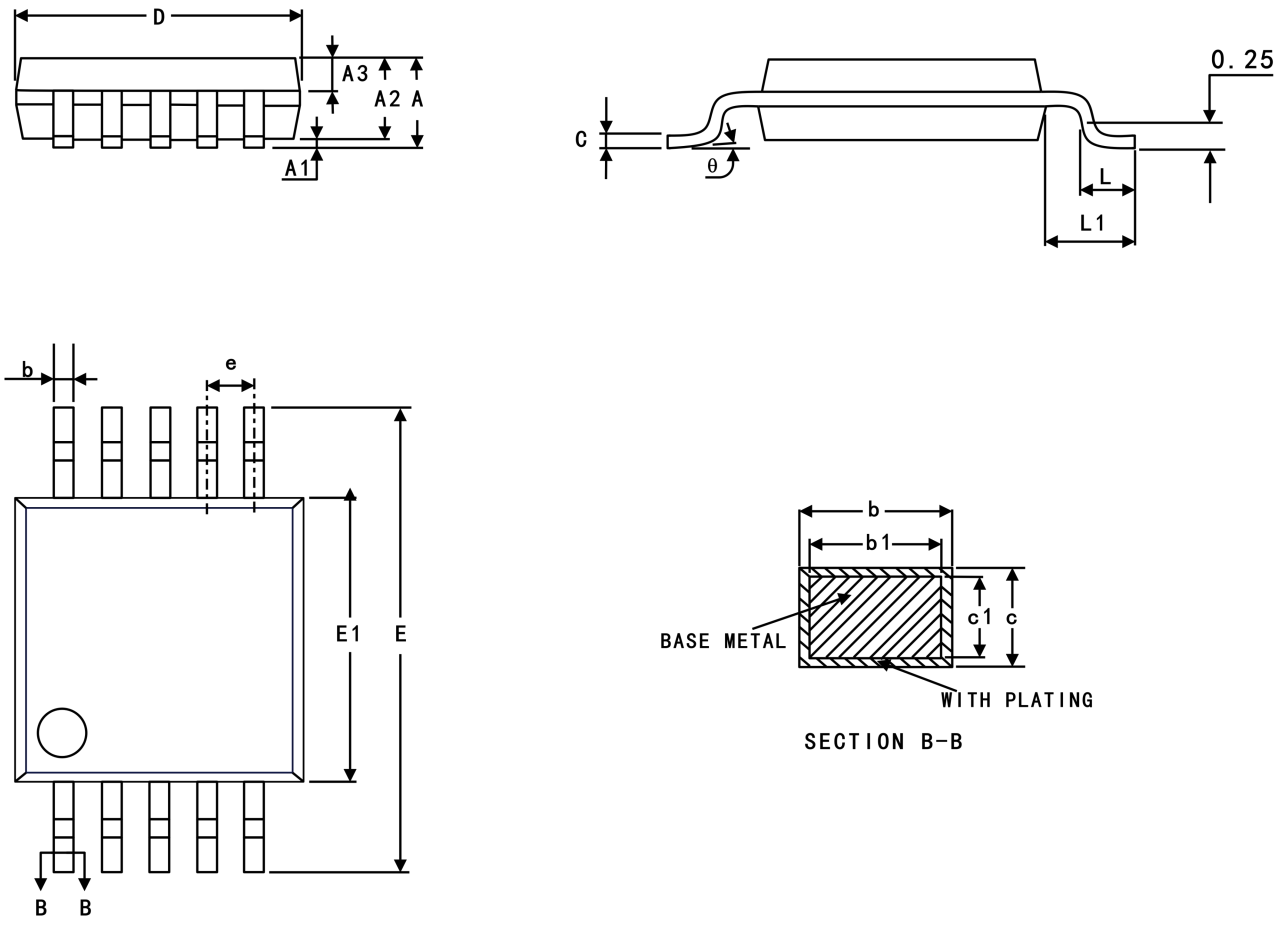


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

SOP14 package size

14.3. 10PIN package Size

(Unit: mm)

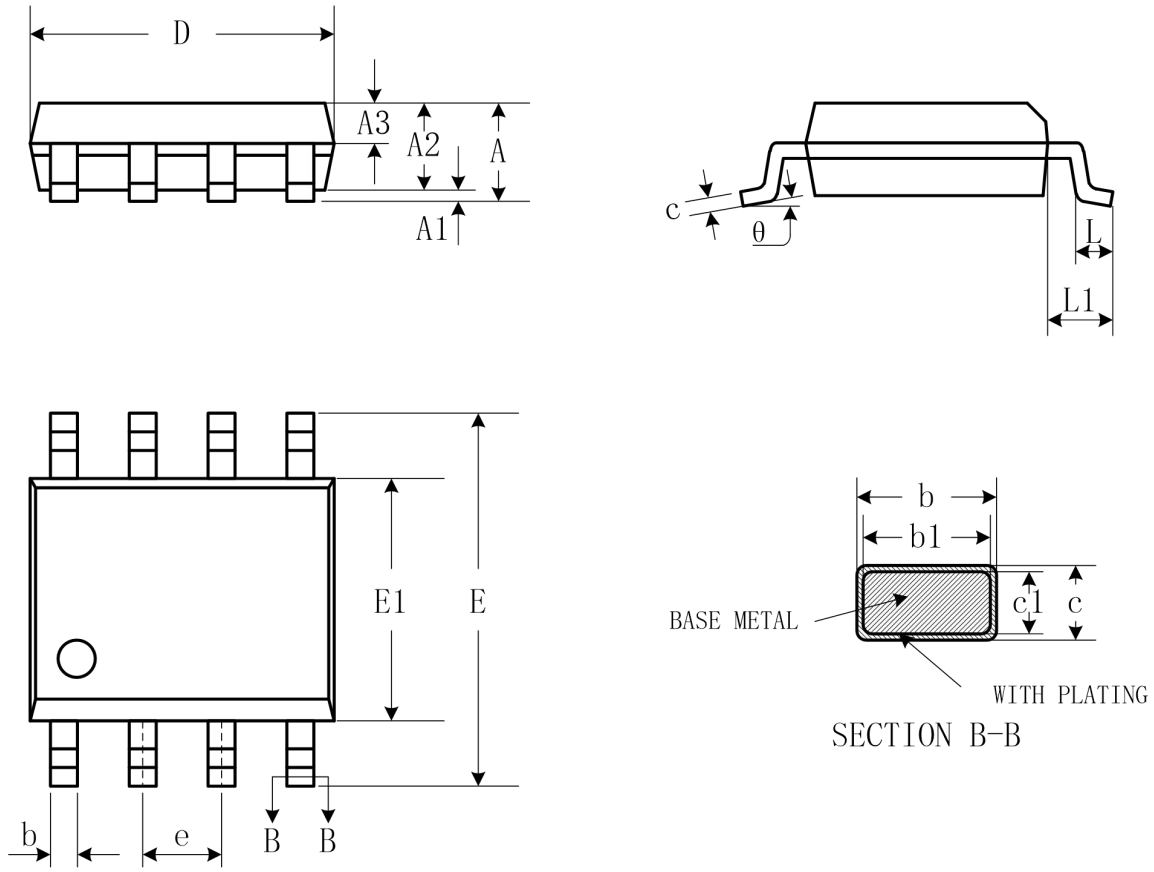


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	_	_	1.10
A1	0.05	_	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18	_	0.26
b1	0.17	0.20	0.23
c	0.15	_	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.50BSC		
L	0.40	_	0.70
L1	0.95REF		
θ	0	-	8°

MSOP10 package size

14.4. 8PIN package Size

(Unit: mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	-	8°

SOP8 package size