JZ8PE155E

8-BIT Microcontroller with OTP ROM

Version 1.0

Description of Modification Records

Version number	Modification Description	note
V1.0	Initial version	

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1 General Description

JZ8PE155E is an 8-bit MCU with high speed and low power consumption based on CMOS technology, with built-in 1K×14Bit disposable programmable read-only memory (OTP-ROM), and provides protection bits to protect instruction codes.

The core of JZ8PE155E is an embedded 8-Bit CPU, the chip contains 48×8Bit SRAM, 128× 8-bit EEPROM, 11 input and output exits, interrupt controller, on-chip RC oscillator, timer/counter, watchdog circuit. It is a powerful microcontrol circuit. As a universal MCU, JZ8PE155E is mainly used in home appliances, consumer electronic products and industrial automation control.

2 Product Features

2.1 CPU Configuration

- 1K x 14-Bit OTP ROM
- 48 x 8-Bit SRAM
- 128×8-Bit EEPROM
- Level 5 stack space
- Less than 2 mA (4MHz/5V)
- Less than 30 μA (32KHz/3V)
- Less than 1 μA (sleep mode)

2.2 I/O Configuration

- 2 groups of bidirectional IO ports :P5, P6
- 11 I/O pins (P63 output low only)
- Wake up port :P6
- 11-bit programmable pull-up I/O pins
- 11-bit programmable drop-down I/O pin
- External interrupt :P60
- P63 can be configured with pull up and open drain output
- Port driver can be enhanced

2.3 Operating voltage range

- Working voltage range:
  1.8V ~ 5.5V (0℃-70℃)
  2.3V ~ 5.5V (-40℃-85℃)
- Operating temperature -40℃-85℃

2.4 Operating frequency range

- External crystal oscillator HXT, LXT
- Built-in RC oscillation circuit:
  455KHz/1MHz/4MHz/8MHz
- Clock cycle frequency selection:
  2Clock/4Clock/8Clock/16Clock

2.5 Low Voltage Reset

- 1.2V±0.3V, 1.5V±0.3V
- 1.7V±0.3V, 2.2V±0.2V
- 2.5V±0.2V, 3.0V±0.2V
- 3.3V±0.2V, 3.6V±0.2V

2.6 Interrupt Source

- TCC overflow interrupt
- External interrupt
- Input port status change interrupt
- T1 interrupt
- E2P write completion interrupt
- PWM cycle interrupte
- PWM duty cycle interrupte

2.7 PWM Output

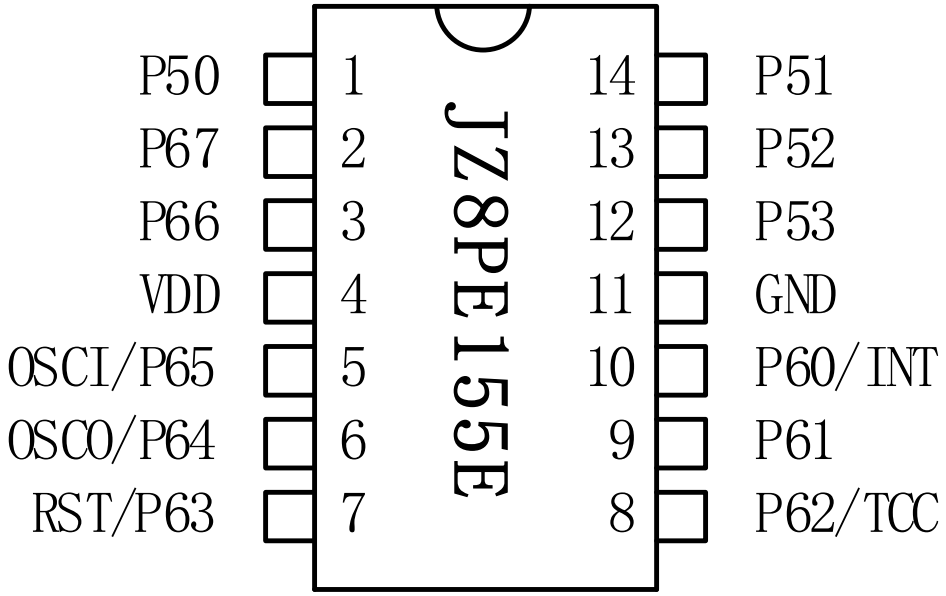
- 1×8bit PWM;

2.8 Package Type

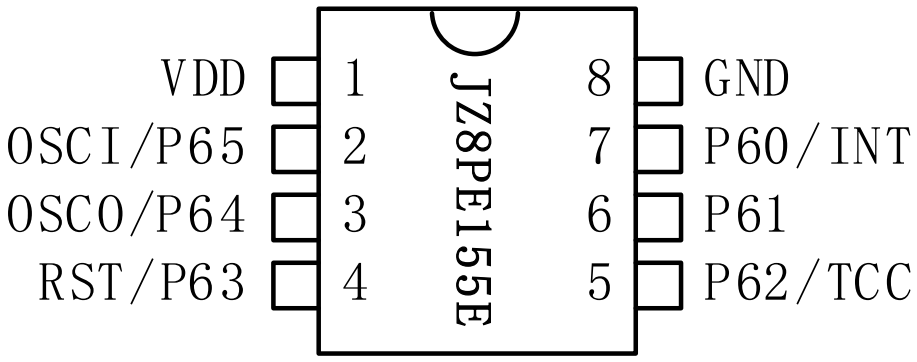
- JZ8PE155E SOP14/DIP14
- JZ8PE155E SOP8

3 Pin description

3.1 Pin assignment



JZ8PE155E-14PIN map



JZ8PE155E-8PIN map

3.2 Pin description

3.2.1 14PIN foot position

Pin number	Name of pin	Pin Function	attribute
1	P50	Universal I/O port Programmable pull up/drop down	GPIO port
2	P67	Universal I/O port Programmable pull up/drop down Wake up from sleep mode when the pin state changes	GPIO port
3	P66	Universal I/O port Programmable pull up/drop down Wake up from sleep mode when the pin state changes	GPIO port
4	VDD	Positive power supply	Positive power supply
5	P65/OSCI	Universal I/O port Programmable pull up/drop down OSCI Wake up from sleep mode when the pin state changes	GPIO port
6	P64/OSCO	Universal I/O port Programmable drop-down/drop-down OSCO Wake up from sleep mode when the pin state changes	GPIO port
7	P63/RST	Universal I mouth/reset foot Burning configuration pull-up/openable leakage output Wake up from sleep mode when the pin state changes	GPI mouth
8	P62/TCC/PWM	Programmable pull-up/pull-down of the universal I/O port The external input is the TCC reference PWM output Wake up from sleep mode when the pin state changes	GPIO port
9	P61	Universal I/O port Programmable pull up/drop down Wake up from sleep mode when the pin state changes	GPIO port
10	P60/EXINT	Universal I/O port Programmable pull up/drop down External interrupt input port	GPIO port

		Wake up from sleep mode when the pin state changes	
11	GND	to	Negative power supply pole
12	P53	Universal I/O port Programmable pull up/drop down	GPIO port
13	P52	Universal I/O port Programmable pull up/drop down	GPIO port
14	P51	Universal I/O port Programmable pull up/drop down	GPIO port

4 Memory Structure

4.1 Data Store Structure

The data store is divided into RPAGE registers and IOPAGE registers. The RPAGE register includes the general register and the operation register. The operation register is located in the low address unit 00H ~ 0FH, and the general register address range is 10H ~ 3FH. The IOPAGE register includes only special function registers and ranges from 00H to 0FH.

The structure distribution of data storage area is shown in the following table:

address	RPAGE register	IOPAGE register
0x00	R0/RIND(indirect addressing register)	keep
0x01	R1/TCC(TCC counter)	keep
0x02	R2/PCL(program counter low)	keep
0x03	R3/STATUS(status register)	keep
0x04	R4/FSR(RAM selection register)	keep
0x05	R5/P5(PORT5 port data Register)	IOC5/P5CR (P5 direction control register)
0x06	R6/P6(PORT6 port data register)	IOC6/P6CR (P6 direction control register)
0x07	R7/T1(T1 counter)	IOC7/PRD(PWM cycle register)
0x08	R8/T1CON(T1 control register)	IOC8/DT(PWM duty cycle register)
0x09	R9/E2PADR(E2P address register)	IOC9/PHDCR(pull down control register)
0x0A	RA/E2PDAT(E2P data register)	keep
0x0B	RB/E2PCON(E2P control register)	IOCB/PDCR(drop down control register)
0x0C	RC/E2PREAD(E2P read register read-only)	IOCC/T2(T2 timer)
0x0D	RD/WUCON(input change interrupt enable register)	IOCD/PHCR(pull up control register)
0x0E	RE/T2CON(T2/PWM control register)	IOCE/WDE(Watchdog Control Register)
0x0F	RF/INTFLAG(Interrupt status register)	IOCF/RIEN(interrupt enable register)
0x10 ~ 0x3F	General purpose register	keep

4.2 RPAGE memory

4.2.1 R0/RIND (Indirect Address Memory)

The indirection register is not an actual register; its main function is to serve as a pointer to indirection.

4.2.2 R1/TCC (TCC counter)

TCC is an 8Bit upstream counter with an optional clock source, internal/external clock, count overflow to form interrupts, and TCC can be read and written.

4.2.3 R2/PCL (Program counter)

A program counter (PC) is a pointer that records the instructions to be processed by the CPU during each instruction cycle.During the CPU cycle, the PC pushes the instruction pointer into the program memory and then incrementalizes the pointer by one to proceed to the next cycle.

4.2.4 R3/STATUS (status register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RST	GB1	GB0	T	P	Z	DC	C

Bit7 RST: Reset type flag bit:
0: indicates another reset type
1: Pin state change causes wake up

Bit6 GB1: When RTC is turned off in OPTION, it is used as the universal read/write bit.

When RTC is enabled in OPTION, as :TCCWKEN;
TCC wake up procedure:
WDT was enabled on the hardware. Procedure
The software closes the WDT
Set TCCWKEN=1 (LXT continues to work during hibernation and stops LXT when TCCWKEN=0)
Enable TCC interrupt (TCIE=1)
ENI or DISI(ENI wakes up to interrupt, DISI wakes up to continue)
Execute sleep instruction (SLEP)
No need to set up a pre-divider for WDT
WDT will be automatically enabled after wake up, and the software needs to disable WDT

Bit5 GB0: indicates the common read/write bit

Bit4T: indicates the time overflow bit
0:WDT overflows
1: Execute the "SLEEP" and "WDTC" commands or low-voltage reset

Events affecting T/P are shown in the following table:

type	RST	T	P
Power-on reset	0	1	1
Press RESET in working mode	0	keep	keep
RESET wake up	0	1	0
The WDT overflows in working mode. Procedure	0	0	keep
WDT overflows wake up	0	0	0
Wake up when the port status changes	1	1	0
Execute the WDTC command	keep	1	1
Execute the SLEEP instruction	keep	1	0

Bit3 P- Power failure flag bit:

0: Execute the SLEEP command

1: Power-on reset or run the WDTC command

Bit2 Z-zero flag bit: Set to "1" if the result of an arithmetic or logical operation is zero

0: When the result of an arithmetic or logical operation is not 0

1: When the result of an arithmetic or logical operation is 0

Bit1 DC- Auxiliary carry flag:

0: The low four bits are not carried during the addition operation. When/performs subtraction, the lower four bits generate a borrow

1: The low four bits are carried when the addition operation is performed. The lower four digits did not generate a borrow when the subtraction was performed

Bit0 C-carry flag:

0: No carry is generated for the high four digits during addition operation. When the subtraction is performed, the higher four bits generate a borrow

1: When the addition operation is performed, the high four bits are carried. No borrowings are generated for the higher four digits when the subtraction is performed

4.2.5 R4/FSR (RAM selection register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	FSR<5:0>					

FSR<7:6> is always "1", and the FSR register is readable and writable

FSR<5:0> is used to select the RAM register address in indirect addressing mode (addressing range :0X00 ~ 0X3F)

FSR is used in conjunction with R0 to implement indirect addressing operations. The user can put the address corresponding to a register into the FSR and then access

the indirect address register R0, which will point to the register corresponding to the address in the FSR.

4.2.6 R5/P5 (PORT5 data register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	P53	P52	P51	P50

Port input/output register, the P5 port is 4 bits
P5 is the read-write register

4.2.7 R6/P6 (PORT6 data register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P67	P66	P65	P64	P63	P62	P61	P60

Port input/output register, P6 port is 8 bits
P6 is a read-write register

4.2.8 R7/T1 (T1 counter)

T1 is an 8-bit upstream counter with an optional internal/external clock source, count overflows to form interrupts, and T1 can be read and written.

4.2.9 R8/T1CON (T1 control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1RTCS	0	0	0	T1PSR3	T1PSR2	T1PSR1	T1PSR0

Bit<3:0> T1PSR3~T1PSR0:T1 pre-division selection control bit:

T1PSR3	T1PSR2	T1PSR1	T1PSR0	T1 frequency division coefficient
0	0	0	0	1:1
0	0	0	1	1:2
0	0	1	0	1:4
0	0	1	1	1:8
0	1	0	0	1:16
0	1	0	1	1:32
0	1	1	0	1:64
0	1	1	1	1:128
1	0	0	0	1:256

Bit6 to Bit4 are not used and the value is fixed to 0
When RTC is turned off in OPTION:
Bit7 Universal read/write bit
When RTC is enabled in OPTION:
Bit7 T1RTCS:T1 signal source selection

1: Select the external crystal oscillator clock (LXT 4 frequency division)

0: internal instruction cycle clock

The T1CON register can be read and written.

4.2.10 R9/E2PADR (E2P address register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	E2PADR<6:0>						

Bit<6:0> :E2P address bit

Bit7: Not used, fixed to 0

4.2.11 RA/E2PDAT (E2P Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E2PDAT<7:0>							

Bit<7:0>:E2P writes data bits

4.2.12 RB/E2PCON (E2P control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E2PWKEN	-	-	-	E2PISAVB	E2PSTATIC	E2PRDEN	E2PWREN

Bit<0>:E2PWREN:

1:E2P write enable (self-defining 0 after E2P write is completed, write operation will continue to be completed directly when sleeping)

0: The E2P write is complete/The E2P write is closed (if the 0 is not automatically cleared for a long time, the write fails and the software needs to clear the 0.)

Bit<1>:E2PRDEN:

1:E2P read enable (Enable E2P, wait for one instruction cycle to start reading E2P (MOV A, 0x0C) valid, continuous read, disable read after reading the required data)

0:E2P read is forbidden

Bit<3:2>:E2P reads the speed control bit

11: High speed mode (reading speed 4MHz)

00: Energy saving mode (reading speed <500KHz)

Bit<6:4>: not used, fixed to 0

Bit<7>:E2PWKEN:E2P wake up enable bit

1:E2P wake up enable (wake up sleep mode after E2P is written)

0:E2P wakes up forbid

4.2.13 RC/E2PREAD (E2P Read Data Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E2PREAD<7:0>							

Bit<7:0>:E2P reads the data bit

4.2.14 RD/WUCON (Input Port Status Change interrupt Enable Control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUEN<7>	WUEN<6>	WUEN<5>	WUEN<4>	WUEN<3>	WUEN<2>	WUEN<1>	WUEN<0>

Bit7 WUEN<7>:P67 Input status change interrupt control bit
Bit6 WUEN<6>:P66 Input status change interrupt control bit
Bit5 WUEN<5>:P65 Input status change interrupt control bit
Bit4 WUEN<4>:P64 Input status change interrupt control bit
Bit3 WUEN<3>:P63 Input status change interrupt control bit
Bit2 WUEN<2>:P62 Input status change interrupt control bit
Bit1 WUEN<1>:P61 Input status change interrupt enable control bit
Bit0 WUEN<0>:P60 Input status change interrupt control bit
1: indicates that the function is enabled
0: Disable

Note: In OPTION, if port is not independent control, port wake-up is not controlled by the WUCON register. Otherwise, you need to process WUCON; otherwise, the port cannot be woken up.

4.2.15 RE/T2CON (T2/PWM control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB_EN	-	-	PWMEN	T2EN	T2PT<2>	T2PT<1>	T2PT<0>

Bit<2:0>:T2 timer pre-division:

T2PT<2>	T2PT<1>	T2PT<0>	Frequency division coefficient
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit<3>-T2EN: indicates the T2 timer enable bit
1: indicates that the T2 timer is enabled
0: indicates that the T2 timer is disabled
Bit<4>:-PWMEN: indicates the PWM enable bit
1:PWM enable (P62 port output)
0: indicates that PWM is disabled

Bit<6:5>: not used, fixed to 0
Bit<7>-DB_EN: indicates PWM frequency doubling
1: Enables PWM frequency doubling
0:PWM frequency doubling is disabled

4.2.16 RF/INTFLAG (Interrupt Status Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	DTIF	PRDIF	E2PIF	T1F	EXIF	ICIF	TCIF

Bit<7> is fixed to 0
Bit<6>-DTIF: indicates the interrupt flag of the T2 timer duty cycle
T2 counts to set duty cycle 1, and the software clears 0
Bit<5>-PRDIF: indicates the interval interruption of the T2 timer.
T2 count to set period 1, software clear 0
Bit<4>-E2PIF: indicates the E2P write completion interrupt flag
E2P is written and set to 1, and the software clears 0
Bit<3>-T1F:T1 overflow interrupt flag;
T1 overflows 1, and the software clears 0
Bit<2>-EXIF: indicates the external interrupt flag
By the drop edge on the EXINT pin set 1, software clear 0
Bit<1>-ICIF:P6 input change interrupt flag;
P6 port input change set to 1, software clear 0
Bit<0>-TCIF:TCC overflow interrupt flag, TCC overflow set to 1, software clear 0
1: indicates an interrupt request
0: there is no interrupt request
INTFLAG can be set to 0 by software but not to 1 by software
Note: The result of reading INTFLAG is the result of matching INTFLAG and RIEN.

4.2.17 R10 to R3F general purpose registers

8-bit general purpose register, readable and writable.

4.3 IOPAGE register

4.3.1 ACC (Adder)

For internal data transfer, instruction operand is temporarily stored, this accumulator is not addressable.

4.3.2 CONT (Control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTCS	INT	TS	TE	PAB	PSR2	PSR1	PSR0

Bit<7> RTCS: When RTC is turned off in OPTION, as the universal read/write bit;
When RTC is enabled in OPTION:
1: Select the external crystal oscillator clock (LXT 4 frequency division)
0:TCC clock is determined by TS

Bit<6> INT: indicates the interrupt enable flag bit
0: masked by DISI instruction or hardware interrupt
1: Interrupt enabled by ENI/RETI directive

Bit<5> TS: indicates the TCC source selection bit
0: internal instruction cycle clock
1: external input signal (P62/TCC is set as input)

Bit<4> TE: edge selection bit of TCC signal
0:TCC pin signal changes from low to high plus 1
1:TCC pin signal changes from high to low plus 1

Bit<3> PAB: The pre-divider allocates bits
0:TCC
1:WDT

Bit<2:0> PSR2 ~ PSR0:TCC/WDT pre-division selection control bit:

PSR2	PSR1	PSR0	TCC frequency division coefficient	WDT frequency division coefficient
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

CONT is a readable and writable register

4.3.3 IOC5/P5CR (I/O control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	P5CR<3>	P5CR<2>	P5CR<1>	P5CR<0>

Bit<3:0>:P53-P50:

1: Define the corresponding I/O pin as a high-resistance input state

0: Define the corresponding I/O as output status

P5CR is a read-write register

4.3.4 IOC6/P6CR (I/O control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6CR<7>	P6CR<6>	P6CR<5>	P6CR<4>	P6CR<3>	P6CR<2>	P6CR<1>	P6CR<0>

Bit<7:0>:P67-P60:

1: Define the corresponding I/O pin as a high-resistance input state

0: Define the corresponding I/O as output status

P6CR is a read-write register

4.3.5 IOC7/PRD (PWM cycle register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD<7:0>							

Bit<7:0>: indicates the PWM cycle register

4.3.6 IOC8/DT (PWM Duty cycle register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT<7:0>							

Bit<7:0>: indicates the PWM duty cycle register

4.3.7 IOC9/PHDCR (pull down control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P6D<7>	P6D<6>	P6D<5>	P6D<4>	P5H<3>	P5H<2>	P5H<1>	P5H<0>

Bit7 P6D<7>: P67 pin pull-down enables the control bit

Bit6 P6D<6>: P66 pin pull-down enables the control bit

Bit5 P6D<5>: P65 pin pull-down enables the control bit

Bit4 P6D<4>: P64 pin pull-down enable control bit

Bit3 P5H<3>: P53 pin pull-up enable control bit

Bit2 P5H<2>: P52 pin pull-up enable control bit

Bit1 P5H<1>: P51 pin pull-up enable control bit

Bit0 P5H<0>: P50 pin pull-up enable control bit

0: Enable internal pull up and down

1: Internal pull up and down is forbidden

PHDCR is a read-write register

4.3.8 IOCB/PDCR (drop down control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	P6D<2>	P6D<1>	P6D<0>	P5D<3>	P5D<2>	P5D<1>	P5D<0>

Bit7: Fixed to 1
Bit6: P6D<2>: P62 pin pull-down enables the control bit
Bit5: P6D<1>: P61 pin pull-down enables the control bit
Bit4: P6D<0>: P60 pin pull-down enables the control bit
Bit3: P5D<3>: P53 pin pull-down enables the control bit
Bit2: P5D<2>: P52 pin pull-down enables the control bit
Bit1: P5D<1>: P51 pin pull-down enables the control bit
Bit0: P5D<0>: P50 pin pull-down enable control bit
0: Enable the internal drop-down function
1: Disable the internal drop-down
IOCB is a readable and writable register

4.3.9 IOCC/T2 (T2 timer)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2<7>	T2<6>	T2<5>	T2<4>	T2<3>	T2<2>	T2<1>	T2<0>

Bit<7:0>: indicates the T2 timer, read only

4.3.10 IOCD/PHCR (Pull-up control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH<7>	PH<6>	PH<5>	PH<4>	1	PH<2>	PH<1>	PH<0>

Bit7 PH<7>: P67 pin pull-up enables the control bit
Bit6 PH<6>: P66 pin pull-up enables the control bit
Bit5 PH<5>: P65 pin pull-up enables the control bit
Bit4 PH<4>: P64 pin pull-up enables the control bit
Bit2 PH<2>: P62 pin pull-up enables the control bit
Bit1 PH<1>: P61 pin pull-up enables the control bit
Bit0 PH<0>: P60 pin pull-up enables the control bit
0: internal pull up is enabled
1: Internal pull-up is forbidden
PHCR is a read-write register

4.3.11 IOCE/WDE (Watchdog Control Register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	1	1	1	1	1	1

Bit7 WDTE: Enables the control bit of the watchdog timer
0: The WDT is disabled

1:WDT is enabled

Bit6 EIS: P60 pin (INT) function control bit

0:P60, two-way I/O pin

1:INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit0 of P6CR) This parameter must be set to 1.

When the EIS is 0, the EXINT channel is masked. If it is "1", the status of the EXINT pin can be read by the P60 port.

Bit<5:0> Not used, fixed to 1

WDE is a read-write register

4.3.12 IOCF/RIEN (Interrupt enable register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIE	DTIE	PRDIE	E2PIE	T1IE	EXIE	ICIE	TCIE

Bit7: indicates the global interrupt enable flag bit

Bit6: DTIE: indicates the interrupt enable bit of PWM duty ratio

0: Disables PWM duty cycle interruption

1: indicates that PWM duty cycle interruption is enabled

Bit5: PRDIE: indicates the PWM period interrupt enable bit

0: Disables the PWM period interruption

1: indicates that PWM period interrupt is enabled

Bit4: E2PIE:E2P Write completion interrupt enable bit

0:E2P write interrupt is forbidden

1:E2P write interrupt is enabled

Bit3: T1IE:T1 interrupt enable bit

0:T1 interrupt disables

1:T1 interrupt is enabled

Bit2: EXIE: indicates the external interrupt enablement bit

0: Disable external interrupt

1: External interrupt is enabled

Bit1: ICIE:P6 input status change interrupt bit

0: indicates that the input status change of port P6 is interrupted

1: The interruption of P6 input status change is enabled

Bit0: TCIE:TMR interrupt enable bit

0:TMR interrupt is forbidden

1:TMR interrupt is enabled

RIEN is a read-write register

5 JZ8PE155E Main function modules

5.1 I/O Function

The JZ8PE155E has 2 sets of two-way I/O ports with 12 inputs and 11 outputs (the P63 can only output low levels).

11 programmable pull-up I/O pins :P5.0 ~ P5.3, P6.0 ~ P6.2, P6.4 ~ P6.7;

11 programmable pull-down I/O pins :P5.0 ~ P5.3, P6.0 ~ P6.2, P6.4 ~ P6.7;

The pull-up function of the P6.3 port is set by the pull-up OPTION of the reset port.

The leak-open output function of P6.3 port is set by using the GPIO port OPTION of P63 option.

5.1.1 Port Overview

The JZ8PE155E has 12 I/O ports. Input characteristics are optional (SMT /HSMT /INV /EMC, which can be configured according to port characteristics in OPTION). When used as an input port, the status change of each port can either form an interrupt or wake up the system. P6.0 port can also be used as an input port for external interrupts. When the P6.3 port serves as the input port, its pull-up function is set by using the reset port pull-up OPTION in Option.

Relevant register:

P5CR: P5 Port control register

P6CR: P6 Port control register

PDCR: Drop down the control register

PHCR: Pull up the control register

PHDCR: Pull down the control register

Description of port features

port	SMT	HSMT	EMC	INV
P5.0 to P5.3	VDD / 0.2 * 0.5 * VDD	VDD / 0.15 * 0.8 * VDD	VDD / 0.2 * 0.3 * VDD	0.48 * VDD
P6.0 to P6.2	VDD / 0.2 * 0.5 * VDD	VDD / 0.15 * 0.8 * VDD	VDD / 0.2 * 0.3 * VDD	0.48 * VDD
P6.3	0.48 * VDD	VDD / 0.15 * 0.8 * VDD	VDD / 0.2 * 0.3 * VDD	0.48 * VDD
P6.4 to P6.5	VDD / 0.2 * 0.5 * VDD	VDD / 0.15 * 0.8 * VDD	0.3 * VDD	0.42 * VDD
P6.6 to P6.7	VDD / 0.2 * 0.5 * VDD	VDD / 0.15 * 0.8 * VDD	VDD / 0.2 * 0.3 * VDD	0.46 * VDD

5.2 TCC/WDT and pre-divider

TCC is an 8-bit timing/counter register. The TCC clock source can be an internal clock or an external clock (input by the TCC pin, trigger edge optional). If it is an internal clock, each instruction cycle is TCC plus 1 (no pre-divider). Either CLK=Fosc/2 or CLK=Fosc/4 or CLK=Fosc/8 depends on the operation bit Tcpu of CONT. If Tcpu=2*Tosc, then CLK=Fosc/2; if Tcpu=4*Tosc, then CLK=Fosc/4. If the TCC source is from an external clock input, the falling or rising edge of the TCC pin triggers the TCC plus 1. If there is no frequency division control, each instruction cycle (select the internal clock) or each clock cycle (external clock), the counter implementation adds 1, count overflow can form interrupt signal. If the external clock is selected as the TCC clock source, the maximum frequency of the external clock cannot exceed one instruction cycle (without pre-frequency division). WDT is a 12-bit upstream counter with two enable control signal controls (WDT enable control in OPTION and WDTE control bits in the WDE register). The count clock is provided by a separate oscillator, so the WDT can still run (if enabled) after the system is in static mode, and an overflow of the WDT can wake/reset the system in either normal or sleep mode. It should be noted that WDT count overflow and WDT reset are two different concepts.

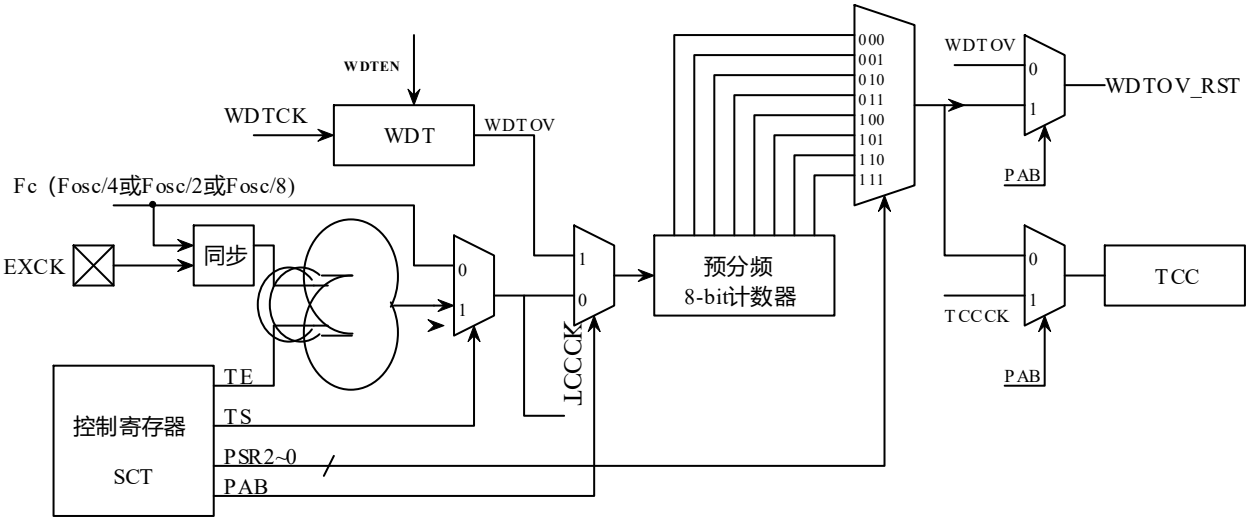
A WDT overflow is a 12-Bit counter overflow. Overflow signals can form interruptions or be used for sleep arousal.

WDT reset means that WDT count overflows after pre-division. At this time, the length of WDT counter may be 12 ~ 19-bit (specifically related to the setting of pre-division). WDT reset signal can make the system perform reset action.

From the structure of WDT and pre-division, WDT overflow may not cause system reset, but system reset must be caused by WDT overflow event.

Frequency divider: The system provides an 8-bit counter as the frequency divider of TCC/WDT, which can only be used as one of the frequency dividers of TCC or WDT at the same time. The choice can be realized through software, which is determined by the PAB bit of the CONT register. PSR0 ~ PSR2 digits determine the distribution coefficient. If assigned to TCC, the pre-divider will be cleared by 0 each time the TCC is written. If assigned to WDT, both WDT and the pre-divider clear 0 when executing the instructions WDTC and SLEEP. In use, it should be noted that after the divider is allocated, TCC will be assigned a value to ensure accurate timing.

The relationship between the three is shown in the figure below:



Relationship diagram of the three

Relevant register:
IOCE: Watchdog control register
CONT: control register

5.3 Sleep and wake up

5.3.1 Function Overview

The chip can switch to hibernation mode (low power mode) by executing "SLEEP" instruction. When you enter hibernation mode, the system clock stops, all modules stop working, and WDT (if enabled) clears 0, but continues to run. The microcontroller can be awakened by the following conditions:

(1) External reset signal input on the RST pin
(2) WDT reset (if enabled)
(3) Input state of P6 changes (if the setting is valid)
(4) TCC timer overflow (valid in RTC mode)

Relevant register:
INTFLAG: indicates the interrupt enable register
WUCON: Input state change interrupts the enable control register

5.3.2 Sleep and Wake Application Description

The first two awakenings make the system reset and terminate all the programs executed before sleep. The T and P flag bits of RCFG can be used to determine the reset source. The third and fourth awakening methods maintain the continuity of the program. You can programmatically choose to continue the process (DISI before SLEEP) or perform the corresponding jump (ENI before SLEEP, jump to interrupt vector (0X08). It is not recommended to use the P6 port to input the state change wake up and the TCC timer overflow wake up.

If you need to perform the wake-up mode of P6 input status change, you need to perform the following steps before entering the sleep mode:

1. Ensure that P6 port is input state;
2. Ensure that the WDT OPTION in Option is set to Enable;
3, software disable WDT (WDTE=0);
4, read P6 port (MOV PORT6,PORT6);
5. Set global interrupt enable signal (execute ENI/DISI instruction);
6. Open the interrupt enable signal (ICIE=1);
7, Turn on the secondary interrupt enable control signal (WUCON corresponding set to high level)
8. Enter SLEEP mode (Perform SLEEP)

After the above Settings, as long as the input status of port P6 changes, the system can be awakened. Note the following after awakening:

a. If ENI is executed before sleep, press PC on the stack before wake up and point PC to 0x08 after wake up. After the wake up subroutine finishes, continue the original process.

b. If DISI is executed before sleep, the PC continues the process before sleep after wake up.

c. WDT is automatically enabled after wake up. If WDT is not required, it should be disabled through software.

d. In order to avoid resetting when P6 input state change interrupts enter the interrupt vector or when it is used to wake up MCU, WDT frequency division coefficient >2(the maximum is recommended).

5.3.3 Wake Up Time

The system has multiple clock options. Considering the different clock performance, the wake-up time varies with the clock source to ensure that the system can work properly after waking up.

Wake up build time comparison table:

type	IRC mode	
	PWRT=140uS	PWRT=WDT
The RESET pin input is low	135us	18ms
WDT overflow	18ms* Frequency division coefficient +135us	18ms* frequency division coefficient +18ms
The input status of port P6 changes	135us	18ms
type	Crystal vibration mode	
	PWRT=140uS	PWRT=WDT
The RESET pin input is low	18ms	18ms
WDT overflow	18ms* frequency division coefficient +18ms	18ms* frequency division coefficient +18ms
The input status of port P6 changes	18ms	18ms
type	RTC mode	
	PWRT=140uS	PWRT=WDT
The RESET pin input is low	18ms	18ms
WDT overflow	18ms* frequency division coefficient +18ms	18ms* frequency division coefficient +18ms
The input status of port P6 changes	TCCWKEN=1 135us TCCWKEN=0 18ms	18ms
TCC wake up	135us	18ms

Description:

1, Including the internal oscillation mode;

2, Can be set to 4.5ms, 18ms, 72ms, 288ms by option-sut option;
3. Maximum time interval in RC mode;

5.4 Interrupt Function

5.4.1 Function Overview

JZ8PE155E has the following 7 interrupts:

(1) TCC overflow interrupted
(2) P6 port input status change interrupted
(3) External interrupt (when P60 is set to EXINT port, built-in pull-up will be shielded, if necessary, external pull-up resistor)
(4) T1 interrupt
(5) E2P write completion interrupt
(6) PWM cycle interruption
(7) The PWM duty cycle is interrupted

The JZ8PE155E chip has only one interrupt entry address :008H. There is no priority between interrupts.The hardware automatically disables global interrupt after the interrupt is entered and turns it on automatically when RETI exits the interrupt.After entering the interrupt, the program determines the interrupt type by the interrupt flag.

Relevant register:

RIEN: Interrupt enable register
INTFLAG: Interrupt status register
WUCON: Input state change interrupts enable control register

5.4.2 Register Description

IOCF/RIEN (interrupt enable register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIE	DTIE	PRDIE	E2PIE	T1IE	EXIE	ICIE	TCIE

Bit7: indicates the global interrupt enable flag bit
Bit6: DTIE: indicates the interrupt enable bit of PWM duty ratio
0: Disables PWM duty cycle interruption
1: indicates that PWM duty cycle interruption is enabled
Bit5: PRDIE: indicates the PWM period interrupt enable bit
0: Disables the PWM period interruption
1: indicates that PWM period interrupt is enabled
Bit4: E2PIE:E2P Write completion interrupt enable bit
0:E2P write interrupt is forbidden
1:E2P write interrupt is enabled
Bit3: T1IE:T1 interrupt enable bit
0:T1 interrupt disables
1:T1 interrupt is enabled
Bit2: EXIE: indicates the external interrupt enablement bit
0: Disable external interrupt
1: External interrupt is enabled

Bit1: ICIE:P6 input status change interrupt bit
0: indicates that the input status change of port P6 is interrupted
1: The interruption of P6 input status change is enabled
Bit0: TCIE:TMR interrupt enable bit
0:TMR interrupt is forbidden
1:TMR interrupt is enabled
RIEN is a read-write register

RD/WUCON (Input port status change interrupt enable control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUEN<7>	WUEN<6>	WUEN<5>	WUEN<4>	WUEN<3>	WUEN<2>	WUEN<1>	WUEN<0>

Bit7 WUEN<7>:P67 Input status change interrupt control bit
Bit6 WUEN<6>:P66 Input status change interrupt control bit
Bit5 WUEN<5>:P65 Input status change interrupt control bit
Bit4 WUEN<4>:P64 Input status change interrupt control bit
Bit3 WUEN<3>:P63 Input status change interrupt control bit
Bit2 WUEN<2>:P62 Input status change interrupt control bit
Bit1 WUEN<1>:P61 Input status change interrupt control bit
Bit0 WUEN<0>:P60 Input status change interrupt control bit
1: indicates that the function is enabled
0: Disable

Note: In OPTION, if port is not independent control, port wake-up is not controlled by the WUCON register. Otherwise, you need to process WUCON; otherwise, the port cannot be woken up.

RF/INTFLAG (Interrupt status register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	DTIF	PRDIF	E2PIF	T1F	EXIF	ICIF	TCIF

Bit<7> is fixed to 0
Bit<6>-DTIF: indicates the interrupt flag of the T2 timer duty cycle
T2 counts to set duty cycle 1, and the software clears 0
Bit<5>-PRDIF: indicates the interval interruption of the T2 timer.
T2 count to set period 1, software clear 0
Bit<4>-E2PIF: indicates the E2P write completion interrupt flag
E2P is written and set to 1, and the software clears 0
Bit<3>-T1F:T1 overflow interrupt flag;
T1 overflows 1, and the software clears 0
Bit<2>-EXIF: indicates the external interrupt flag
By the drop edge on the EXINT pin set 1, software clear 0
Bit<1>-ICIF:P6 input change interrupt flag;
P6 port input change set to 1, software clear 0
Bit<0>-TCIF:TCC overflow interrupt flag, TCC overflow set to 1, software clear 0
1: indicates an interrupt request
0: there is no interrupt request

INTFLAG can be set to 0 by software but not to 1 by software

Note: The result of reading INTFLAG is the result of matching INTFLAG and RIEN.

5.4.3 Application Description of the Interrupt Function

(1) Before performing the interrupt, be sure to turn on the enable signal of the corresponding interrupt type;

(2) If the interrupt jump needs to be executed, the ENI command should be executed before the interrupt; otherwise, the DISI command should be executed and the original process will continue after the interrupt is formed;

(3) When the external interrupt is executed, the external interrupt channel (ICIE=1) should be opened. At this time, the state of P6.0 port can still be read through the command. Only when there is a falling edge on P6.0 port, the interrupt will be formed;

(4) Before the P6 input change interrupt is enabled, it is necessary to read the P6 register (for example: "MOV P6, P6"). Every pin of port P6 can have this function, except the pin in output state and P6.0 as the /EXINT pin, if its state has changed. If the port P6 input state change interrupt is valid before the SLEEP instruction is executed to enter hibernation mode, the chip can be awakened from hibernation mode. Once the chip is woken up, the controller will continue to execute the next instruction when the global interrupt is disabled, and the controller will go to the interrupt vector 008H for execution when the global interrupt is valid.

(5) INTFLAG is an interrupt status register, which records the interrupt request of the corresponding flag bit. RIEN is the interrupt enable register. Overall interrupt enabling or disabling is done by ENI or DISI instructions. When an interrupt occurs, the next instruction is fetched from address 008H. Once in the interrupt service subroutine, you can detect the interrupt source by querying the INTFLAG bit. The interrupt flag bit must be cleared and the interrupt enabled before leaving the interrupt service subroutine to avoid repeated interrupts.

(6) Whether interrupts are allowed or not, the corresponding bit of the INTFLAG register is set by the interrupt. Note that the result of reading RF is the logic of INTFLAG and IOCINT. The RETI instruction terminates the interrupt subroutine and enables the overall interrupt (execution of ENI).

(7) When an INT instruction (if ENI is enabled) generates an interrupt, the next instruction is fetched from address 001H.

5.5 PWM pulse width modulation

5.5.1 Function Overview

JZ8PE155E has a built-in counter with a pre-divider, which is used to generate pulse width modulation signals. The PWM is 8Bit precision.The PWM output waveform is determined by the period and duty cycle factor.

5.5.2 Register Description

RE/T2CON (T2/PWM control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB_EN	-	-	PWMEN	T2EN	T2PT<2>	T2PT<1>	T2PT<0>

Bit<2:0>:T2 timer pre-division:

T2PT<2>	T2PT<1>	T2PT<0>	Frequency division coefficient
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit<3>:T2EN:T2 timer enable bit
1: T2 timer is enabled
0: T2 timer is disabled
Bit<4>:PWMEN: PWM enable bit
1: PWM enable (P62 port output)
0: PWM is disabled
Bit<7>:DB_EN:PWM frequency doubling
1: Enables PWM frequency doubling
0: PWM frequency doubling is disabled

IOC7/PRD (PWM cycle register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRD<7:0>							

Bit<7:0>: indicates the PWM cycle register

IOC8/DT (PWM duty cycle register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT<7:0>							

Bit<7:0>: indicates the PWM duty cycle register

5.6 Data EEPROM

5.6.1 Function Overview

JZ8PE155E integrates a 128-byte EEPROM for addressing access via E2PADR.E2PCON can be used to program EEPROM in software, and the self-timing function of erasing and programming is realized in hardware, without software query, saving code space. When the power supply voltage is less than 2.3v, data writing may fail. Therefore, ensure that the chip works above 2.3v and EEPROM can be used normally.

5.6.2 Register Description

R9/E2PADR (E2P address register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	E2PADR<6:0>						

Bit<6:0> :E2P address bit

Bit7: Not used, fixed to 0

RA/E2PDAT (E2P data register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E2PDAT<7:0>							

Bit<7:0>:E2P writes data bits

RB/E2PCON (E2P control register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E2PWKEN	-	-	-	E2PISAVB	E2PSTATIC	E2PRDEN	E2PWREN

Bit<0>:E2PWREN:

1:E2P write enable (self-defining 0 after E2P write is completed, write operation will continue to be completed directly when sleeping)

0: The E2P write is complete/The E2P write is closed (if the 0 is not automatically cleared for a long time, the write fails and the software needs to clear the 0.)

Bit<1>:E2PRDEN:

1:E2P read enable (Enable E2P, wait for one instruction cycle to start reading E2P (MOV A, 0x0C) valid, continuous read, disable read after reading the required data)

0:E2P read is forbidden

Bit<3:2>:E2P reads the speed control bit

11: High speed mode (reading speed 4MHz)

00: Energy saving mode (reading speed <500KHz)

Bit<6:4>: not used, fixed to 0

Bit<7>:E2PWKEN:E2P wake up enable bit

1:E2P wake up enable (wake up sleep mode after E2P is written)
0:E2P wakes up forbid

RC/E2PREAD (E2P read data register)

Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E2PREAD<7:0>							

Bit<7:0>:E2P reads the data bit

5.6.3 EEPROM Application Description

5.6.3.1 Reading Data

(1) Set the E2PCON register;
(2) Set the address to be read to E2PADR;
(3) Set the enable flag bit E2PRDEN;
(4) Read the value of E2PREAD;
(5) Clear the read enable flag bit E2PRDEN;

5.6.3.2 Data Write Operations

(1) Set the E2PCON register;
(2) Set the address to be written to E2PADR;
(3) The value to be written is assigned to E2PDAT;
(4) Write enable flag bit E2PWREN;
(5) After the write is completed, the write enable flag bit is automatically cleared;

5.7 Reset Function

5.7.1 Function Overview

The reset is caused by:

(1) Power-on reset

(2) Reset pin input as "low"

(3) WDT reset (if enabled)

After the effective reset is detected, the system enters the reset establishment state, including the reset register, the OPTION preset value is loaded, and the oscillator oscillator is set up. If the influence of the oscillator oscillator is not considered, the reset establishment time of the system is determined by the option-SUT bit, and the user can make corresponding configuration according to the needs. For the oscillation mode with short starting time, such as IRC, a shorter reset setting time, such as 18ms, can be considered. For an oscillation mode with a longer starting time, a longer setting up time can be considered.

Reset time:

The reset time of the last three reset modes has been given in the wake up section. The reset time of the first reset mode is determined by SUT selection in OPTION, as shown in the following table:

Power-on reset establishment time

Reset setup time	
SUT	PWRT=WDT= 18ms
	PWRT = WDT = 4.5 ms
	PWRT=WDT= 288ms
	PWRT=WDT= 72ms

5.8 Clock Module

The JZ8PE155E provides three oscillation modes, which can be configured by OPTION. See the table below for details:

Type of oscillator	note
IRC (built-in RC oscillator)	The RCM can be used to select 1M, 4M, 8M, or 455K
HXT (High speed crystal oscillator)	1M/4M/8M/16M
LXT (Low speed crystal oscillator)	32.768K.

Internal RC oscillator mode:

The JZ8PE155E provides internal RC mode with a frequency of 4MHz by default. The internal RC oscillation mode also has other frequency values such as 8MHz, 1MHz and 455KHz. IRC operating frequency can be selected by setting the frequency selection bit of OPTION. Their corresponding relationship is as follows:

Firc	IRC frequency
455 K	The IRC frequency was selected as 455KHz
1 M	The IRC frequency is set to 1MHz
4 M	The IRC frequency was set to 4MHz
8 M	The IRC frequency was set to 8MHz

The IRC frequency can be automatically corrected by the burner, with a theoretical correction accuracy of ±1%.

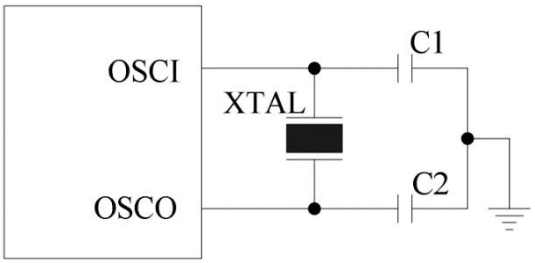
IRC frequency drift (Ta=25℃, VDD=5V±5%, GND=0V)				
IRC	Rate of drift			
	Temperature (-40℃ ~ +85℃)	Voltage (1.8V ~ 5.5V)	process	Total
4MHz	Plus or minus 5%	Plus or minus 5%	±1%	±11%
8MHz	Plus or minus 5%	Plus or minus 5%	±1%	±11%
1MHz	Plus or minus 5%	Plus or minus 5%	±1%	±11%
455KHz	Plus or minus 5%	Plus or minus 5%	±1%	±11%

JZ8PE155E provides a variety of frequency division options, can be selected in the OPTION, suitable for more occasions. The following table:

Clocks	Clocks frequency division
2clock	The frequency division is 2clock
4clock	The frequency division is 4clock
8clock	The frequency division is 8clock
16clock	The frequency division is 16clock

External crystal oscillator:

In most applications, pin OSCO and OSCI can be connected to a crystal oscillator to generate oscillations. The circuit diagram below applies to both HXT and LXT modes. The recommended values for C1 and C2 are shown in the table. Due to the different characteristics of each resonator, users should refer to its specifications to select the appropriate values of C1 and C2.



Crystal oscillator circuit

Reference for capacitor selection of crystal oscillator:

Mode of oscillator	Mode of frequency	frequency	C1(pF)	C2(pF)
Crystal oscillator	LXT	32.768 KHz	15 to 25	15 to 25
	HXT	1 MHz	15	15
		4 MHz	20	20

Note: The above data is for reference only, all subject to the actual test.

Application description of clock module:

(1) Internal oscillator is the most commonly used oscillation mode, which can omit the external circuit;

(2) With different external conditions, the clock frequency of each oscillation mode may be slightly different, so reasonable selection should be made according to the needs.

6 Code options register

Code Option	options	Function Description
Watch dog	Enable	The WDT function was enabled
	Disable	The WDT function is disabled
Clocks Frequency division	2*Clocks	2 oscillating clocks as one machine cycle
	4*Clocks	4 oscillating clocks as one machine cycle
	8*Clocks	8 oscillating clocks as one machine cycle
	16*Clocks	16 oscillating clocks as one machine cycle
Mode of oscillation	IRC	The oscillation mode is selected as the internal RC oscillator
	HXT	The oscillation mode is selected as high speed crystal oscillator
	LXT	The oscillating mode is selected as low speed crystal oscillator
IRC frequency	455 K	The IRC frequency was selected as 455KHz
	1 M	The IRC frequency is set to 1MHz
	4 M	The IRC frequency was set to 4MHz
	8 M	The IRC frequency was set to 8MHz
P64 Ports	GPIO	P6.4 serves as a general I/O port
	OSCO	P6.4 serves as the output of the system machine clock
Low pressure reduction	ban	No low pressure reset
	1.2 V	Select 1.2V for low voltage reset point
	1.5 V	The low voltage reset point is 1.5V
	1.7 V	The low voltage reset point is 1.7V
	2.2 V	The low voltage reset point is 2.2V
	2.5 V	The low voltage reset point is 2.5V
	3.0 V	The low voltage reset point is 3.0V
	3.3 V	The low voltage reset point is 3.3V
	3.6 V	The low voltage reset point is 3.6V
Encryption of code	Enable	Encryption of program
	Disable	The program is not encrypted
Reset port On the pull	Enable	P6.3 Pull-up was enabled
	Disable	P6.3 Pull-up was disable
P63 Port	RST	P6.3 as reset
	GPI	P6.3 as general input
	GPIO	P6.3 as general IO port
SUT	PWRT = WDT = 4.5 ms	Wake up time =WDT overflow time (regardless of frequency) = 4.5ms
	PWRT=WDT=18ms	Wake up time =WDT overflow time (regardless of frequency) = 18ms

	PWRT=WDT=72ms	Wake up time =WDT overflow time = 72ms
	PWRT=WDT=288ms	Wake up time =WDT overflow time = 288ms
	PWRT=140us WDT = 4.5 ms	Wake up setup time =140us WDT overflow time =4.5ms
	PWRT=140us WDT=18ms	Wake up setup time =140us WDT overflow time =18ms
	PWRT=140us WDT=72ms	Wake up setup time =140us WDT overflow time =72ms
	PWRT=140us WDT=288ms	Wake up setup time =140us WDT overflow time =288ms
Scope of table lookup	1/4K	The value ranges from 0 to 256
	1K	The value ranges from 0 to 1024
Port Features	EMC	The I/O port input feature is set to EMC
	SMT	The I/O port input feature is SMT
	INV	Set the I/O port input feature to INV
	HSMT	Set the I/O port input feature to HSMT
Drive enhancement	Enable	Enhanced port driver capability enabled
	Disable	The port driver capability is enhanced
POWER	HIGH	IRC is calibrated at VDD=5V
	LOW	IRC was calibrated at VDD=3V
Port P6 wakes up	Independent control	P6 port input status change Interrupt/wake up function is controlled by the WUCON register
	Non independent control	P6 All ports have the interrupt/wake up function for port input status changes
RTC	Enable	The RTC is enabled
	Disable	RTC Prohibition
P5, P6 Pull down control	Disable	P53 drop-down, P5 drop-down, P64-P67 drop-down invalid
	Enable	P53 drop-down, P5 drop-down, P64-P67 drop-down The software Settings are valid
E2P write current control	15mA, 1.5ms	E2P write current 15mA time 1.5ms
	30mA, 0.75ms	E2P write current 30mA time 0.75ms

Note :SUT contains 3 times in total:
1) PWRT:port wake, reset wake Set time
2) WDT:wdt overflow(no prescale) WDT has no overflow time
3) Power up setup time 3) Power up setup time
Where, power-on reset establishment time = WDT regardless of frequency overflow time;

7 JZ8PE155E Performance parameters

Note: The following performance parameters are measured, for reference only!

7.1 Limit Parameters

Operating temperature (℃)	(√) E:-40 ~ 85;	() R:-55 ~ 85;	() M:-55 ~ 125;
Storage temperature (° C)	() -55 to +125	() -40 to +125	(√) -65 to +150
Operating voltage (V)	() -0.3 ~ 15;	(√) Other 1.8 ~ 5.5	
Limit input voltage (V)	() GND-0.3 ~ VDD+0.3;	(√) Other GND-0.3 ~ VDD+0.5;	
Limit output voltage (V)	() GND-0.3 ~ VDD+0.3;	(√) Other GND-0.3 ~ VDD+0.5;	

7.2 DC Parameters

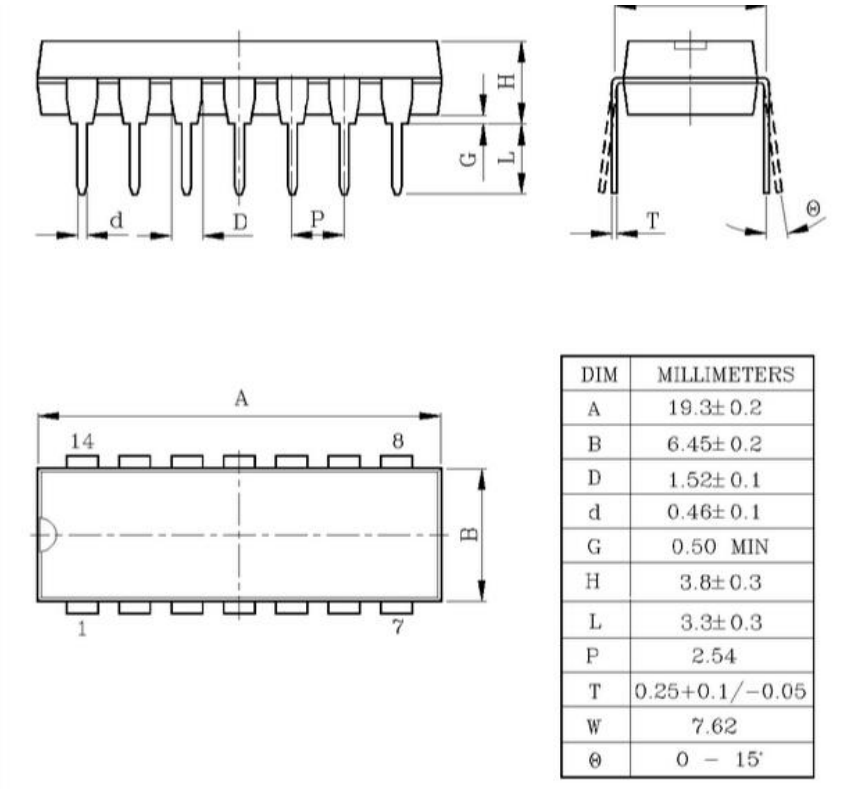
(T=25℃, VDD=5±5%V,GND=0V)

symbol	Parameter Description	conditions	The minimum	A typical	The biggest	unit
IRC1	Built-in resistance-volume oscillation 1 (After correction)	Firc0:Firc1=1:1	0.95 * 4	4	1.05 * 4	MHz
IRC2	Built-in resistance-volume oscillation 2 (After correction)	Firc0:Firc1=1:0	0.95 * 8	8	1.05 * 8	MHz
IRC3	Built-in resistance and volume oscillation 3 (After correction)	Firc0:Firc1=0:1	0.95 * 1	1	1.05 * 1	MHz
IRC4	Built-in resistance and volume oscillation 4 (After correction)	Firc0:Firc1=0:0	0.95 * 455	455	1.05 * 455	KHz

IOH1	Output high level drive (except P63)	IOH = 4.6 V	4	5	12 (Enhanced)	mA
IOL1	I/O output low level drive	IOL = 0.6 V	18	20	30 (Enhanced)	mA
IPH	Pull up current	The pull-up function is enabled and the input is grounded	65	100	105	uA
IPL	Pull down current	Pull down Enable and enter VDD	45	55	52	uA
Isb1	Standby current 1	Regular sleep		0.5	1	uA
Isb2	Standby current 2	The watchdog awakens sleep		7	10	uA
Isb3	Standby current 3	RTC sleep		10	15	uA
Iop1	Current of operation	System clock 4MHz, 2clks, The output terminal is suspended, the input is connected to VDD, and the high power mode is selected		0.5	1	mA
LVR1	Low voltage reset voltage 1	Select the 1.8V reset point	1.6	1.8	2	V
LVR2	Low voltage reset voltage 2	Select the 1.6V reset point	1.4	1.6	1.8	V

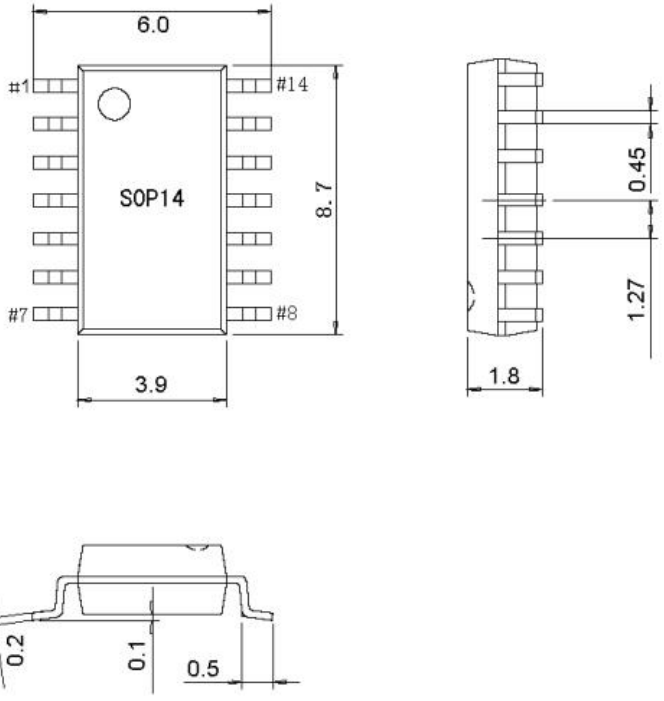
8 Package size information

8.1 14PIN package dimensions



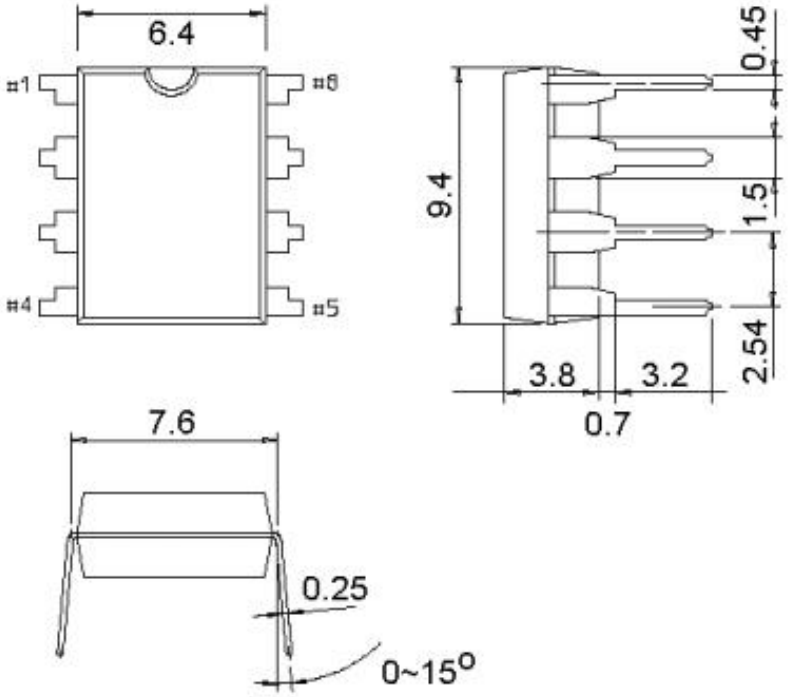
DIM	MILLIMETERS
A	19.3±0.2
B	6.45±0.2
D	1.52±0.1
d	0.46±0.1
G	0.50 MIN
H	3.8±0.3
L	3.3±0.3
P	2.54
T	0.25+0.1/−0.05
W	7.62
Θ	0 ~ 15°

DIP14 package size

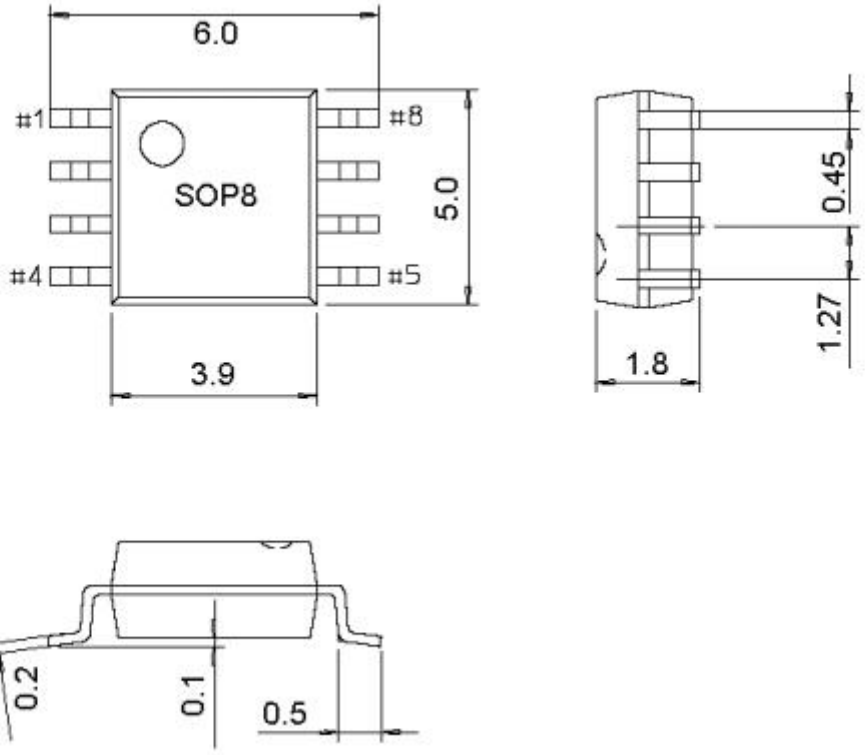


SOP14 package size

8.2 8PIN package size



DIP8 package size



SOP8 package size