JZ8PE255E
Product Specification

8-bit OTP + EEPROM Microcontroller with OTP ROM

Ver 1.0

Specification Revision History

Version	Revision Description	Remarks
V1.0	Initial version	

Note:

1, When the TC0CON register bit.3 (PAB) predivision Bit and bit.2 ~ 0(TC0PSR2 ~ PSR0) division Bit are in the switching state。 you need to turn off the watchdog enable first, and then turn on the watchdog enable after the switching is completed, otherwise it is easy to cause reset.

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1 General Description

1.1 Features

CPU Configuration

- 2K×14-Bit OTP ROM
- 80×8-Bit SRAM
- 64×8-Bit EEPROM (more than 10,000 erasures)
- 8-level stack space
- 8-stage Programmable voltage reset (LVR)
  1.2V, 1.6V, 1.8V, 2.4V
  2.7V, 3.3V, 3.6V, 3.9V
- Operating current less than 2mA(4MHz/5V)
- Operating current less than 5μA (14KHz/5V)
- Sleep current less than 1μA(sleep mode)

I/O port configuration

- 1 set of 6 GPIO ports: P6<5:0>
- 6 programmable pull-up I/O pins
- 6 programmable pull-down I/O pins
- 6 programmable wake-up ports: P6<5:0>
- 6 configurable drivers enhance P6<5:0>
- 3configurable secondary filling current enhancement P6<2:0>
- External interrupt: P60

Operating voltage

- Operating voltage range:

$V_{LVR3.9V \sim 5.5V}$|Fcpu=0 ~ 8MHz

$V_{LVR2.4V \sim 5.5V}$|Fcpu=0 ~ 4MHz

$V_{LVR1.8V \sim 5.5V}$|Fcpu=0 ~ 1MHz

Operating temperature

- Operating temperature range:
  -40 ℃ -- 85 ℃

Operating frequency range

- External crystal oscillator HXT, LXT
- Internal capacitance of external crystal oscillator:Disable, 7PF, 9PF, 12.5PF
- Built-in IHRC oscillator circuit:
  8MHz/1MHz/910KHz
- Instruction clock frequency division selection:
  2Clock, 4Clock, 8Clock,16Clock, 32Clock
- Built-in ILRC oscillating circuit:
  14KHz(5V)/8KHz(3V)

Peripheral modules

- 8Bit real-time clock/counter
- 3-channel common-period 8Bit pulse width modulator PWM

Interruption Source

- External interrupts
- TC0 overflow interrupt
- TC1 overflow /PWM cycle overflow interrupt
- E2P write completion interrupt
- Port status change interrupt

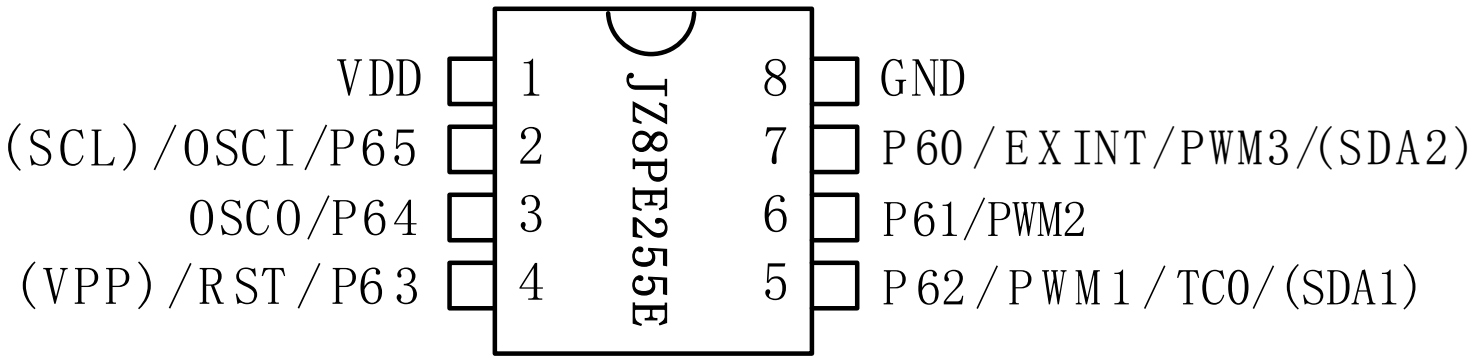
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- Four modes of operation
- Programmable WDT timer
- RTC clock count
- OTP can do 1K burn twice

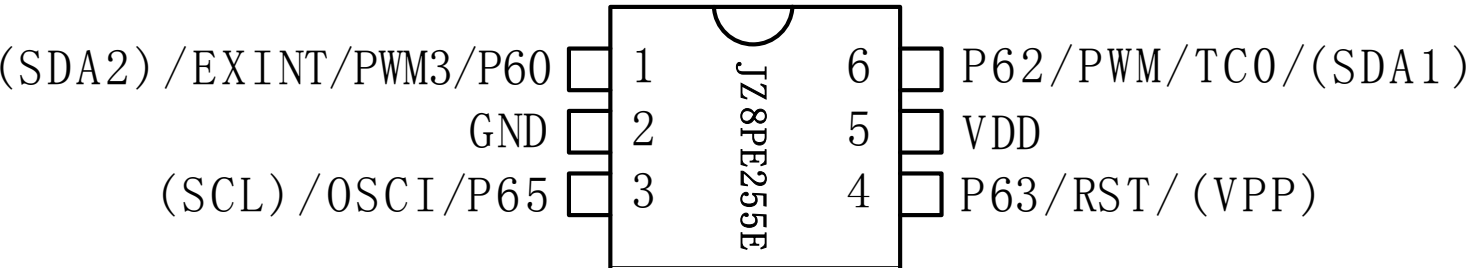
Type of package

- JZ8PE255E-DIP/SOP8
- JZ8PE255E-SOT23-6

1.2 Pin Assignment



JZ8PE255E-8PIN MAP

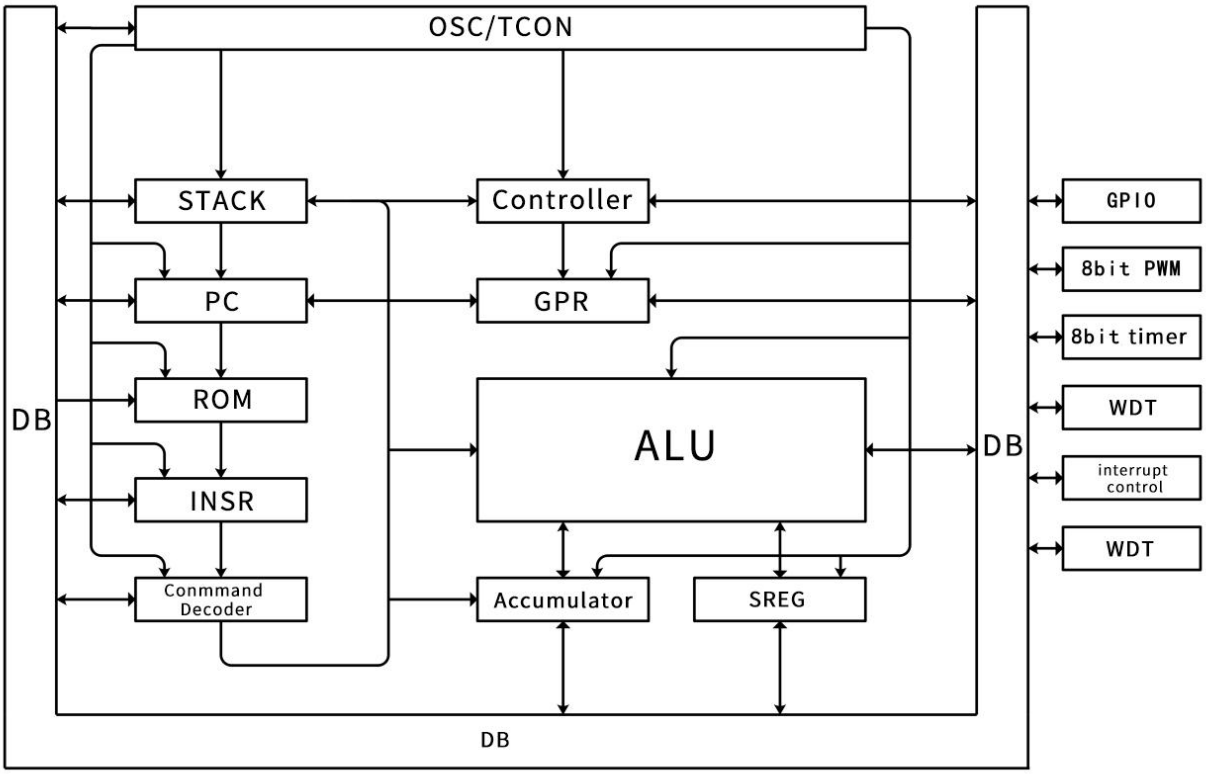


JZ8PE255E-6PIN MAP

1.3 Pin Description

NUM	NAME	I/O	Description
P60	P60	I/O	GPIO, programmable pull up and down, pull fill current enhancement, secondary fill current enhancement, port wake up
	EXINT	I	External interrupt input port
	PWM3	O	PWM3 output
	SDA2	I	Burn data port
P61	P61	I/O	GPIO, programmable pull up and down, pull perfusion current enhancement, secondary perfusion current enhancement, port wake-up
	PWM2	O	PWM2 output
P62	P62	I/O	GPIO, programmable pull up and down, pull fill current enhancement, secondary fill current enhancement, port wake up
	PWM1	O	PWM1 Output
	TC0	I	TC0 External count clock input port
	SDA1	I	Burn data port
P63	P63	I/O	GPIO, programmable pull up and down, perfusion current enhancement, port wake up
	RST	I	External reset port
	VPP	I	Burn the high pressure port
P64	P64	I/O	GPIO, programmable pull up and down, pull fill current enhancement, port wake up
	OSCO	O	Crystal oscillator pins
P65	P65	I/O	GPIO, programmable pull up and down, pull fill current enhancement, port wake up
	OSCI	I	Crystal oscillator pins
	SCL	I	Burn clock port
	VDD	--	ADD
	VSS	--	GND

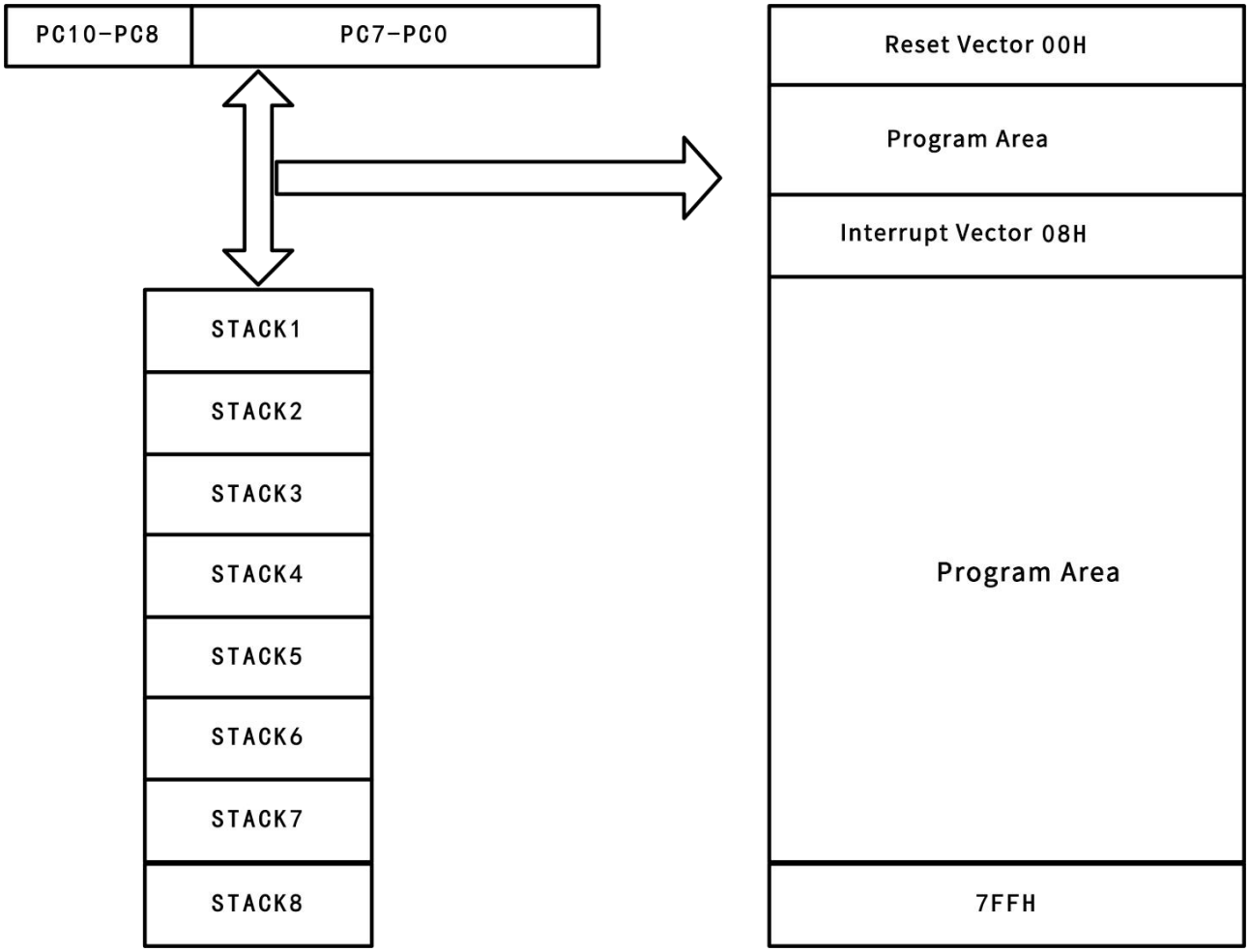
1.4 System block diagram



System circuit block diagram

2. Memory structure

2.1 Program Memory Area



Program memory area structure

2.2 Data Memory Area

Addresses	Register
0x00	R0/IAR (indirectly addressed register)
0x01	R1/TC0C (TC0 count register)
0x02	R2/PCL (PC low address register)
0x03	R3/STATUS (Status flag register)
0x04	R4/RSR (RAM address selector register)
0x05	Reserved
0x06	R6/P6 (P6 data register)
0x07	Reserved
0x08	R8/TC1CON(TC1 control register)
0x09	R9/TC1PRD (TC1 cycle register)
0x0A	RA/PWM1DT (PWM1 Duty cycle register)
0x0B	RB/PWM2DT (PWM2 duty cycle register)
0x0C	RC/PWM3DT (PWM3 Duty cycle register)
0x0D	RD/P6IWE (P6 State Change Wake up Interrupt Register)
0x0E	RE/CPUCON(CPU Mode control Register)
0x0F	RF/INTF (Interrupt flag register)
0x10 ~ 0x5F	**General register area**
0x70	Reserved
0x71	Reserved
0x72	R72/P6PH (P6 pull-up control register)
0x73	R73/P6PD (P6 pull-down control register)
0x74	Reserved
0x75	Reserved
0x76	R76/P6CON (P6 Direction Control Register)
0x77	Reserved
0x78	R78/E2PADR (E2P address register)
0x79	R79/E2PDAT (E2P write data register)
0x7A	R7A/E2PCON (E2P control register)
0x7B	R7B/E2PREAD (E2P read data register)
0x7C	Reserved
0x7D	R7D/TC0CON (TC0 control register)
0x7E	R7E/ SYSCON (System control Register)
0x7F	R7F/INTE (Interrupt enable register)

3. Function description

3.1 Operation Register

3.1.1 RPAGE ~ R0/IAR (Indirectly-Addressed Registers)

00H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
IAR	RIND<7:0>							
Read/Write	R							
Reset value	X							

R0 is not a physically implemented register. It is used as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the low 6-bit RAMS<5:0> of RAM Select Register (R4).

3.1.2 RPAGE ~ R1/TC0C(TC0 count register)

01H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
TC0C(R)	TC0C<7>	TC0C<6>	TC0C<5>	TC0C<4>	TC0C<3>	TC0C<2>	TC0C<1>	TC0C<0>
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

TC0 is an 8Bit upstream counter, clock source optional internal clock/external clock, count overflow can form interrupt, TC0C can be read and written.

The TC0 can be triggered by a signal edge on the P62 pin or an internal instruction cycle to produce a plus-1 operation (cont.4-bit definition). If the PAB bit is cleared (CONT.3), there is a pre-divider assigned to TC0, and when a value is written to the TC0C register, the value of the pre-divider is cleared to 0.

3.1.3 RPAGE ~ R2/PCL(PC low address register)

02H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
PCL	PC<7>	PC<6>	PC<5>	PC<4>	PC<3>	PC<2>	PC<1>	PC<0>
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

The program counter (PC) is a pointer that records the instructions that the CPU is going to process in each instruction cycle. During the CPU cycle, the PC pushes the instruction pointer into the program memory, and the pointer increses by 1 to enter the next cycle. The JZ8PE255E has an 11-bit-wide program counter (PC), with the low bytes coming from the read-write PCL and the high bits (PC<10:8>) unreadable.

The stack is used to record the instruction pointer returned by the program. When the subroutine is called, the PC presses the instruction pointer onto the stack. When the return instruction is executed, the stack sends the instruction pointer back to the PC to continue the original process. The JZ8PE255E has an 8-level stack that takes up neither program storage nor data storage, and the stack pointer cannot be read or written.

(1) Register PC and built-in 8-level stack are both 11 bits wide for addressing 2K×14Bit ROM, JZ8PE255E program storage area mapping.

(2) In general, PC self-increment one; On reset, all bits of the PC are cleared to zero.

(3) The instruction "JMP" allows the low 11 bit address to be loaded directly, so the JMP instruction can realize any position jump within the current page (within 2K range). Instruction "JMP" directly load the low 11 bit address, at the same time the PC +1 press stack, the subroutine entry address as long as in the same page can be accurately positioned.

(4) When executing "RET" instruction, the top data of the stack is sent to the PC.

(5) Any instruction that overwrites the PCL value will affect the PC's highest three digits accordingly. Thus, the resulting jump can be extended to the 2K range.

(6) When an interrupt occurs, the value of the program counter will change, and the PC will be assigned 0x08.

(7) The stack works like a cyclic buffer, that is, after pressing the stack 8 times, the data pushed in the 9th push will overwrite the data pushed in the 1st push, and the data pushed in the 10th push will overwrite the data pushed in the 2nd push, and so on.

3.1.4 RPAGE ~ R3/STATUS(status register)

03H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
STATUS	RST	GB1	GB0	T	P	Z	DC	C
Read/Write	R	R/W	R/W	R	R	R/W	R/W	R/W
Reset value	0	0	0	1	1	X	X	X

Bit<7> : RST- Reset type flag bit

0: Other reset type

1: If sleep mode is awakened by pin state change

Bit<6> : GB1- Undefined, universal read/write bit

Bit<5> : GB0- undefined, common read/write bit

Bit<4> : T- Time overflow bit

0: WDT overflow

1: Perform the "SLEEP" and "CWDT" instructions or low voltage reset

Bit<3> : P- Power failure flag bit

0: Execute the "SLEEP" command

1: Power-on reset or execute the CWDT command

The events that affect T/P are shown in the following table:

Types	RST	T	P
Power-on reset	0	1	1
Press RESET in working mode	0	Hold	Hold
RESET Wake up	0	1	0
WDT overflow in working mode	0	0	Hold
WDT overflow Wake up	0	0	0
Port status changes wake up	1	1	0
Execute CWDT instructions	Hold	1	1
Executing SLEEP instructions	Hold	1	0

Bit<2> : Z-zero flag bit set to "1" when the result of an arithmetic or logical operation is zero

0: when the result of an arithmetic or logical operation is not zero

1: When the result of an arithmetic or logical operation is 0

Bit<1> : DC- auxiliary carry flag

0: No carry is generated in the lower four digits during the addition operation. / When subtraction is performed, the lower four digits produce a borrow

1: When performing the addition operation, the lower four digits are generated by a carry; / When the subtraction operation is performed, the lower four digits do not produce a borrow

Bit<0> : c-carry flag

0: When performing the addition operation, no carry is generated for the higher four digits; / When subtraction is performed, the higher four digits produce a borrow

1: When performing the addition operation, the higher four digits have a carry generation; / When performing subtraction, the higher four digits produce no borrows

3.1.5 RPAGE ~ R4/RSR(RAM address selection register)

04H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
RSR	-	RSR<6>	RSR<5>	RSR<4>	RSR<3>	RSR<2>	RSR<1>	RSR<0>

Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	X	X	X	X	X	X	X

RSR<6:0> is used to select the RAM register address in indirect addressing mode (addressing range: 0x10 ~ 0x5F)

RSR is used in conjunction with R0 for indirect addressing operations. The user can put the address of a register into the RSR, and then access the indirect register R0, which will point to the register of the corresponding address in the RSR.

3.1.6 RPAGE ~ R6/P6(P6 Data Register)

06H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
P6	-	-	P65	P64	P63	P62	P61	P60
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	1	1	1	1	1

Port data register, P6 port is 6 bits

3.1.7 RPAGE ~ R8/TC1CON(TC1 control register)

08H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
TC1CON	TC1EN	PWM3EN	PWM2EN	PWM1EN	TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7> : TC1EN-TC1 /PWM counter Enable control

1: Enable

0: Disable

If the TC1PRD register is set, TC1 counts to the TC1PRD preset reset, and TC1 counts from 1.

Bit<6:4> : PWM3EN ~ PWM1EN-PWM3 ~ PWM1 Enables the control bit

1: Enable (PWM3(P60), PWM2(P61), PWM1(P62), corresponding port set to output)

0: Disable

Bit<3> : TC1PTEN-TC1 Pre-split selection control bit

Bit<2:0> : TC1PSR2 ~ TC1PSR1 frequency division selection bit:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	Frequency division ratio
0	0	0	0	1:1

1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.8 RPAGE ~ R9/TC1PRD(TC1 cycle register)

09H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
TC1PRD	TC1PRD <7>	TC1PRD <6>	TC1PRD <5>	TC1PRD <4>	TC1PRD <3>	TC1PRD <2>	TC1PRD <1>	TC1PRD <0>
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : TC1PRD<7:0>-PWM period 8-bit data

3.1.9 RPAGE ~ RA/PWM1DT(PWM1 Duty cycle register)

0AH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
PWM1DT	PWM1DT <7>	PWM1DT <6>	PWM1DT <5>	PWM1DT <4>	PWM1DT <3>	PWM1DT <2>	PWM1DT <1>	PWM1DT <0>
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWM1DT <7:0>-PWM1 Duty cycle Indicates 8-bit data

3.1.10 RPAGE ~ RB/PWM2DT (PWM2 duty cycle register)

0BH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
PWM2DT	PWM2DT <7>	PWM2DT <6>	PWM2DT <5>	PWM2DT <4>	PWM2DT <3>	PWM2DT <2>	PWM2DT <1>	PWM2DT <0>

Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWM2DT<7:0>-PWM2 Duty cycle 8-bit data

3.1.11 RPAGE ~ RC/PWM3DT (PWM3 Duty cycle register)

0CH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
PWM3DT	PWM3DT < 7 >	PWM3DT < 6 >	PWM3DT < 5 >	PWM3DT < 4 >	PWM3D < 3 >	PWM3DT < 2 >	PWM3DT < 1 >	PWM3DT < 0 >
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : PWM3DT<7:0>-PWM3 Duty cycle 8-bit data

3.1.12 RPAGE ~ RD/P6IWE(P6 input Change Interrupt, Wake up enable register)

0DH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
P6IWE	-	-	P6IWE < 5 >	P6IWE < 4 >	P6IWE < 3 >	P6IWE < 2 >	P6IWE < 1 >	P6IWE < 0 >
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<5:0> : P6IWE<5:0> -P6 Input change interrupt, wake up enable control bit

1: Enable

0: Disable

3.1.13 RPAGE ~ RE/CPUCON(CPU Mode control Register)

0EH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
CPUCON	CRYCAP<1>	CRYCAP<0>	TC0CKS	TC1CKS	IPWM1EN	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value	X	X	0	0	0	0	0	0

Bit<7:6> : CRYCAP<1:0>- crystal capacitance selection bit

CRYCAP<1>	CRYCAP<0>	Crystal capacitor
0	0	Crystal capacitor 12Pf
0	1	Crystal capacitor 9Pf
1	0	Crystal capacitor 7Pf
1	1	Forbidden

Bit<5>：TC0CKS-TC0 Clock source selection bit

1: Select System clock/Low speed clock

0: Select Instruction Cycle Clock/External input Clock

Bit<4>：TC1CKS-TC1/PWM Clock source selection bit

1: Select the system clock

0: Select instruction cycle clock

Bit<3> : IPWM1EN-PWM1 dead zone Complementary output enable bit

1: Enable dead zone complementary output (PWM1-P62/IPWM1-P61)

0: Disable dead zone complementary output

Bit<2>：STPHX-High speed clock control bit

1: Stop high speed clock, including IRC and crystal oscillator clock (excluding RTC clock)

0: The high speed clock is working properly

Bit<1>：CLKMD-System clock selection bit

1: The system clock uses a low speed RC oscillator clock

0: The system clock uses a high speed IRC or crystal oscillator clock

When the system enters the low speed mode from the high speed mode, set CLKMD=1 first, then set STPHX=1;

When the system enters high-speed mode from low-speed mode, set STPHX=0 first, and then set CLKMD=0.

Bit<0>：IDLE-Idle mode select bit

1: The system enters idle mode when the SLEEP command is executed, and the system clock works properly

0: The system enters the SLEEP mode when the sleep command is executed

3.1.14 RPAGE ~ RF/INTF(Interrupt flag Register)

0FH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
INTF	-	-	-	E2PIF	TC1IF	EXIF	P6ICIF	TC0IF
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W

Reset value	0	0	0	0	0	0	0	0

Bit<7:5> : unused bit

Bit<4> : E2PIF-EEPROM write complete interrupt flag

Bit<3> : TC1IF-TC1 Timing overflow /PWM period overflow interrupt flag bit

Bit<2> : EXIF- external port interrupt flag bit

Bit<1> : indicates the P6ICIF-P6 port status change interrupt flag bit

Bit<0> : TC0IF-TC0 Timing overflow interrupt flag bit

1: there is an interrupt, and the software clears 0

0: no interruption

Note: When clearing interrupt flag bits, you must use MOV RF,A operation, cannot use BTC AND AND RF,A instruction operation.

3.1.15 RPAGE ~ R72/P6PH (P6 pull-up control register)

72H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
P6PH	-	-	P6PH<5>	P6PH<4>	P6PH<3>	P6PH<2>	P6PH<1>	P6PH<0>
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit<5:0> : P6PH<5:0>-P6 Enable pull-up

0: Enable

1: Disable

3.1.16 RPAGE ~ R73/P6PD (P6 pull-down control register)

73H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
P6PD	-	-	P6PD<5>	P6PD<4>	P6PD<3>	P6PD<2>	P6PD<1>	P6PD<0>
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit<5:0> : P6PD<5:0> Drop down enable control

0: Enable

1: Disable

3.1.17 RPAGE ~ R76/P6CON(P6 Direction Control Register)

76H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
P6CON	-	-	P6CON < 5 >	P6CON < 4 >	P6CON < 3 >	P6CON < 2 >	P6CON < 1 >	P6CON < 0 >

Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	1	1	1	1	1	1	1

Bit<5:0> : P6CON<5:0>- P6 direction control bit

1: Input

0: Output

3.1.18 RPAGE ~ R78/E2PADR (E2P address register)

78H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
E2PADR	-	-	E2PADR<5>	E2PADR<4>	E2PADR<3>	E2PADR<2>	E2PADR<1>	E2PADR<0>
Read/write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<5:0> : E2PADR<5:0> -EEPROM address bit

3.1.19 RPAGE ~ R79/E2PDAT (E2P write data register)

79H(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
E2PDAT	E2PDAT<7>	E2PDAT<6>	E2PDAT<5>	E2PDAT<4>	E2PDAT<3>	E2PDAT<2>	E2PDAT<1>	E2PDAT<0>
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	0	0	0	0

Bit<7:0> : E2PDAT<7:0>-EEPROM Write data bits

3.1.20 RPAGE ~ R7A/E2PCON (E2P control register)

7AH(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
E2PCON	WRERR	PC<10>	PC<9>	PC<8>	-	CS	E2PRDEN	E2PWRE

								N
Read/Write	R/W	R	R	R	R	R/W	R/W	R/W
Reset value	0	X	X	X	0	0	0	0

Bit<7>：WRERR-EEPROM　Write failure flag bit

1: failed to write data

0: The write function is normal or not written

Bit<2>：CS-EEPROM　Enable bit

1: indicates that the EEPROM module is enabled

0: disables EEPROM

Bit<1>：E2PRDEN-EEPROM　Read data enable bit

1: Enable (Wait 2us for E2PREAD register data reading after EEPROM read status is enabled)

0: Disable

Bit<0>：E2PWREN-EEPROM　Write data enable bit

1: Enable (automatic 0 after EEPROM writing is complete)

0: Disable

3.1.21 RPAGE ~ R7B/E2PREAD (E2P read data register)

7BH(R)	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**BiTC1**	**Bit0**
E2PREAD	E2PREAD <7>	E2PREAD <6>	E2PREAD <5>	E2PREAD <4>	E2PREAD <3>	E2PREAD <2>	E2PREAD <1>	E2PREAD <0>
Read/write	R	R	R	R	R	R	R	R
Reset value	X	X	X	X	X	X	X	X

Bit<7:0> : E2PREAD<7:0>-EEPROM Read data bits

3.1.22 RPAGE ~ R7D/TC0CON (Control register)

7D(R)	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**BiTC1**	**Bit0**
TC0CON	TC0EN	RTCS	TS	TE	PAB	TC0PSR	TC0PSR	TC0PSR

						< 2 >	< 1 >	< 0 >
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	1	1	1	1

Bit<7> : TC0EN-TC0 Count enable flag bit

0: Disable

1: Enable

Bit<6>：RTCS-RTC Clock select bit

0: Disable RTC clock (crystal oscillator clock)

1: Enable RTC clock (TC0 clock source select crystal clock)

Bit<5> : TS-TC0 signal source select bit

0: Internal instruction cycle clock (TC0CKS=0)/System clock (TC0CKS=1)

1: External input clock (TC0CKS=0)/Low speed oscillator clock (TC0CKS=1)

Bit<4>：TE-TC0 Signal edge selection bit

0: The TC0 pin signal changes from low to high plus 1

1: The TC0 pin signal changes from high to low plus 1

Bit<3>：PAB-Pre-divider allocates bits

0: Predivider assigned to TC0

1: The pre-divider is assigned to WDT

Bit<2:0> : TC0PSR2 ~ TC0PSR0-TC0/WDT pre-divider selection control bit:

TC0PSR<2>	TC0PSR<1>	TC0PSR<0>	TC0 frequency division coefficient	WDT frequency division coefficient
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

3.1.23 RPAGE ~ R7E/SYSCON(System Control Register)

7E(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
SYSCON	WDTEN	EIS	PEDGEN	NEDGEN	TC0WE	TC1WE	E2PWE	EXINTWE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value	1	0	0	0	0	0	0	0

Bit<7>：WDTEN-WDT Enable control

1: Enable

0: Disable

Note: To enable watchdog, WDTEN is required and the OPTION [Watchdog] is selected [Enable].

Bit<6> : EIS-P60 pin external interrupt enable bit

1: Enable the P60 external interrupt function, P60 pin is set as the input port by default, and the status of the pin can be read by the P6 port

0: Disable, P60 is GPIO, and the EXINT channel is blocked

Bit<5> : PEDGEN- External interrupt rising edge trigger selection bit

1: Enable

0: Disable

Bit<4> : NEDGEN- External interrupt drop edge trigger selection bit

1: Enable

0: Disable

Bit<3> : TC0WE-TC0 Wake up enable bit

1: Enable TC0 wake up, wake up idle mode, wake up sleep mode and idle mode in RTC mode

0: disables TC0 wake up

Set TC0WE=1&RTCS=1 in RTC mode. LXT will continue to work and will not stop when hibernating. Otherwise, LXT will stop when hibernating.

Bit<2> : TC1WE-TC1/PWM wake up enable bit

1: enables TC1/PWM wake up to wake up idle mode

0: disables TC1/PWM wake up

Bit<1> : E2PWE-EEPROM write finish wake up enable bit

1: enable (write failure will still wake up, pay attention to check the write failure flag bit)

0: Disable

Bit<0> : EXINTWE- external interrupt wake up enable bit

1: Enable

0: Disable

3.1.24 RPAGE ~ R7F/INTE(Interrupt enable register)

7F(R)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	BiTC1	Bit0
INTE	-	-	-	E2PIE	TC1IE	EXIE	P6ICIE	TC0IE
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W

Reset value	0	0	0	0	0	0	0	0

Bit<7:5> : unused bit

Bit<4> : E2PIE-EEPROM write completion interrupt enable bit

Bit<3> : TC1IE-TC1 Timing overflow /PWM period overflow interrupt enable bit

Bit<2> : EXIE- External port interrupt enable bit

Bit<1> : P6ICIE-P6 port status change interrupt enable bit

Bit<0> : TC0IE-TC0 Timing overflow interrupt enable bit

1: Enable

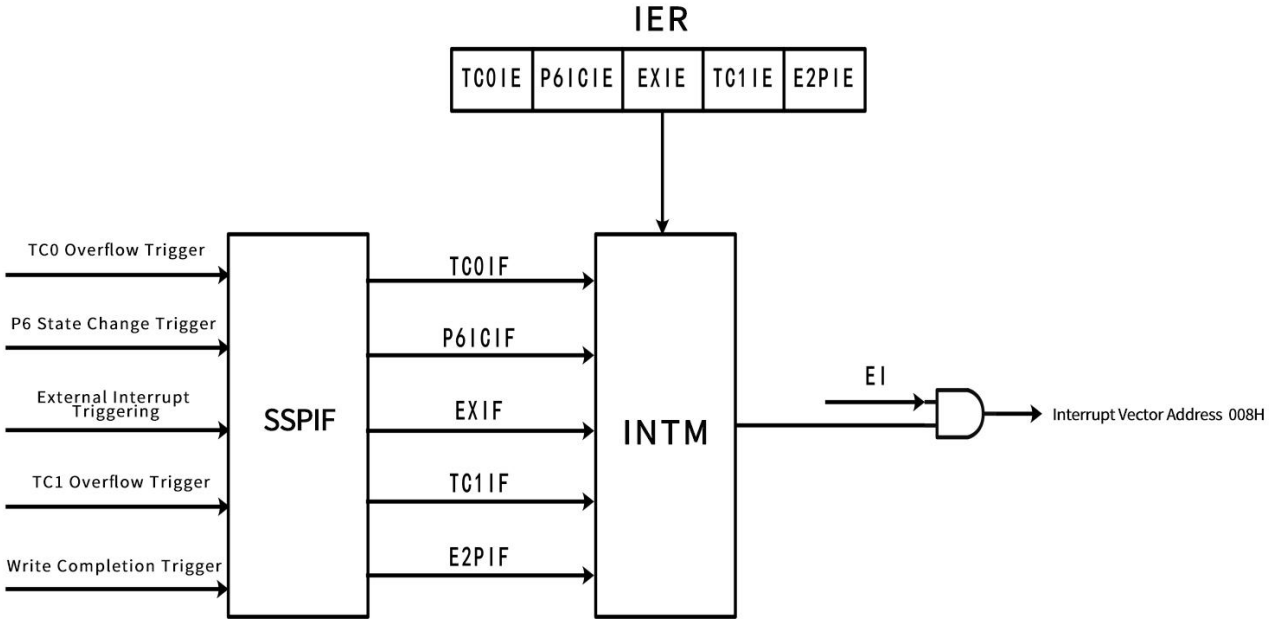
0: Disable

3.2 Interrupt

The JZ8PE255E has five interrupt sources, and to use any of them, the total interrupt, or "EI" instruction, must be enabled. The interrupt vector is the fixed default address 008H. Here are the characteristics of each interrupt:

Interrupt type	Interrupt Source	Enable condition	Interrupt flag
Exterior	External interrupt	EI + EXIE=1	EXIF
Exterior	P6 Status change Interrupt	EI + P6ICIE=1	P6ICIF
Internal	TC0 overflow interrupted	EI + TC0IE=1	TC0IF
Interior	TC1 Timing overflow /PWM Cycle overflow interrupt	EI + TC1IE=1	TC1IF
Interior	E2P write swap complete interrupt	EI + E2PIE=1	E2PIF

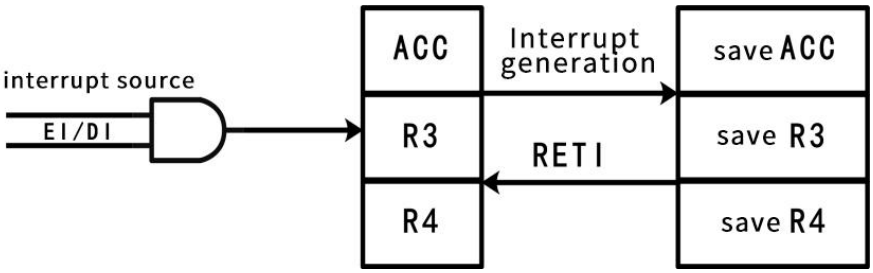
The RF of RPAGE is the interrupt status flag register, which records the interrupt flag bit when an interrupt generates an interrupt request. R7F sets the interrupt register. Interrupt permit and disable are set in these two registers. The total interrupt is allowed by the EI instruction, in contrast, the total interrupt is forbidden by the DI instruction. When an interrupt is generated, the execution of its next instruction will be executed from the interrupt vector address 008H. The corresponding interrupt flag bit must be cleared to zero before leaving the interrupt service routine to avoid the error of the interrupt.



Schematic diagram of interrupt principle

3.2.1 Interrupt site protection

In response to the interrupt process, it is strongly recommended to use interrupt protection in the program, save the contents of ACC, R3, R4, until leaving the interrupt subroutine, the saved value will be reloaded into ACC, R3, R4, so as to avoid instructions to change the value of ACC, R3, R4 when executing the interrupt subroutine. Resulting in an error when returning to the main program. As shown in the image below:



Software interrupt site protection schematic

3.3 Resetting

3.3.1 Overview of the reset function

The JZ8PE255E system provides 4 reset methods:

- POR power-on reset
- RESET pin input low level reset
- WDT watchdog overflow reset
- LVR low voltage reset

When either of these resets occurs, all system registers are initialized to the reset value, the program stops running, and the program counter PC clears to zero. After the reset, the system starts running again at 0000H.

Any kind of reset requires a certain response time, and the system reset mechanism can ensure the reliable reset of MCU. The time required to complete the reset is different for different types of oscillators. Therefore, the rise rate of VDD and the starting time of different oscillators are not fixed. RC oscillators have the shortest starting time, while crystal oscillators have a longer starting time. In the process of using the user terminal, attention should be paid to the requirements of the application scenario on the power-on reset time.

3.3.2 Resetting the WDT watchdog

A watchdog reset is a protection setting for the system. Under normal conditions, the watchdog timer is reset by the program. If an error occurs, the system is in an unknown state, the watchdog timer overflows, and the system resets. After the watchdog is reset, the system restarts and enters the normal state.

- Watchdog timer status: The system checks whether the watchdog timer overflows. If it overflows, the system resets.
- System initialization: all system registers are set to the default value of initialization;
- Oscillator starts working: oscillator starts providing the system clock;
- Execution program: the end of the power-on, the program starts to run;

Watchdog timer application notes:

- Checking the status of the I/O port and the contents of RAM before zeroing out the watchdog enhances the reliability of the program;
- Do not zero the watchdog in the interrupt, otherwise it can not detect the main program running;
- The program should only have one clear watchdog action in the main program, this architecture can maximize the protection function of the watchdog.

3.3.3 POR power-on reset

Power-on reset is closely related to LVR operations. The power-on process of the system is in the form of a gradual upward curve, and it takes a certain time to reach the normal level value.

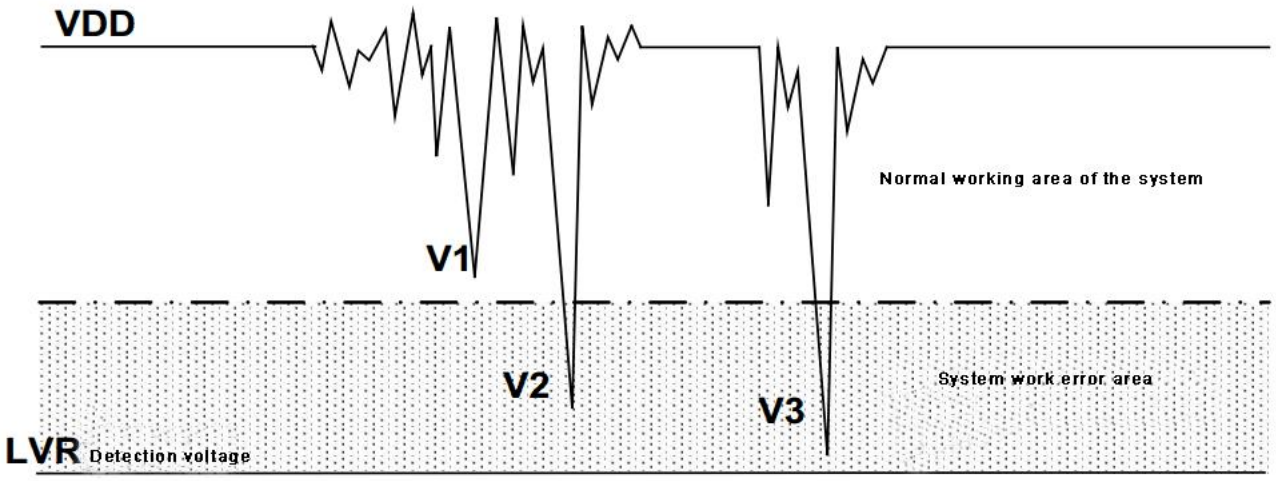
- Power-on: The system detects the power supply voltage rise and waits for it to stabilize;
- External reset (limited to the external reset pin enabled state) : The system detects the external reset pin status. If it is not high, the system maintains the reset state until the external reset pin is released;
- System initialization: All system registers are set to their initial values;
- Oscillator starts working: oscillator starts providing the system clock;
- Execution program: the end of the power-on, the program starts to run;

The power-on reset time is determined by the selection of [Reset time] in OPTION, as shown in the following table:

PWRT and WDT	Reset build time
PWRT=WDT	4.5ms(follow watchdog reset time)
PWRT=WDT	18ms(reset time with watchdog)
PWRT=WDT	72ms(follow watchdog reset time)
PWRT=WDT	288ms(follow watchdog reset time)
PWRT≠WDT	140us(independent fixed reset time)

3.3.4 LVR low voltage reset

Power-off reset refers to the situation where the system voltage drops due to external factors (such as interference or changes in external load). Power-off may cause abnormal system working status or program execution errors.



A voltage drop may enter the system dead zone. A system dead zone means that the power supply cannot meet the minimum operating voltage requirements of the system. The picture above is a typical power-down reset schematic. In this diagram, the VDD is severely disturbed and the voltage drop is very low. Above the dotted line, the system works normally. Below the dotted line, the system enters an unknown working state. This region is called the dead zone. When VDD drops to V1, the system is still in normal state; When VDD falls to V2 or V3, the system enters the dead zone, which is prone to errors. The system may enter the dead zone under the following conditions:

DC is in operation:

DC is generally used in battery power supply, when the battery voltage is too low or the MCU drive load, the system voltage may fall and enter the dead zone. At this time, the power supply will not further drop to the LVR detection voltage, so the system is maintained in the dead zone.

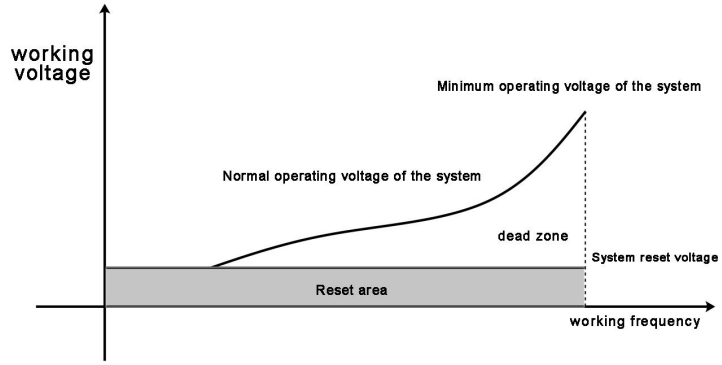
In AC operation:

When the system uses AC power supply, the DC voltage value is affected by the noise in the AC power supply. When the external load is too high, such as when the motor is driven, the interference generated by the load action also affects the DC power supply. If the VDD falls below the minimum operating voltage due to interference, the system may enter an unstable working state. In AC operation, the system is powered on and off for a long time. The power-on sequence protection enables the system to power on normally, but the power-off process is similar to that in

DC operation. After the AC power is turned off, the VDD voltage is easy to enter the dead zone during the slow decline.

3.3.5 Relationship between working frequency and LVR low voltage detection

In order to improve the performance of the system power failure reset, the minimum operating voltage value of the system must be defined first. The minimum operating voltage of the system is related to the execution speed of the system, and the minimum operating voltage value is different under different execution speed.



As shown in the figure above, the normal operating voltage area of the system is generally higher than the system reset voltage, and the reset voltage is determined by the low voltage detection (LVR) level. When the system execution speed increases, the system minimum operating voltage also increases accordingly, but because the system reset voltage is fixed, there will be a voltage region between the system minimum operating voltage and the system reset voltage, the system can not work normally, and will not reset, this area is the dead zone.

In order to avoid dead zone voltage, the corresponding LVR reset voltage point should be selected when selecting the working frequency. The following table:

IRC frequency	Oscillator frequency doubling	Clocks frequency division	LVR recommended voltage points
IRC-8MHz	Frequency multiplier	2 Clocks	As = 3.9 V
IRC-8MHz	No frequency doubling	2 Clocks	As = 2.4 V
IRC-910KHz	Frequency doubling	2 Clocks	As = 1.8 V
IRC-910KHz	No frequency doubling	2 Clocks	As = 1.8 V

Note: 1, operating frequency = instruction cycle frequency =IRC frequency + Clocks frequency division; 2, the corresponding value of this working frequency and LVR reset voltage

point is only recommended value, the user can adjust the reset voltage point appropriately according to the specific application in the course of use.

3.4 Working mode

The JZ8PE255E can operate at different clock frequencies in 4 operating modes that control the operation of the oscillator, the execution of the program, and the functional loss of the analog circuit.

- High speed mode: The system clock selects a high speed IRC clock;
- Low speed mode: system clock selects internal low speed clock;
- Idle mode: the system clock works normally, and other parts go to sleep (TC0 and TC1/PWM system clock can continue to work and wake up the system, RTC overflow and P6 port status change can wake up the system);
- Sleep mode: all functions stop working, the system enters sleep (RTC mode can work), P6 port status change can wake up, RTC overflow can wake up;

Function module	High speed mode	Low Speed mode	Idle mode	Sleep Mode
IHRC	Run	STPHX control	STPHX control	Stop
ILRC	Run	Run	Run	Stop
CPU instructions	Carry out	Execute	Stopping	Stop
TC0	Working	Workable	Workable	RTC works
TC1/PWM	Works	Workable	Workable	Stop
Internal break	All valid	All valid	TC0,TC1/PWM work	Stop
External interrupt	Valid	Valid	Valid	Valid
Wake up function	-	-	P6IC,TC0,TC1/PWM,	P6IC,RTC
Watchdog timer	WDT option control	WDT Option Control	WDT option control	WDT Option Control

3.4.1 High-speed mode

High speed mode is the system high speed clock working mode, and the system clock source is provided by the high speed RC oscillator. The program is executed. After the power-on reset or either reset is triggered, the system enters high-speed mode to execute the program. The system enters high speed mode when it is awakened from sleep mode. In high speed mode, the high speed oscillator works normally and consumes the most power.

◆ The program is executed and all the functions can be controlled;

- The system speed is high;
- Both the high speed oscillator and the internal low speed oscillator work normally;
- Through the CPU mode control register, the system can switch from the high-speed mode to any other working mode;
- After waking up from sleep mode, the system can enter high-speed mode.
- The low-speed mode can be switched to the high-speed mode;
- Enter the idle mode from the high-speed mode, and return to the high-speed mode after awakening;

3.4.2 Low Speed mode

Low speed mode is the system low speed clock working mode. The system clock source is provided by the internal low speed RC oscillator. The low speed mode is controlled by the CLKMD bit of the CPU mode control register. When CLKMD=0, the system is in high speed mode; When CLKMD=1, the system enters low speed mode. After entering low speed mode, the high speed oscillator cannot be automatically disabled and must be disabled by SPTHX bit to reduce power consumption.

- The program is executed and all functions can be controlled;
- The system speed is low;
- The internal low speed RC oscillator works normally and the high speed oscillator is controlled by STPHX=1. In low speed mode, it is highly recommended to stop the high speed oscillator;
- Through the CPU mode control register, the low-speed mode can be switched to other working modes.
- From low mode to sleep mode, wake up to return to low mode;
- High speed mode can be switched to low speed mode;
- Enter the idle mode from the low mode, and return to the low mode after awakening;

3.4.3 Idle mode

Idle mode is another ideal state. In sleep mode, all functions and hardware devices are disabled, but in idle mode, the system clock keeps working, and power consumption in idle mode is greater than that in sleep mode. In idle mode, no program is executed, but the timer and PWM with wake function still work normally, and the clock source of the timer and PWM is the system clock that is still working. In idle mode, there are four ways to wake up the system: 1, P6 port status change triggered; 2, TC0 timer wake up; 3, TC1 timing /PWM cycle overflow can wake up; 4, RTC timing wake up. The user can set a fixed period for the timer or PWM, and the system will be woken up when it overflows. The CPU mode control register IDLE bit determines whether to enter the IDLE mode. When IDLE=1, the system enters the idle mode.

- The program stops executing and all functions are disabled.
- The timer with wake-up function works normally;
- The oscillator as the system clock source works normally, and the working state of other oscillators depends on the configuration of the system working mode;
- From the high-speed mode into the idle mode, wake up after the return to the high-speed mode;
- From low-speed mode to idle mode, after being woken up to return to low-speed mode;
- The wake up mode in idle mode is P6 port state change trigger wake up, TC0 timer overflow and TC1 timing overflow /PWM cycle overflow, RTC timing wake up;
- In idle mode, TC0 and TC1/PWM functions are still effective;

3.4.4 Sleep mode

Sleep mode is the ideal state of the system where no program is executed (except RTC) and the oscillator stops working. The entire chip consumes less than 1uA. Sleep mode can be triggered by P6 port status changes, RTC overflow wake up. Enter sleep mode from high speed mode or low speed mode, and return to the corresponding mode after being woken up. The IDLE bit of the CPU mode control register controls whether to enter the sleep mode. When IDLE=0, the system enters the sleep mode.

- The program stops executing and all functions are prohibited;
- All oscillators, including external high speed oscillators, internal high speed oscillators, and internal low speed oscillators, stop working;
- Power consumption is less than 1uA;

- From high speed mode to sleep mode, wake up after the return to high speed mode;
- From low speed mode to sleep mode, wake up to return to low speed mode;
- The waking source of sleep mode is P6 port state change trigger, RTC overflow wake up;

3.5 System Clock

The JZ8PE255E has 3 types of oscillators integrated inside. See the following table for details:

Oscillator types	Instructions
IHRC (Built-in High speed RC oscillator)	910K/1M/8M can be selected via RCM
ILRC (Built-in Low speed RC oscillator)	14KHz
LXT (Low speed crystal oscillator)	32.768K ~ 400K
HXT (High speed crystal oscillator)	400K to 16M

3.5.1 Internal RC oscillator

The JZ8PE255E offers an internal RC mode with a frequency of 8MHz by default.

The internal RC oscillation mode contains three frequency values of 8MHz, 1MHz, and 910KHz. By setting the configuration bits of OPTION, you can select the IRC operating frequency, and the following is their correspondence:

Firc	IRC frequency
8 M	8MHz for IRC frequency
1 M	Choose 1MHz for IRC frequency
910K	Choose the IRC frequency as 910KHz

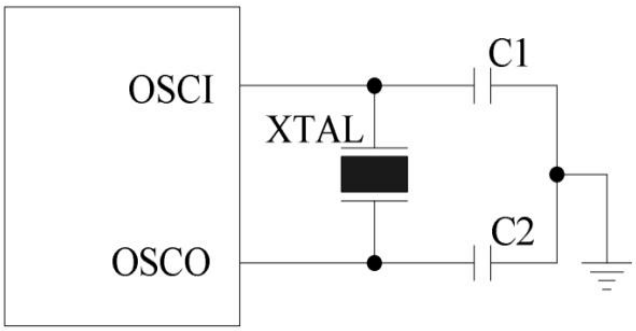
The JZ8PE255E offers a variety of frequency splitting options that can be selected in the OPTION for more occasions. The following table:

Clocks	Clocks Frequency Division

2clock	The frequency division is 2clock
4clock	The frequency division is 4clock
8clock	The frequency division is 8clock
16clock	The frequency division is 16clock
32clock	The frequency division is 32clock

3.5.2 External crystal/ceramic oscillator

In most applications, pin OSCO and OSCI can be connected to a crystal or ceramic resonator to generate oscillations. The circuit diagram below is suitable for both HXT and LXT modes. The recommended values for C1 and C2 are shown in the table. Due to the different characteristics of each resonator, the user should refer to its specifications to select the appropriate value of C1 and C2.



Crystal oscillator application circuit

Capacitor selection reference for crystal oscillator or ceramic oscillator:

Oscillator mode	Frequency mode	Frequency	C1(pF)	C2(pF)	Recommended value of built-in capacitance
Ceramic oscillator	HXT	455KHz	100-200.	100-200.	-
Crystal oscillator	LXT	32.768 KHz	5-30	5-30	12.5 pf
	HXT	8 MHz	5-20	5-20	9pf
		16 MHz	5-20	5-20	-

Note: The above data is for reference only, all subject to the actual test

3.5.3 Application Description of clock module

- Internal oscillator is the most commonly used mode of oscillation, which can eliminate the external circuit;

- When using the external clock input, the clock signal is input from OSCI, OSCO can be suspended;
- Different external conditions, the clock frequency of each oscillation mode may be slightly different, should be used according to the needs of reasonable choice;

3.6 I/O ports

The JZ8PE255E has a set of bidirectional I/O ports with 6 inputs and 6 outputs, and the I/O can be reused for other functions.

6 programmable pull-up I/O pins: P6<5:0>;

6 programmable drop-down I/O pins: P6<5:0>;

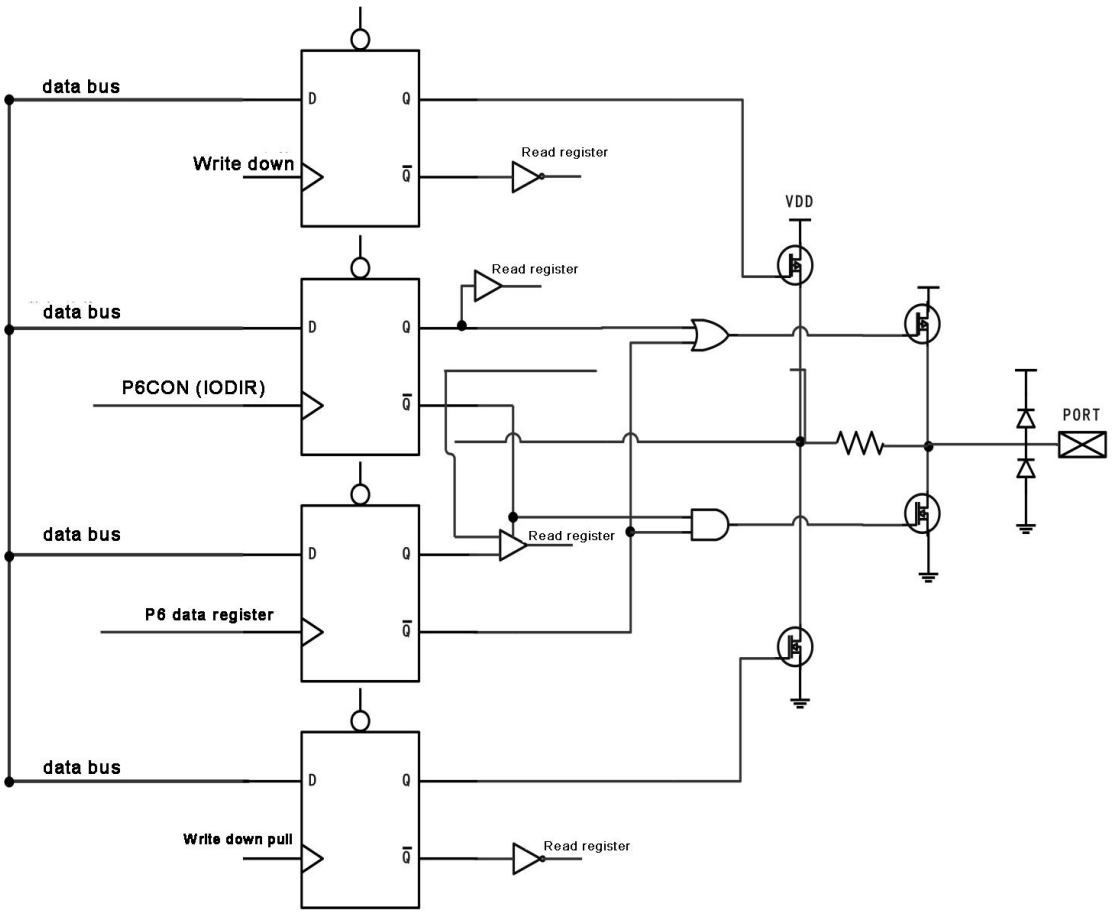
6 configurable drive enhanced I/O pins: P6<5:0> feed current enhanced, P6<5:4>, P6<2:0> pull current enhanced;

3 configurable secondary fill current enhancement: P60, P61, P62;

6 programmable port status change wake-up I/O pins: P6<5:0>;

3.6.1 GPIO internal structure diagram

The following internal structure diagram is for reference only and does not represent the actual circuit.



IO control register/Data register/pull-up/pull-down structure circuit

3.6.2 Port Driver capability description

The JZ8PE255E has 6 primary perfusion current enhanced IO ports (P6<5:0>), 5 primary pull current enhanced IO ports (P6<5:4>,P6 <2:0>), and 3 secondary perfusion current enhanced IO ports (P60,P61,P62). The pull current enhancement needs to be selected through the configuration OPTION of [Drive enhancement] and [secondary drive enhancement].

Drive Category	Drive capability (VOH=4.4V, VOL=0.6V)	Driver port
No drive capability enhancement	IOH 6mA IOL 16mA	P6<5:0>
First stage pull current enhancement	IOH 12mA	P6<5:4>, P6<2:0>
Primary filling current enhancement	IOL 21mA	P6<5:0>
Secondary perfusion current enhancement	IOL 27mA	P60,P61,P62

Note: Driving ability is for reference only, the specific value is based on actual measurement.

3.6.3 Port Schmidt parameter

The table of Schmidt characteristics of the JZ8PE255E port is as follows (for reference only) :

Ports	SMT
P6<5:0>	VDD / 0.54 * 0.25 * VDD

The above parameters are for reference only, please refer to the measured data of the target prototype.

3.6.4 Wake Up When Port Status Changes

The JZ8PE255E includes 6 programmable port state change Wake up I/O: P6<5:0>. The chip executes the "SLEEP" command to enter the sleep mode. At this point, the system clock stops, all modules stop working, WDT (if enabled) clears 0, but continues to run. Port status change wake up can be selected through the program to continue the original process (DI before SLEEP) or perform the corresponding jump (EI before SLEEP), and open the corresponding enable control bit, jump to interrupt subroutine.

Port status change query mode wake up Settings

1, P6 port wake up port set as input;

2. Select the internal pull up or pull down of the wake up port according to your needs;

4, enable P6 input change wake up enable register P6IWE;

5, execute DI instruction, do not enter interrupt address port;

6, execute the "SLEEP" instruction, enter the SLEEP sleep mode;

7. After waking up, execute the next instruction of SLEEP;

Port state change interrupt mode wake up Settings

1, P6 port wake up port set as input;

2, according to the need to select the internal wake up and down port;

3, enable port status change independent interrupt and wake up control;

4, enable P6 port status change interrupt;

5, execute the "EI" command, wait to enter the interrupt address port;

6, under the instruction "SLEEP", enter the SLEEP sleep mode;

7, wake up will enter the interrupt address interface, exit the interrupt, execute the next instruction SLEEP;

3.7 Timer

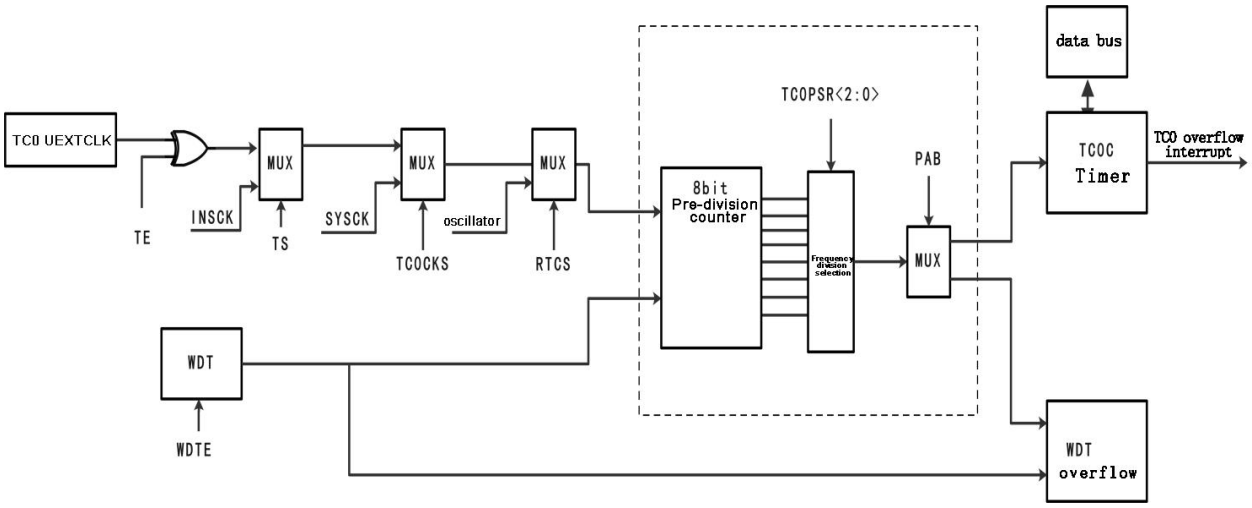
3.7.1 TC0 Timer counter

The JZ8PE255E offers an 8-bit counter as a pre-divider for TC0 and WDT. The pre-divider is available for TC0 or WDT only at the same time, and the PAB bit in the CONT register determines the allocation of the pre-divider. The TC0PSR<2:0> three bits determine the pre-divider ratio. Each time a value is written to TC0C in TC0 mode, the pre-split register is cleared to zero. When the pre-divider is assigned to WDT mode, the values of the WDT and the pre-divider register are cleared when the "CWDT" or "SLEEP" instruction is executed. If the pre-divider is assigned to TC0 and then to WDT, the contents of the pre-divider counter are cleared automatically, and vice versa.

The TC0 is an 8-bit upstream counter that works as long as there is a clock. The clock source can either be an internal system clock (triggered by the rising edge), an external clock can be selected (input by the TC0 pin, triggered edge is optional), or an RTC mode can be selected using an external crystal oscillator clock count. TC0 adds 1 to the counter on each clock arrival. The system provides an 8Bit counter as a pre-divider for the TC0. The TC0 pre-divider, trigger edge, clock, etc. can be set through the CONT register.

TC0 count overflow can form interrupt signals.

In IDLE mode, TC0 interrupt can wake up the circuit. After wake up, you can choose to interrupt or continue to execute the original program. For the method, refer to the port status change to wake up.



TC0/WDT structure block diagram

3.7.1.1 TC0 timing setting instructions

- Assign an initial value to the TC0C register;
- Set the value of the TC0CON register (select as a timer or counter and pre-division ratio);
- To use as a counter, it is necessary to select the TC0 external signal as positive edge or negative edge plus 1 in the TC0CON register;
- If the interrupt function needs to be performed, TC0IE (Bit0) in the R7F register must be set to 1, and EI instruction should be executed;
- Interrupt program part will manually save ACC, STATUS and R4 in the stack, after the execution of RETI instruction, and then take out from the stack, before exiting the interrupt to clear the TC0 interrupt flag bit;

3.7.1.2 TC0 timing calculation Description

TC0 timing function by writing the value to the TC0 register, assign an initial value to the timer, and the timer starts to add up from the initial value position until the timer overflows and generates an interrupt.

TC0 timing time calculation formula (select internal instruction cycle clock) :

$$\text{TC0 timing time} = (\text{System clock frequency division/Fosc}) \times (\text{TC0frequency demultiplication}) \times (256 - \text{TC0initial value})$$

Example:

System clock frequency division =2clock, Fosc=8 MHz, TC0 frequency division selection =4 frequency division, TC0 initial value =156;

$$\text{TC0timing time} = (2/8) \times (4) \times (256 - 156) = 100\ \text{us}$$

TC0 timing time calculation formula (select external input clock) :

$$\text{TC0timing time} = (\text{External input clock}) \times (\text{TC0fractional frequency}) \times (256 - \text{TC0initial value})$$

Example:

External input clock =1 MHz, TC0 crossover selection =4 crossover, TC0 initial value =156;

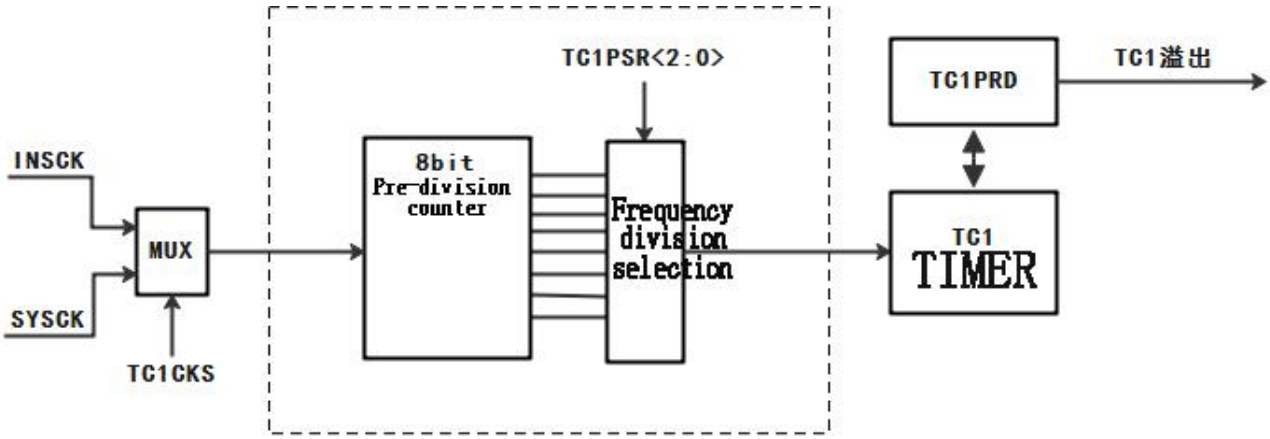
$$\text{TC0 timing time} = (1) \times (4) \times (256 - 156) = 400\ \text{us}$$

3.7.2 TC1 timing counter

The TC1 timing counter provides an 8-bit pre-divider, and the TC1CON register's TC1PSR<2:0> three bits determine the pre-divider ratio. Under the mode of TC1 each TC1EN/PWM1EN/PWM2EN/PWM3EN enabled, preassigned frequency registers are reset.

TC1 is an 8Bit upstream counter. The TC1 timer needs to enable TC1EN to work. The clock source is the internal instruction clock/internal system clock. When each clock cycle comes, the counter is increased by 1. The TC1 count value is consistent with the TC1PRD register set value, resulting in overflow. If TC1IE and EI are enabled, the system jumps to the corresponding interrupt vector address and executes the interrupt service program.

In IDLE mode, TC1 interrupt can wake up the circuit (the clock selects the system clock), and after waking up, you can choose to interrupt or continue to execute the original program. For the method, refer to the port status change to wake up.



TC1 structure block diagram

3.7.2.1 TC1 Timing Setting Instructions

1. Assign an initial value to the TC1PRD register;

2, set TC1CON register, according to the need to configure the pre-division ratio;

Enable TC1IE of R7F/INTE register to open interrupt, and execute EI instruction;

Enable TC1EN, open TC1 timer count;

5, the system execute interrupt service program will automatically save ACC, STATUS and RSR data, after the execution of RETI instruction, the data will automatically recover, before exiting the interrupt to clear the TC1 interrupt flag bit;

3.7.2.3 TC1 timing calculation description

TC1 timing function by writing the value to the TC1PRD register, the timer starts to add up from the initial value 0x01, until the timer value matches the TC1PRD register value, then overflow execution interrupt service program.

TC1 timing time calculation formula:

$$\text{TC1timing time} = (1/\text{Fosc}) \times (\text{TC1frequency demultiplication}) \times (\text{TC1PRD} - 1)$$

Example:

Fosc=8 MHz, TC1 crossover selection =8 crossover, TC1PRD value =255;

$$\text{TC1timing time} = (1/8) \times (8) \times （255 - 1） = 254\text{us}$$

3.7.2.4 TC1 Idle Mode Wake up Instructions

TC1 can wake up idle mode, enable R7E/SYSCON register bit2-bit TC1WE, and select the TC1 clock source as the system clock. IDLE = 1 plus the SLEEP instruction system goes into idle mode and the TC1 timer works normally. When the TC1 timer overflows, the system wakes up. If TC1IE and EI are enabled, the system will enter interrupt after waking up. If DI is executed, the system will execute the next command after waking up.

3.8 PWM pulse width modulation

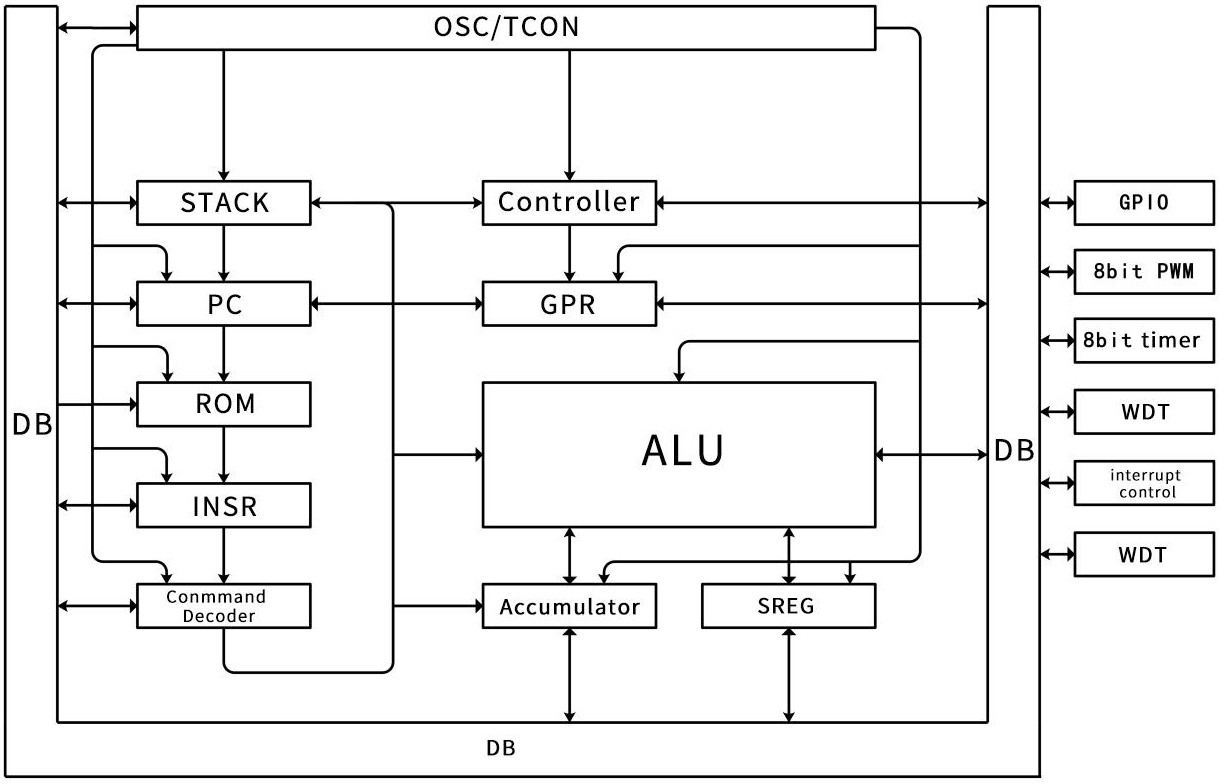
JZ8PE255E provides 3 common period 8-bit PWM signals to generate pulse width modulation signals. The PWM output waveform is determined by the period and duty cycle, and the transmission rate is the reciprocal of the period. The chip provides dead zone complementary output, which is used as IPWM1 after passing PWM2 and PWM3 XOR, and PWM1 as dead zone complementary signal.

PWM comes with period overflow interrupt, which can be jumped to interrupt when enabled.

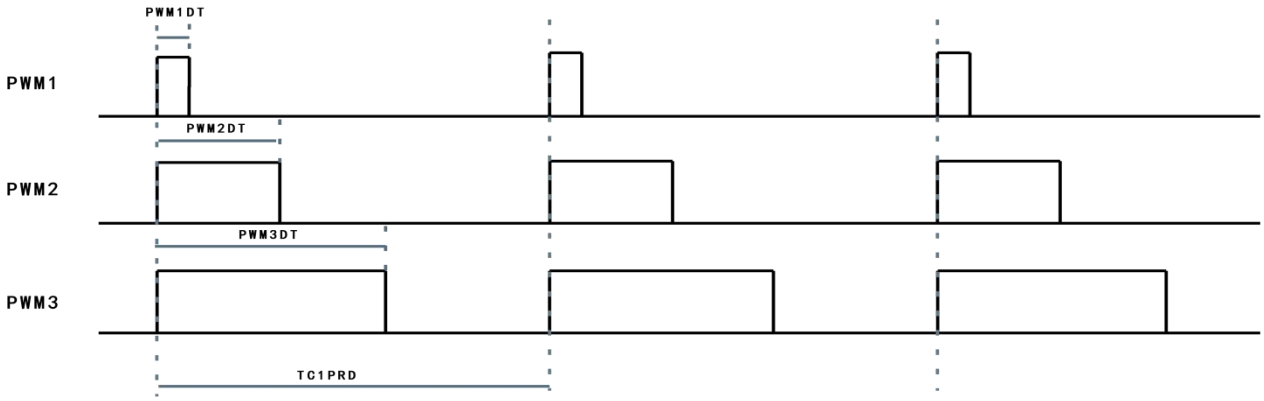
In IDLE(idle mode), PWM can wake up the system by selecting TC1CKS=1 in the CPU mode control register and enabling TC1WE.

3.8.1 Internal structure and timing of PWM

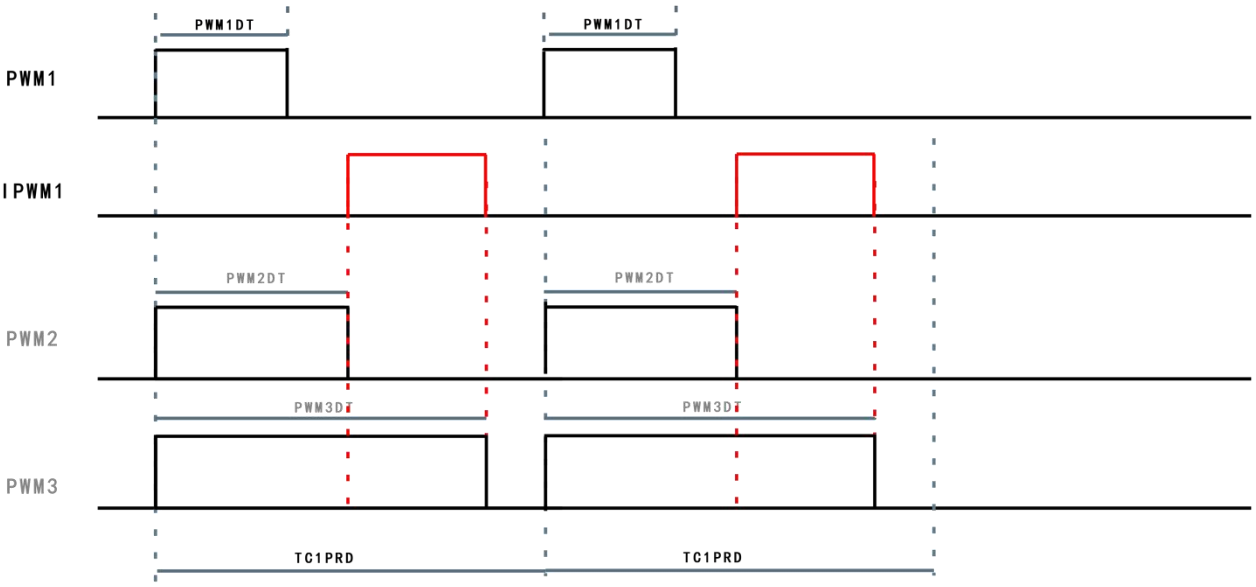
The following internal structure diagram is for reference only and does not represent the actual circuit.



PWM working structure circuit



3 way common-period PWM timing description



PWM and IPWM timing instructions

3.8.2 PWM period and duty cycle

PWM provides a clock counter (TC1) with 8bit programmable pre-division that acts as the baudrate clock generator for the PWM module. By enabling TC1EN in PWM control register, enable TC1 counter function, by TC1PTEN and TC1PSR<2:0> control bit, TC1 counter can be pre-divided frequency Settings.

PWM cycle by writing the value to the PWM cycle register (TC1PRD), when the TC1 counter value is equal to the TC1PRD value, the following events occur in the next increment cycle:

- TC1 counter cleared to zero;
- Corresponding PWM output pin set high level;
- Generate PWM cycle overflow interrupt (if enabled);

- The PWM duty cycle is latched from PWM1DT/PWM2DT/PWM3DT to the DT/TC1 comparison register;

PWM cycle calculation formula:

$$\text{PWM cycle} = (\text{TC1PRD}) \times (\frac{1}{Fosc}) \times (\text{TC1}_{\text{frequency division}})$$

Example:

TC1PRD=100, Fosc=8 MHz, TC1 frequency division selection =2 frequency division;

$$\text{PWM cycle} = (100) \times \left(\frac{1}{8}\right) \times (2) = 25 \text{ us}$$

PWM duty cycle by writing the value to the PWM duty cycle register (PWM1DT,PWM2DT,PWM3DT), when the value of the TC1 counter overflow is cleared, the value of PWM1DT/PWM2DT/PWM3DT is locked to the DT/TC1 comparison register. When the value of the DT/TC1 comparison register equals the value of the TC1 counter, the PWM output pin is set to low. The value of PWM1DT,PWM2DT,PWM3DT can be written at any time, but the value of the DT/TC1 comparison register is only written when the cycle overflows:

The formula for calculating PWM duty cycle is:

$$\text{PWM duty cycle} = (\text{PWMxDT}) \times (\frac{1}{Fosc}) \times (\text{TC1}_{\text{frequency division}})$$

Example:

PWMxDT=50, Fosc=8 MHz, TC1 frequency division selection =2 frequency division;

$$\text{PWM}_{\text{duty cycle}} = (50) \times \left(\frac{1}{8}\right) \times (2) = 12.5 \text{ us}$$

3.8.3 Setting instructions for PWM pulse width modulation

- Set TC1CON register, select the corresponding timer for PWM mode, timer frequency division ratio, timer clock source, etc.;
- Write the value of RPAGE-R9 register to determine the period of the PWM channel;
- Write the value of PWMxDT register to determine the duty cycle of the PWM channel;
- Enable the corresponding timer;
- Enable or disable the timer interruption corresponding to PWM, and press the "EI" or "DI" command (if necessary);

3.9 EEPROM module

The JZ8PE255E has 64 Byte EEPROM integrated inside. This type of memory content is not directly mapped to the register, but is indirectly addressed through the Special Function register (SFR). By giving the E2PADR register access address, the E2PCON register configures read and write operations to read or write data in the corresponding read and write data register. The chip realizes the self-timing function of erasing and programming on the hardware, without software query, saving code space. EEPROM function module has a total of 4 SFR registers for read, write and control:

- E2PADR (EEPROM address Register)
- E2PCON (EEPROM control register)
- E2PDAT (EEPROM write data register)
- E2PREAD (EEPROM Read data register)

Note: 1, when the power supply voltage is less than 2.5v, there is a probability of writing data failure, so ensure that the chip works above 2.5v, and EEPROM can be used normally.

2, After enabling EEPROM read state, wait 2us to start reading EEPROM data.

3.9.1 EEPROM Application Instructions

Read data operation

- Set the E2PCON register, which can set the reading speed according to the need;
- Set the address to be read to E2PADR;
- Set the read enable flag bit E2PRDEN to 1;
- Read the value of the E2PREAD register;
- Clear read enable flag bit E2PRDEN;

Write data operation

- Set the E2PCON register to enable wake up as needed (with E2PIE to jump to interrupt after wake up);
- Set the address to write to E2PADR;

- Assign the value to be written to E2PDAT;
- Set the write enable flag bit E2PWREN to 1;
- Wait for the write to complete, the write enable flag bit hardware automatically clear (write failure automatically clear);

4. OPTION configuration table

CODE OPTION	Options	Function Description
A Guard Dog	Enable	Watchdog WDT is enabled
	Prohibited	Guard dog WDT prohibited
Clocks Frequency division	2 Clocks	Instruction cycle Select 2 Clocks
	4 Clocks	Instruction cycle select 4 Clocks
	8 Clocks	Instruction cycle Select 8 Clocks
	16 Clocks	Select 16 Clocks for the instruction cycle
	32 Clocks	Instruction cycle Select 32 Clocks
IRC frequency	8M	IRC frequency select 8M
	1M	Select 1M IRC frequency
	910KHz	The IRC frequency is selected as 910KHz
Oscillator frequency doubling option	Disable	The oscillator frequency doubling function is disabled
	Enable	Enable the frequency doubling function of the oscillator
Low voltage reset	As = 1.2 V	Low pressure reset point select 1.2V
	As = 1.6 V	Low pressure reset point select 1.6V
	As = 1.8 V	Low pressure reset point select 1.8V
	As = 2.4 V	Low pressure reset point select 2.4V
	As = 2.7 V	The low voltage reset point is 2.7V
	As = 3.3 V	Low pressure reset point select 3.3V
	As = 3.6 V	Low pressure reset point select 3.6V
	As = 3.9 V	Low pressure reset point select 3.9V
OTP paging selection	Use 2K	Programs use OTP full 2K space
	Use the first 1K	Programs only use the first 1K of OTP space
	Use the back 1K	Programs only use post-OTP 1K space
Code Encryption	2K/ front 1K/ back 1K no encryption	OTP program space selection is not encrypted (Storage space is controlled by OTP paging selection)

	2K/ pre-1K/post-1K encryption	OTP program space select encryption (Storage space is controlled by [OTP Paging Selection])
Reset port pull-up	Enable	Enable the pull-up of the P63 port
	Disable	Do not pull up the P63 port
P63 port	GPIO	P63 as a universal I/O port
	RST	P63 as the external reset port

Reset time	PWRT = WDT = 4.5 ms	Reset setup time =WDT overflow time (regardless of frequency) = 4.5ms
	PWRT=WDT=18ms	Reset build time =WDT overflow time (regardless of frequency) = 18ms
	PWRT=WDT=72ms	Reset build time =WDT overflow time (regardless of frequency) = 72ms
	PWRT=WDT=288ms	Reset build time =WDT overflow time (regardless of frequency) = 288ms
	PWRT = 140 us, WDT = 4.5 ms	Reset setup time =140us,WDT overflow time (regardless of frequency) =4.5ms
	PWRT=140us,WDT=18ms	Reset build time =140us,WDT overflow time (regardless of frequency) =18ms
	PWRT=140us,WDT=72ms	Reset build time =140us,WDT overflow time (regardless of frequency) =72ms
	PWRT=140us,WDT=288ms	Reset build time =140us,WDT overflow time (regardless of frequency) =288ms
RTC	Prohibited	Disable the RTC function
	Enable	Enable the RTC function
Driver Enhancement	Forbidden	IO port drive enhancements are disabled
	Enable	Enable P6<5:0> Feed current enhancement and P6<5:4><2:0> pull current enhancement
Secondary Drive enhancement	P60/P61/P62 secondary drive enhancement prohibited	P60/P61/P62 secondary perfusion current enhancement is prohibited
	P60/P61/P62 secondary strong irrigation is enabled	Enable P60/P61/P62 secondary irrigation current enhancement

5. Instruction set

Instructions	Command actions	Flag bit effect
ADD A,R	A+R→A	Z,C,DC
ADD R,A	A+R→R	Z,C,DC
AND A,R	A&R→A	Z
AND R,A	A&R→R	Z
CLRA	0→A	Z
CLR R	0→R	Z
INVA R	/R→A	Z
INV R	/R→R	Z
DA	A register adjusted to a BCD value	C
DECA R	R-1→A	Z
DEC R	R-1→R	Z
DJA R	R-1→A, skip if zero	-
DJ R	R-1→R, skip if zero	-
INCA R	R+1→A	Z
INC R	R+1→R	Z
IJA R	R+1→A, skip if zero	-
IJ R	R+1→R, skip if zero	-
MOV R,A	A→R	-
MOV A,R	R→A	Z
MOV R,R	R→R	Z
OR A,R	A∨VR→A	Z
OR R,A	A∨VR→R	Z
SUB A,R	R-A→A	Z,C,DC
SUB R,A	R-A→R	Z,C,DC
XOR A,R	A⊕R→A	Z
XOR R,A	A⊕R→R	Z
IR R	IOCR→A	-
IW R	A→IOCR	-
CTR	CONT→A	-
CTW	A→CONT	-

BTC R,b	0→R(b)	-

BTS R,b	1→R(b)	-
JBTC R,b	if R(b)=0, skip	-
JBTS R,b	if R(b)=1, skip	-
LCR R	R(n)→R(n+1),R(7)→C, C→R(0)	C
LCA R	R(n)→A(n+1),R(7)→C, C→A(0)	C
RCR R	R(n)→R(n-1),R(0)→C, C→R(7)	C
RCA R	R(n)→A(n-1),R(0)→C, C→A(7)	C
SWAP R	R(0-3) ↔ R(4-7)	-
SWAPA R	R(0-3)→A(4-7),R(4-7)→A(0-3)	-
ADD A,k	A+k→A	Z,C,DC
AND A,k	A&k→A	Z
MOV A,k	k→A	-
OR A,k	A∨k→A	Z
SUB A,k	k-A→A	Z,C,DC
XOR A,k	A⊕k→A	Z
CALL k	PC+1→[SP], (Page,k)→PC	-
DI	Disable interrupt	-
EI	Enable Interrupt	-
JMP k	K (Page,k)→PC	-
NOP	Null instruction	-
RET	[Top of stack]→PC	-
RETI	[Top of stack]→PC, enable interrupt	-
RETL k	k→A,[top of stack]→PC	-
SLEEP	0→WDT, oscillator stops oscillating (sleep mode)	T,P
CWDT	0→WDT	T,P

6 Electrical characteristics

6.1 Limit parameters

Working temperature... -40℃ ~ 85℃
Storage temperature... -65℃ ~ 150℃
The input voltage... Vss-0.3V ~ Vdd+0.5V
The output voltage... Vss-0.3V ~ Vdd+0.5V
Working voltage... 1.8 V to 5.5 V

6.2 DC electrical characteristics

(VDD =5V, operating temperature =25 ° C, unless otherwise stated)

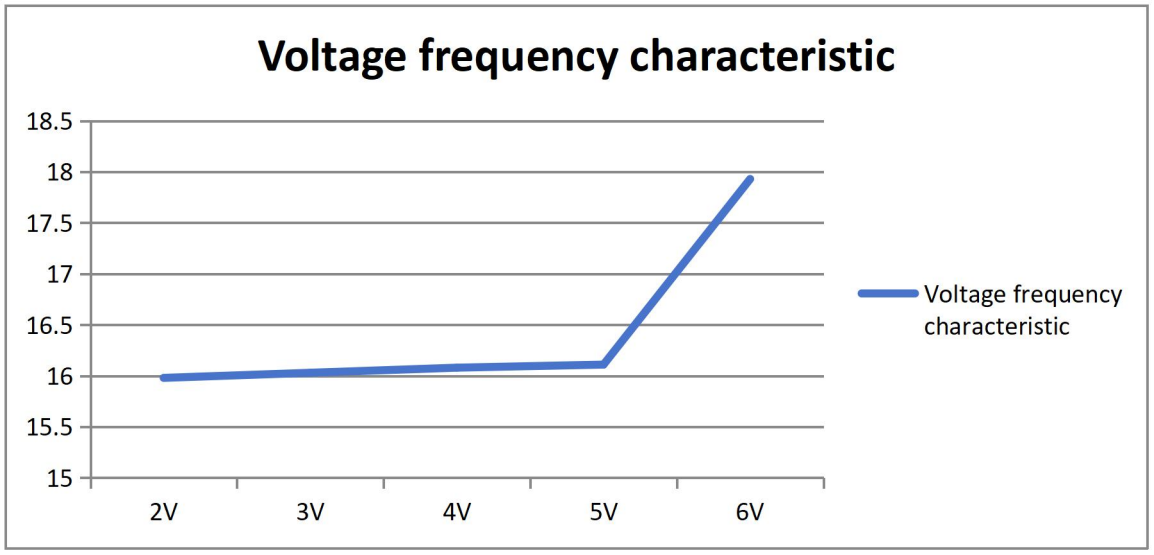
Symbols	Parameter Description	Conditions	Minim	Typical	Max	Units
IRC1	IRC1 (after correction)	OPTION select 8MHz	-	8	-	MHz
IRC2	IRC2 (after correction)	OPTION select 1MHz	-	1	-	MHz
IRC3	IRC3 (corrected)	OPTION select 910KHz	-	910	-	KHz
IOH1	Output high level drive (except P63)	Ioh = 4.4 V	5	5.5	6	mA
IOH2	Output High Level Drive (P63)	Ioh = 4.4 V	6	6.5	7	mA
IOH3	Output high level drive enhancement	Ioh = 4.4 V	12	14	16	mA
IOL1	Output Low drive (normal IO)	Iol = 0.6 V	10	11	12	mA
IOL2	Output Low drive one level	Iol = 0.6 V	19	21	23	mA
IOL3	Output Low-level Drive One Level	Iol = 0.6 V	15	17	19	mA
IOL4	Output Low-level Drive secondary	Iol = 0.6 V	24	26	28	mA
VIL1	Input low		-	-	1.3	V
VIH1	Enter high		2.6	-	-	V
RPH1	Pull-up resistors (except P63)	VDD=5V, GPIO	-	50	-	K Ω
RPH2	Pull-up resistors (except P63)	VDD=3V, GPIO	-	100	-	K Ω
RPH3	Pull-up resistor (P63)	VDD=5V, GPIO	-	40	-	K Ω
RPH4	Pull-up resistor (P63)	VDD=3V, GPIO	-	75	-	K Ω
RPD1	Pull-down resistor	VDD=5V, GPIO to VDD	-	90	-	K Ω
RPD2	Pull-down resistor	VDD=3V, GPIO to VDD	-	166	-	K Ω
Isb1	Shutdown current 1	Input connected to VDD, output suspended, WDT	-	-	1	μA
Isb2	Shutdown current 2	Input connected to VDD, output suspended, WDT	-	-	10	μA
Iop2	Working current 1 (VDD=5V)	IRC=8MHz 2clock	-	1.2	1.5	mA
Iop2	Working current 2 (VDD=5V)	IRC=910KHz 2clock	-	0.2	0.3	mA
LVR	Low voltage reset voltage	Select the LVR reset	Vlvr -	Vlvr	Vlvr +	V

6.3 Feature graph

The curves listed in this chapter are for design reference only, and some of the data given may exceed the specified working range of the chip. To ensure the normal operation of the chip, please strictly refer to the electrical characteristics

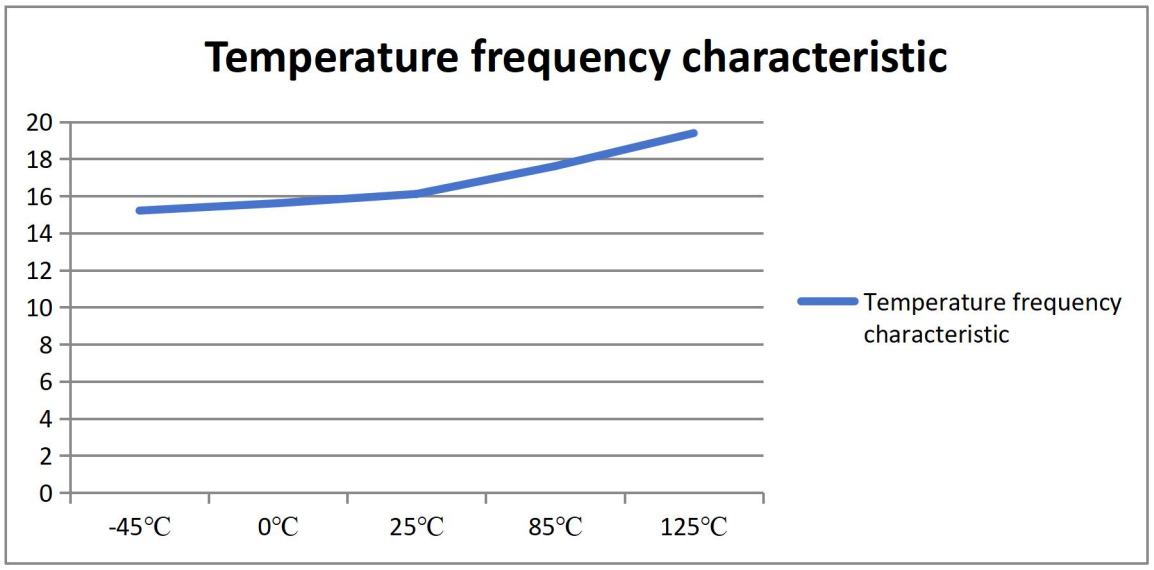
6.3.1 Internal Low speed RC oscillator - voltage frequency characteristic curve

Operating temperature at 25℃ : (unit KHz)



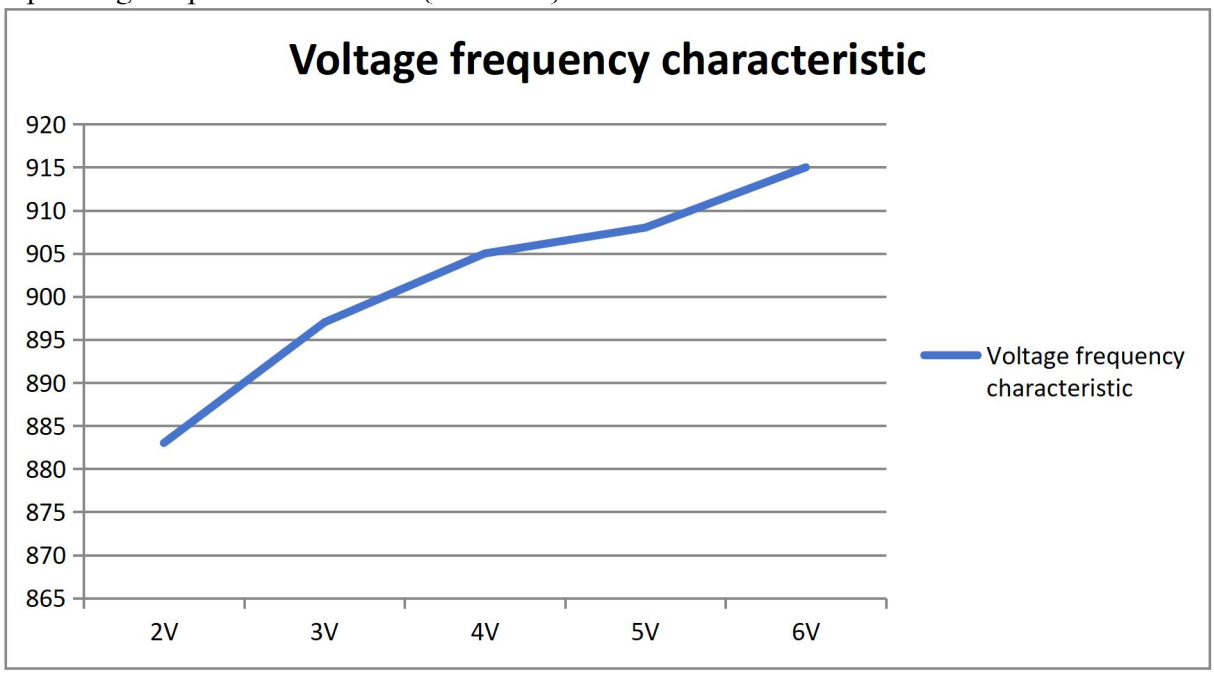
6.3.2 Internal low speed RC oscillator - temperature frequency characteristic curve

Operating voltage under 5V condition: (unit KHz)



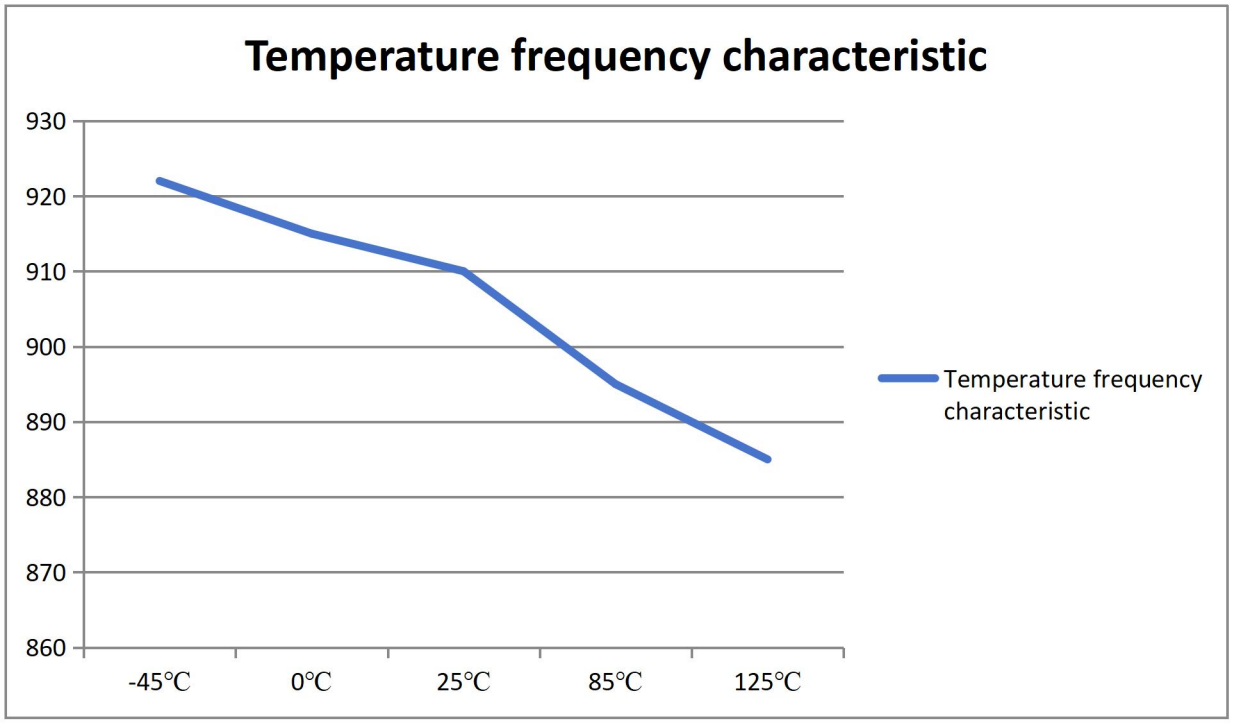
6.3.3 Internal 910KHz RC oscillator - voltage frequency characteristic curve

Operating temperature at 25℃ : (unit KHz)



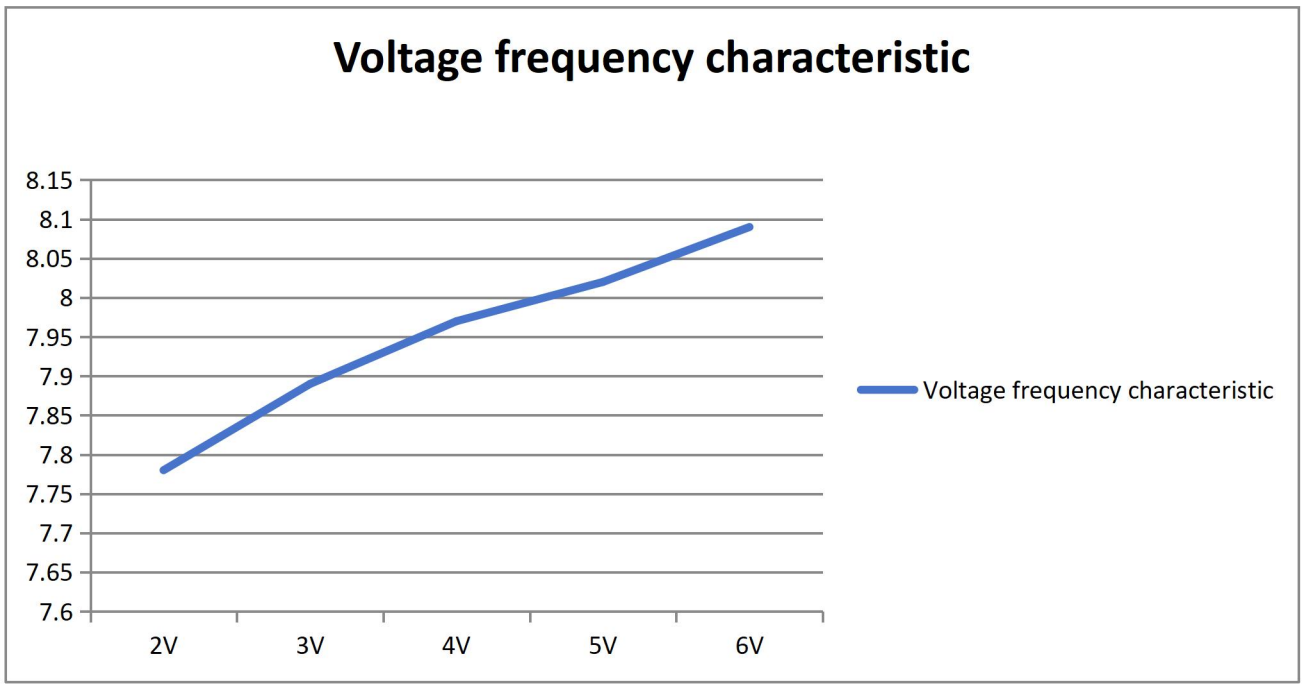
6.3.4 Internal 910KHz RC oscillator - temperature frequency characteristic curve

Operating voltage under 5V condition: (unit KHz)



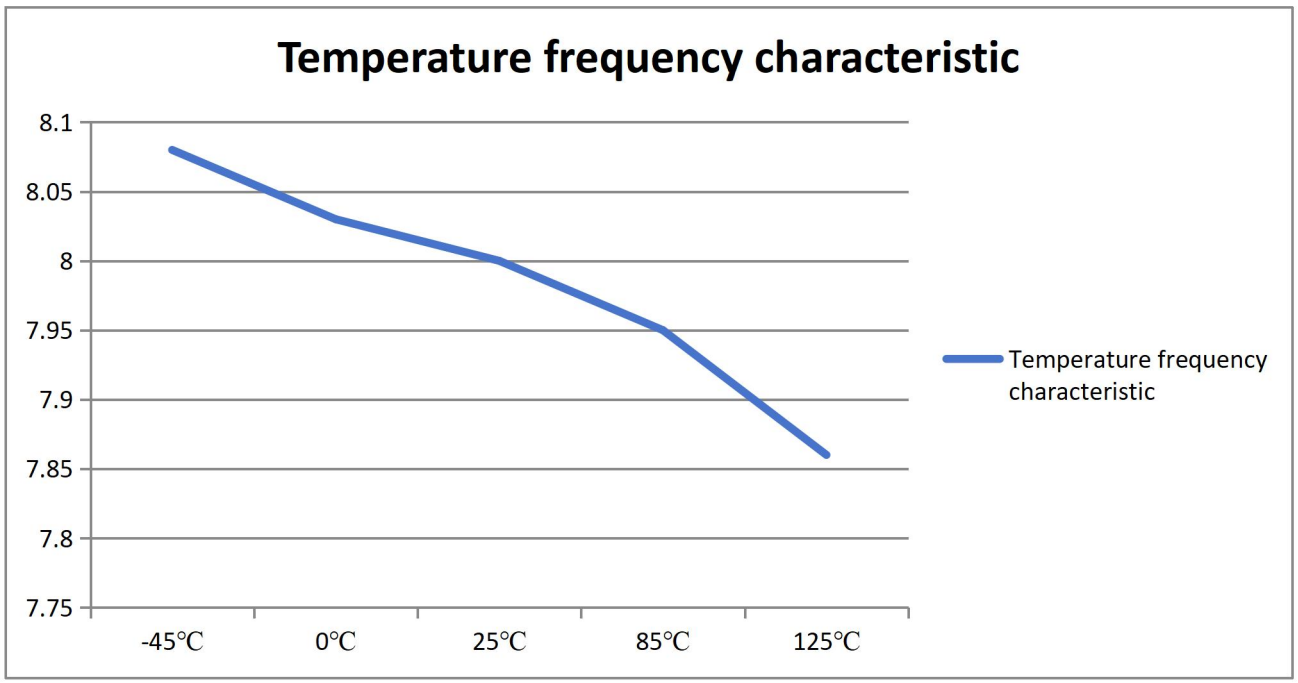
6.3.5 Internal 8MHz RC oscillator - voltage frequency characteristic curve

Operating temperature at 25℃ : (unit Mhz)



6.3.6 Internal 8MHz RC oscillator - temperature frequency characteristic curve

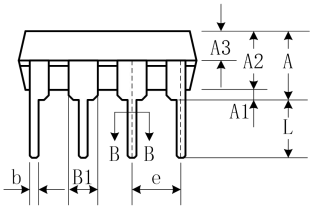
Operating voltage under 5V condition: (unit Mhz)

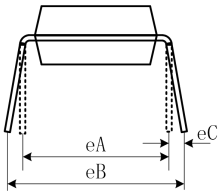


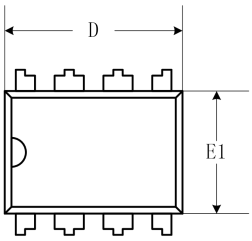
7 Package size

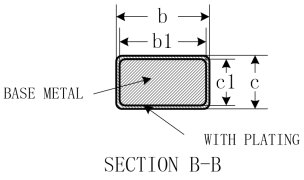
7.1 8PIN package size

DIP8



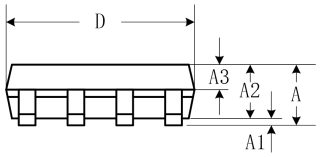


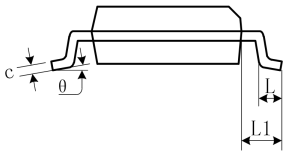


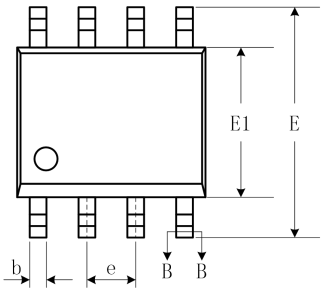


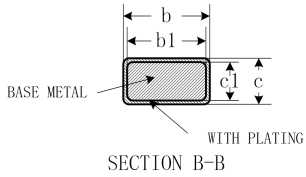
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	-	-
A2	3.10	3.30	3.50
A3	1.50	1.60	1.70
b	0.44	-	0.53
b1	0.43	0.46	0.48
B1	1.52 BSC		
c	0.25	-	0.31
c1	0.24	0.25	0.26
D	9.05	9.25	9.45
E1	6.15	6.35	6.55
e	2.54 BSC		
eA	7.62 BSC		
eB	7.62	-	9.50
eC	0	-	0.94
L	3.00	-	-

SOP8



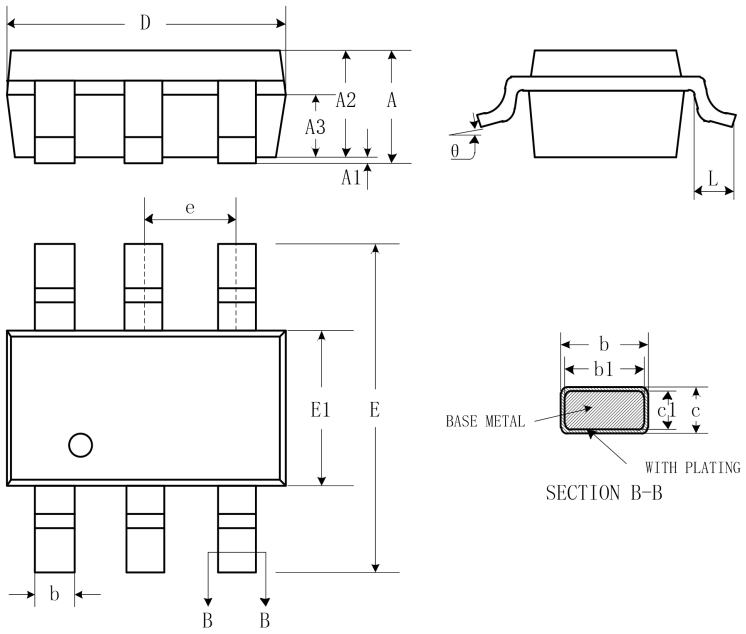






SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
L	0.50	0.65	0.80
L1	1.05 BSC		
Theta.	0	-	8 °

7.2 6PIN package size



Package specifications:

Symbol	mm			Inch		
	MIN	NOM	MAX	MIN	NOR	MAX
A	-	-	1.35	-	-	0.053
A1	0.04	-	0.15	0.002	-	0.006
A2	1.00	1.10	1.20	0.039	0.043	0.047
A3	0.55	0.65	0.75	0.022	0.026	0.030
b	0.30	-	0.50	0.013	-	0.017
b1	0.30	0.40	0.45	0.013	0.016	0.018
c	0.08	-	0.22	0.006	-	0.008
c1	0.08	0.13	0.20	0.003	0.005	0.08
D	2.72	2.92	3.12	0.107	0.115	0.123
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95 BSC			0.037 BSC		
L	0.30	-	0.60	0.012	-	0.024
Theta.	0	-	8 DHS	0	-	8 DHS