JZ8PT2503/4

8-bit OTP microcontroller

User Data Manual

Version V1.1

Modification Record Description

Version Number	Modification Description	Remarks
V1.0	Initial Release	
V1.1	Added JZ8PT2504 pin description	
V1.2	Correct the pin numbers on the foot diagram.	

Notes:

1. It is recommended to use pin P63 (VPP) as an output;

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1. Chip Introduction

1.1 Functional Features

CPU Configuration

- 2K×16-Bit OTP ROM
- 128×8-Bit SRAM
- 8-level stack space
- 8-level programmable voltage reset (LVR)
  1.8V, 2.0V, 2.2V, 2.4V
  2.7V, 3.0V, 3.3V, 3.6V
- Operating current < 2 mA (4MHz/5V)
- Operating current <10 uA (40KHz/5V)
- Sleep current < 1 uA (sleep mode)

I/O configuration

- 2 sets of bidirectional IO ports: P5, P6
- Wake-up ports: P5, P6
- 14 programmable pull-up I/O pins
- 14 programmable pull-down I/O pins
- External Interrupt:
  INT0: P60 INT1: P63
- Reference Voltage Output: P65

Operating Voltage

- Operating Voltage Range:
  V_{LVR}2.2V～5.5V|Fcpu=0～8MHz
  V_{LVR}1.8V～5.5V|Fcpu=0～2MHz

Operating Frequency Range

- Internal IHRC Oscillation Circuit:
  16MHz/8MHz/4MHz/1MHz
- Internal ILRC Oscillation Circuit:
  40KHz(5V)/39.5KHz(3V)
- Clock cycle division selection:
  2T, 4T, 8T, 16T, 32T

Peripheral modules

- 8-bit counter TC0 with capture function
- 6 channels, 2 groups of 12-bit PWM with dead zone complementary
- 12-channel CDC (Capacitive Digital Converter)
- 1 comparator CMP
- 2-channel RGB LED cascade controller (driving colorful lights)

Interrupt sources

- TC0 Overflow Interrupt
- External Interrupt 1
- External Interrupt 0
- P6 Port Input Change Interrupt
- P5 Port Input Change Interrupt
- PWM1 Period Match/TC1 Timer Interrupt
- PWM4 Period Match/TC2 Timer Interrupt
- PWM2 Duty Cycle Match Interrupt
- CMP Comparison Result Change Interrupt
- TK Detection End Interrupt

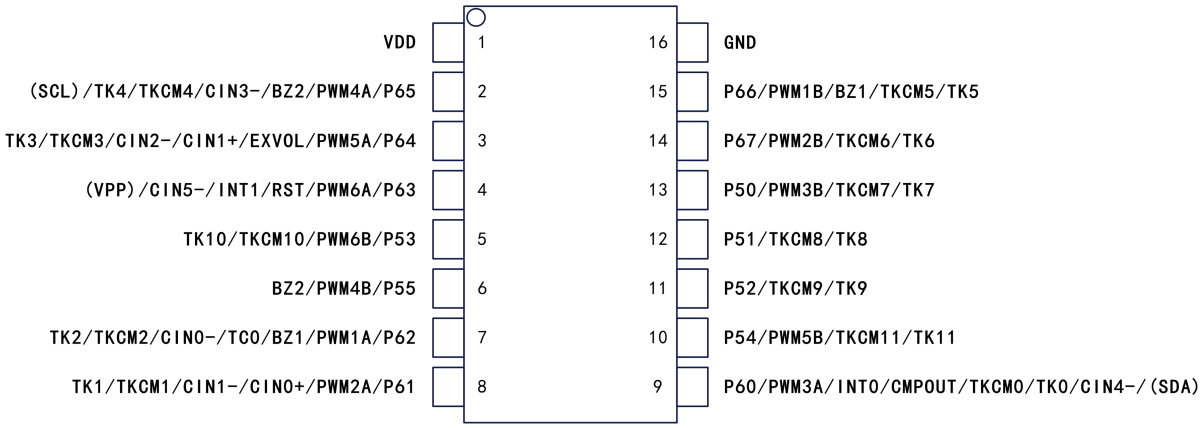
Characteristics

- Programmable WDT Timer
- Four working mode switches

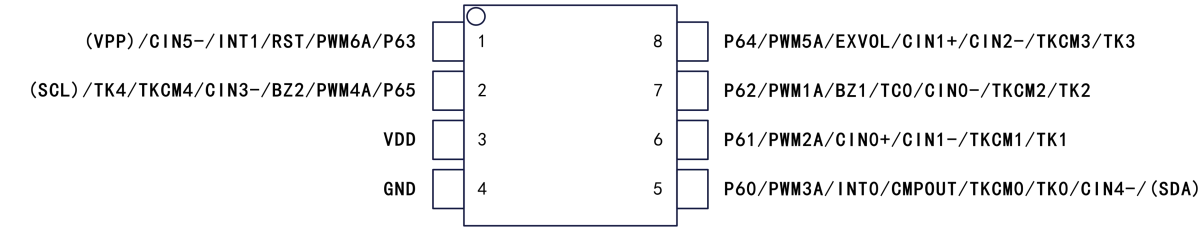
Package type

- JZ8PT2503-SOP16
- JZ8PT2503-SOP8
- JZ8PT2504-SOP16
- JZ8PT2504-SOP8

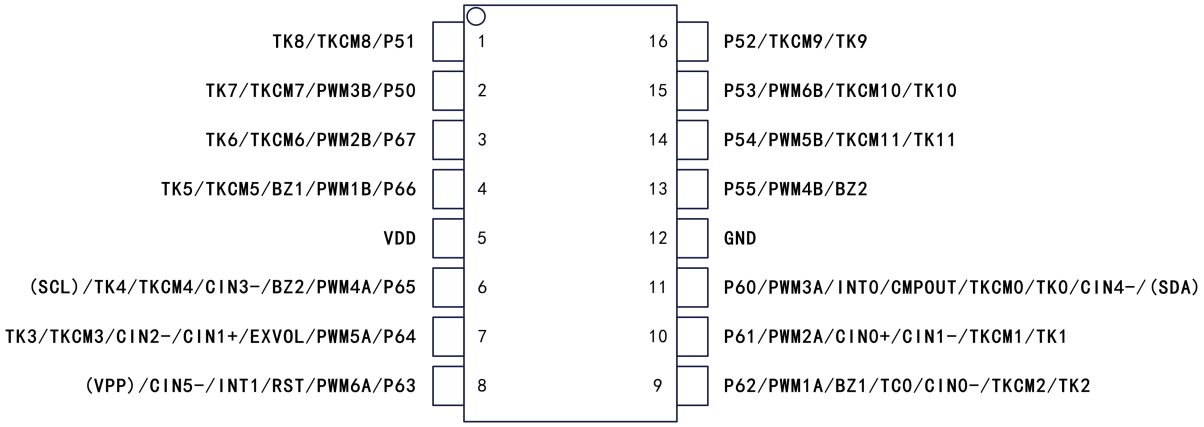
1.2 Pin assignment



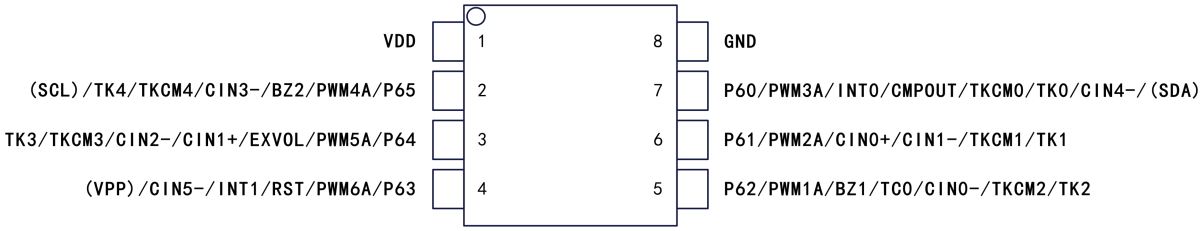
JZ8PT2503-16 pin diagram



JZ8PT2503-8 pin diagram



JZ8PT2504-16 Pinout Diagram



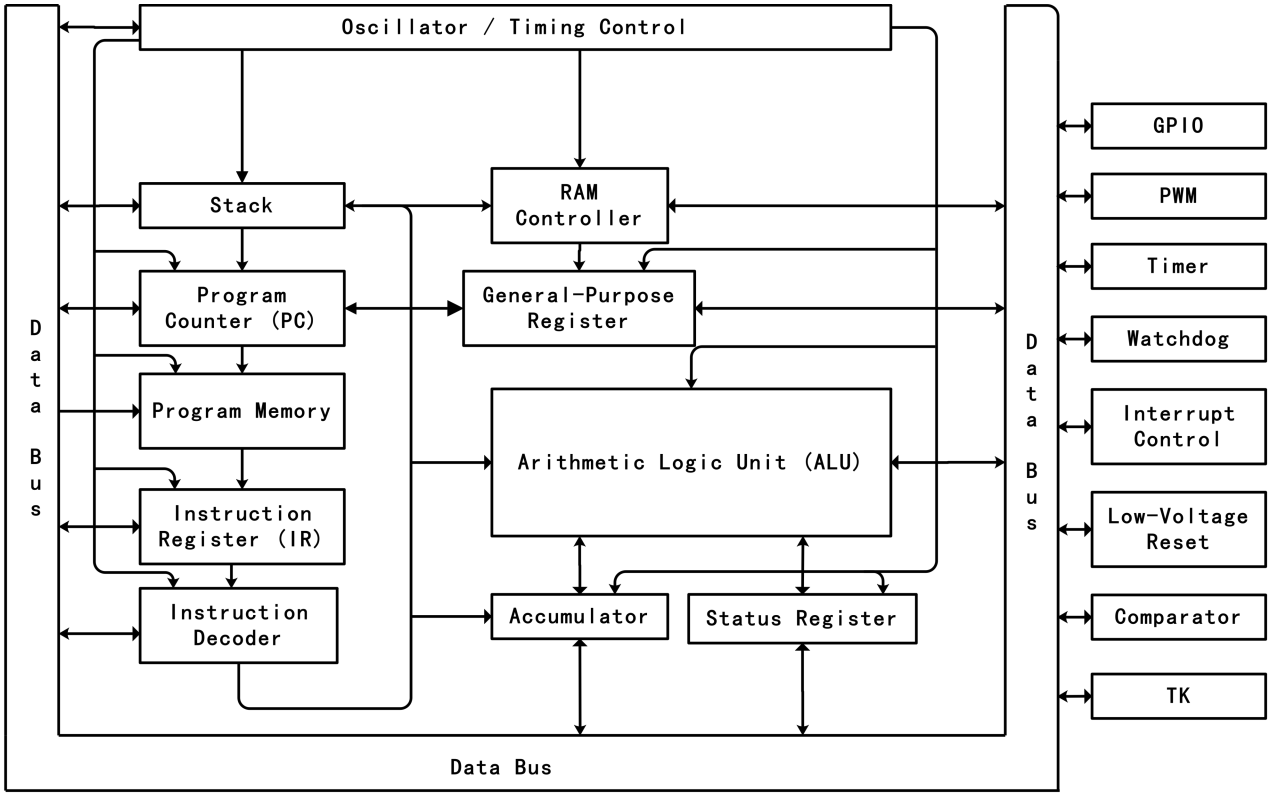
JZ8PT2504-8 Pinout Diagram

1.3 Pin Description

Number	Pin Name	I/O	Function Description
P50	P50	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM3B	O	PWM3B output
	TKCM7	I/O	TK Touch COM Port
	TK7	I	TK Touch Channel
P51	P51	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	TKCM8	I/O	TK Touch COM Port
	TK8	I	TK Touch Channel
P52	P52	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	TKCM9	I/O	TK Touch COM Port
	TK9	I	TK Touch Channel
P53	P53	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM6B	O	PWM6B output
	TKCM10	I/O	TK Touch COM Port
	TK10	I	TK Touch Channel
P54	P54	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM5B	O	PWM5B output
	TKCM11	I/O	TK Touch COM Port
	TK11	I	TK Touch Channel
P55	P55	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM4B	O	PWM4B output
	BZ2	O	BZ2 buzzer output
P60	P60	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM3A	O	PWM3A output
	INT0	I	External interrupt INT0 input port
	CMPOUT	O	Comparator result output
	TCKM0	I/O	TK Touch COM Port
	TK0	I	TK Touch Channel
	CIN4-	I	Comparator negative input port
	SDA	I	Programming data port
P61	P61	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM2A	O	PWM2A output
	CIN0+	I	Comparator positive input port
	CIN1-	I	Comparator negative input port
	TKCM1	I/O	TK Touch COM Port
	TK1	I	TK Touch Channel

P62	P62	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM1A	O	PWM1A output
	BZ1	O	BZ1 buzzer output
	TCO	I	TCO external clock input port
	CINO-	I	Comparator negative input port
	TKCM2	I/O	TK Touch COM Port
	TK2	I	TK Touch Channel
P63	P63	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM6A	O	PWM6A output
	RST	I	external reset input port
	INT1	I	External interrupt INT1 input port
	CIN5-	I	Comparator negative input port
	VPP	I	Programming high voltage port
P64	P64	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM5A	O	PWM5A output
	EXVOL	I	CMP resistor voltage divider input port
	CIN1+	I	CMP positive input source
	CIN2-	I	CMP negative input source
	TKCM3	I/O	TK Touch COM Port
	TK3	I	TK Touch Channel
P65	P65	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM4A	O	PWM4A output
	BZ2	O	BZ2 buzzer output
	CIN3-	I	CMP negative input source
	TKCM4	I/O	TK Touch COM Port
	TK4	I	TK Touch Channel
	SCL	I	Burning clock port
P66	P66	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM1B	O	PWM1B output
	BZ1	O	BZ1 buzzer output
	TKCM5	I/O	TK Touch COM Port
	TK5	I	TK Touch Channel
P67	P67	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	PWM2B	O	PWM2B output
	TKCM6	I/O	TK Touch COM Port
	TK6	I	TK Touch Channel
	VDD	--	Power Supply
	GND	--	Ground

1.4 System Block Diagram



System Circuit Block Diagram

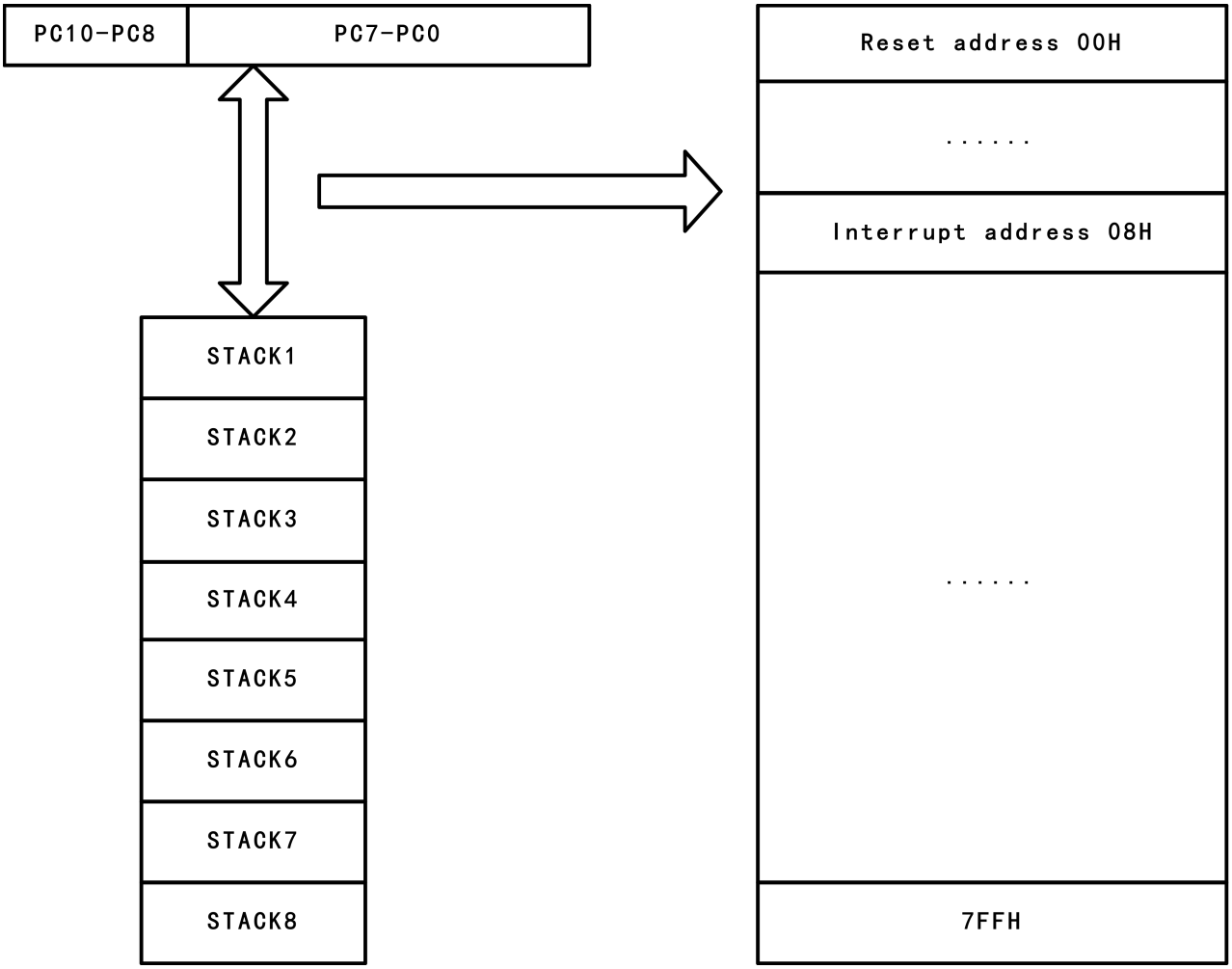
2. Central Processing Unit

2.1 Program Storage Area and Stack

OTP: 2K, ROM address range 00H - 7FFH

Interrupt address: 08H

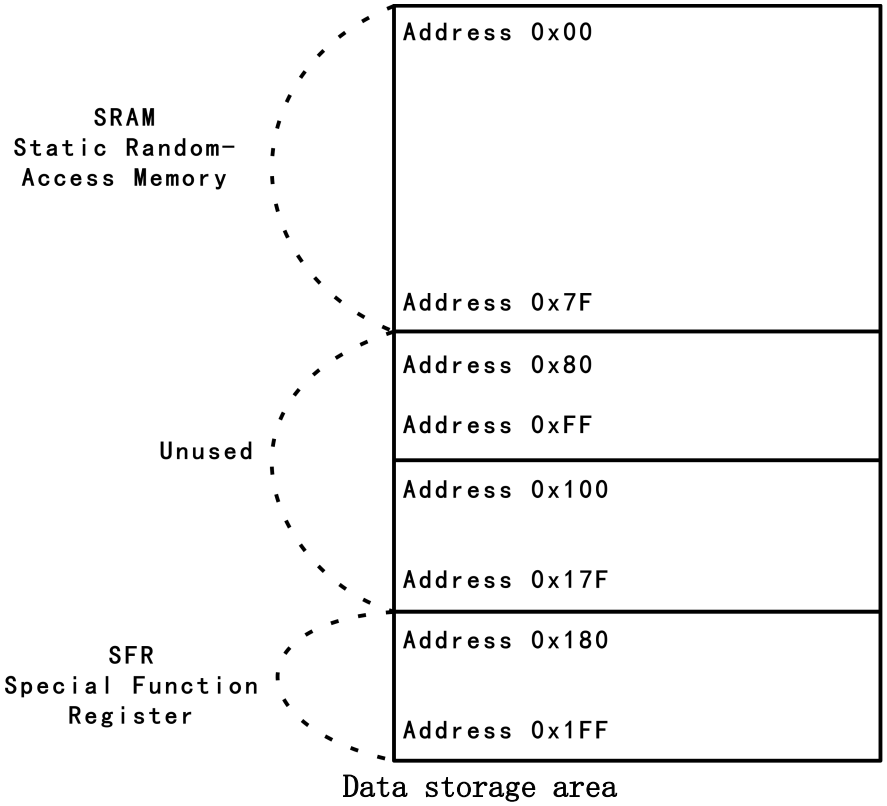
Stack: 8 levels



Program storage area structure diagram

2.2 Data storage area

2.2.1 Data storage area structure



2.2.2 Overview of special function registers

Address	0X18_	0X19_	0X1A_	0X1B_	0X1C_	0X1D_	0X1E_	0X1F_
0	RSR	P5PH		TC1CON	TKCON0			
1	PCH	P6PH	P6AE	TC1PRDL	TKCON1			
2	PCL			PWM1DTL	TKCHS0			
3	STATUS	P5PD		PWM2DTL	TKCHS1			
4	TC0CON	P6PD		PWM3DTL	TKVS			
5	TC0C			TC1PRDTH	TKCNTH			
6	TBRDH			PWM12DTH	TKCNTL	INTE0		
7	TBRDL			PWMCON1	TKVCNTH	INTE1		
8	CPUCON			TC2CON	TKVCNTL			
9	IHRCCAL			TC2PRDL	CMPCON0			
A(10)	PORT5			PWM4DTL	CMPCON1	INTF0		
B(11)	PORT6			PWM5DTL		INTF1		
C(12)		P5IWE	VREFCAL	PWM6DTL				
D (13)	P5CON	P6IWE	TPRE	TC2PRDTH				
E (14)	P6CON		EXINTCON	PWM45DTH				
F(15)			WDTCON	PWMCON2				IAR

2.3 Special System Register

2.3.1 Indirect Addressing

Data memory can be addressed directly or indirectly, and indirect addressing operations can be performed through the IAR register.

The RSR register is used in conjunction with the IAR register to implement indirect addressing operations. Users can place the address corresponding to a certain register into the RSR, and then by accessing the indirect addressing register IAR, the address will point to the register corresponding to the address in the RSR.

IAR is not a physically existing register; its main function is to serve as a pointer for indirect addressing. Any instruction that uses R1FF (IAR) as a pointer actually corresponds to the data pointed to by R180 (RAM selection register) RSR<7:0>.

Example: Indirect Addressing Clear RAM (0x00～0x7F)

```
MOV    A,@0X00
MOV    RSR,A      // The indirect addressing pointer points to 00H
CLR    IAR        // Clear the data pointed to by the address 00H
INC    RSR        // Address +1
MOV    A,RSR
XOR    A,@0X7F
JBTS   STATUS,2
JMP    $-5        // Go back 5 instructions, continuously clear until RSR
                      points to 7FH
CLR    0X7F       // Clear the data pointed to by the address 7FH
```

2.3.1.1 R180/RSR (RAM Selection Register)

0X180	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSR	-	RSR<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	X	X	X	X	X	X	X

RSR<7:0> is used to select the RAM register address in indirect addressing mode (addressing range: 0X00～0X7F).

2.3.1.2 R1FF/IAR (Indirect Addressing Register)

0X1FF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAR	IAR<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

The indirect addressing register does not actually exist as a physical register.

2.3.2 Lookup Table

2.3.2.1 Jump Table

The program register PC controls the execution order of program instructions and can address the entire ROM range. The PC increments by 1 after executing an instruction, always pointing to the address of the next instruction. When performing operations such as jumps, conditional jumps, PCL assignments, subroutine calls, interrupt triggers, and returns, the PC automatically loads the address related to the instruction instead of the address of the next instruction.

The jump table can achieve multi-address jump functionality, where the new PCL value is obtained by adding the value to PCL for multi-address jumps. For example, if ACC=1, it indicates that the current address is PCL+1. It is important to note that jumps should not exceed the range to avoid functional anomalies.

Example 1: Jump table returns the value 0X4F

```
MOV     A,@0X03
ADD     PCL,A
RETL    @0X3F   //0
RETL    @0X06   //1
RETL    @0X5B   //2
RETL    @0X4F   //3
RETL    @0X66   //4
```

Example 2: Jump to program LOOP2

```
MOV     A,@0X02
ADD     PCL,A
JMP     LOOP0   //0
JMP     LOOP1   //1
JMP     LOOP2   //2
JMP     LOOP3   //3
```

2.3.2.2 R181/PCH (Program Counter High Register)

0X181	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCH	-	-	-	-	-	PC<10:8>		
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

2.3.2.3 R182/PCL (Program Counter Low Register)

0X182	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCL	PC<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

The Program Counter (PC) is a pointer used to record the instruction that the CPU needs to process during each instruction cycle. During the CPU's operation cycle, the PC advances the instruction pointer to the program memory, and then the pointer increments by 1 to enter the next cycle. The JZ8PT2503/4 has an 11-bit wide Program Counter (PC), with its low byte coming from the readable and writable PCL register and the high byte coming from the readable PCH register.

The stack is used to record the instruction pointer for returning to the program. When a subroutine is called, the PC pushes the instruction pointer onto the stack. When the return instruction is to be executed, the stack sends the instruction pointer back to the PC to continue the original process. The JZ8PT2503/4 has an 8-level stack that occupies neither program storage space nor data storage space, and the stack pointer cannot be read or written.

Details of the Program Counter (PC) and stack are as follows:

(1) The PC register and the built-in 8-level stack are both 11 bits wide, used for addressing 2K×16Bit OTP ROM.

(2) Generally, the PC increments by one; during reset, all bits of the PC are cleared to zero.

(3) The instruction "JMP" allows for directly loading an 11-bit address, then pushing PC+1 onto the stack. Therefore, the JMP instruction allows the PC to jump to any location in the program.

(4) The instruction "CALL" allows for loading the 11-bit address of the PC, then pushing PC+1 onto the stack. Therefore, the entry address of the subroutine can be located at any position in the program.

(5) Executing the "RET" instruction will send the top data of the stack to the PC.

(6) Executing the "ADD PCL,A" instruction can add a relative address to the current PC, incrementing the ninth bit and above of the PC successively.

(7) Executing the "MOV PCL, A" instruction loads an address from the "A" register into the low 8 bits of the PC, while the ninth bit and above of the PC remain unchanged.

(8) Any instruction that writes a value to PCL (except for the "ADD PCL,A" instruction) (for example, "MOV PCL,A", "BTC PCL,1") will keep the ninth and tenth bits of the PC unchanged.

(9) Any instruction other than "TBRD R" is a single instruction cycle.

(10) The stack operates like a circular buffer, meaning that after pushing onto the stack 8 times, the data pushed during the 9th push will overwrite the data from

the 1st push, and the data pushed during the 10th push will overwrite the data from the 2nd push, and so on.

2.3.2.4 ROM area lookup

The TBRDH and TBRDL registers can be used with the TBRD instruction to query data from the ROM area address. The high 8 bits of the queried data are stored in a custom register, while the low 8 bits are stored in ACC.

Example: The 16-bit data queried from ROM address 0XF5 is 0X55D6

```
        MOV     A,@0x00
        MOV     TBRDH,A
        MOV     A,@0xF5
        MOV     TBRDL,A
        TBRD    reg_tempH           // The high 8 bits are saved to reg_tempH, and the
                                       low 8 bits are saved to ACC
        MOV     reg_tempL,A         // The ACC value is saved to reg_tempL
Table:
        ORG     0X0F0               // The fixed ROM program starting address is 0X0F0
        DW      0X00F3      // 0
        DW      0X1103      // 1
        DW      0X22BC      // 2
        DW      0X339E      // 3
        DW      0X444E      // 4
        DW      0X55D6      // 5
```

2.3.2.5 R186/TBRDH (Table Pointer High Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	-	-	-	-	-	RBIT<10:8>		
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<2:0>: RBIT<10:8>-TBRD pointer address high 3 bits.

2.3.2.6 R187/TBRDL (Table Pointer Low Register)

0X187	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDL	RBIT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: RBIT<7:0>-TBRD pointer address low 8 bits, RBIT<7:0> is used to select the low 8 bits of the table ROM address in table mode.

2.3.3 Program Status Register

The STATUS register can be the target register for any instruction. If any instruction that affects the Z, DC, or C bits uses the STATUS register as the target register, then these 3 status bits cannot be written. These bits are set to 1 or cleared based on the device logic. VOUTEN enables the output of the internal LDO reference voltage, which can be used as a reference but is not recommended for driving large loads. All other bits are read-only flags; the program can only read them and cannot manipulate them.

2.3.3.1 R183/STATUS (Status Flag Register)

0X183	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	RST	GIE	VOUTEN	T	P	Z	DC	C
Read/Write	R	R	R/W	R	R	R/W	R/W	R/W
Reset Value	0	0	0	1	1	X	X	X

Bit<7>: RST - Reset or wake-up flag

0: Other reset types

1: Wake-up triggered by pin state change

Bit<6>: GIE - Interrupt enable flag

0: Masked by DIT instruction or hardware interrupt

1: Interrupt enabled by EIT/RTI instruction

Bit<5>: VOUTEN - Internal reference voltage output enable

0: Disabled

1: Enabled, P65 port output (the port needs to be set as analog input)

Bit<4>: T-Time Overflow Bit

0: WDT Overflow

1: Execute "SLEEP" and "CWDT" instructions or low voltage reset

Bit<3>: P-Power Down Flag Bit

0: Execute "SLEEP" instruction

1: Power-on reset or execute "CWDT" instruction

The events affecting T/P are shown in the table below:

Type	RST	T	P
Power-on reset	0	1	1
Press RESET in working mode	0	Hold	Hold
RESET wakeup	0	1	0
WDT overflow in working mode	0	0	Hold
WDT overflow wakeup	0	0	0
Port input change wakeup	1	1	0
Execute CWDT instruction	Hold	1	1
Execute SLEEP instruction	Hold	1	0

Bit<2>: Set to "1" when the arithmetic or logical operation result of the Z-zero flag is zero

0: When the result of arithmetic or logical operations is not 0

1: When the result of arithmetic or logical operations is 0

Bit<1>: DC-carry flag

0: When performing addition, there is no carry generated in the low four bits; / When performing subtraction, a borrow is generated in the low four bits

1: When performing addition, a carry is generated in the low four bits; / When performing subtraction, no borrow is generated in the low four bits

Bit<0>: C-carry flag

0: When performing addition, there is no carry generated in the high four bits; / When performing subtraction, a borrow is generated in the high four bits

1: When performing addition, a carry is generated in the high four bits; / When performing subtraction, no borrow is generated in the high four bits

3. I/O ports

JZ8PT2503/4 has 2 sets of bidirectional I/O ports, with a total of 14 inputs and 14 outputs, most of which can be reused for other functions.

14 programmable pull-up I/O pins: P50 to P55, P60 to P67;

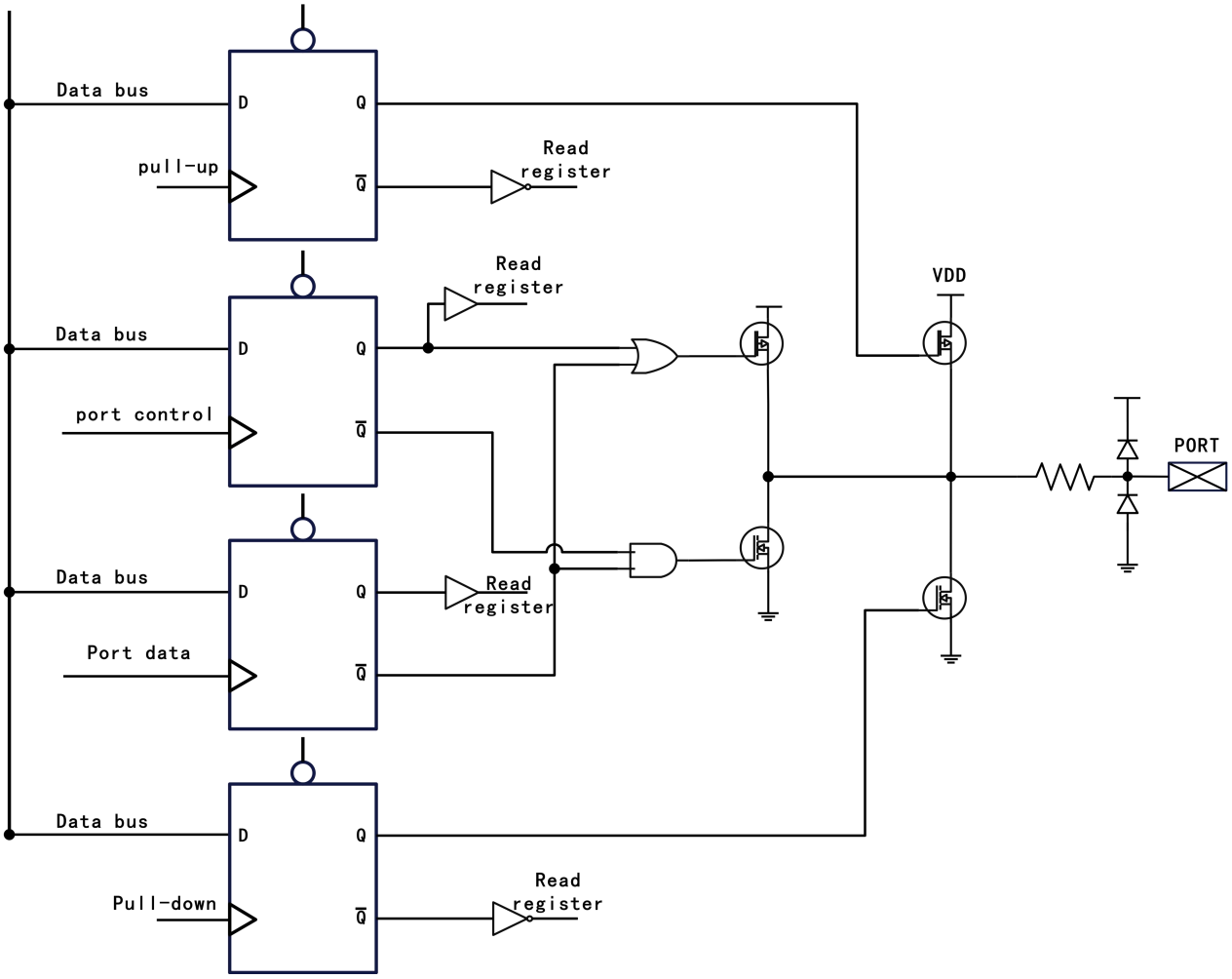
14 programmable I/O pins: P50 to P55, P60 to P67;

14 programmable wake-up I/O pins: P50 to P55, P60 to P67;

6 programmable analog ports: P60 to P65;

3.1 GPIO internal structure diagram

The following internal structure diagram is for reference only and does not represent the actual circuit.



IO control register/data register/pull-up/pull-down structure circuit

3.2 P5 port

The P5 port is a 6-bit wide bidirectional port. The corresponding direction control register is P5CON. Setting a bit in P5CON to 1 (=1) configures the corresponding pin as an input. Clearing a bit in P5CON to 0 (=0) configures the corresponding P5 pin as an output.

The data register corresponding to the P5 port is PORT5. When the port is configured as an input, reading the PORT5 register reads the state of the pins; when the port is configured as an output, reading the PORT5 register reads the data of P5.

Registers related to the P5 port include PORT5, P5CON, P5PH, P5PD, P5IWE, etc.

3.2.1 R18A/PORT5(P5 Data Register)

0X18A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORT5	-	-	P5<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 port data control

3.2.2 R18D/P5CON (P5 control register)

0X18D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5CON	-	-	P5CON<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port input/output control bits:

0: Output

1: Input

3.2.3 R190/P5PH (P5 pull-up control register)

0X190	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PH	-	-	P5PH<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port pull-up control bits:

0: Enable

1: Disable

3.2.4 R193/P5PD (P5 pull-down control register)

0X193	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PD	-	-	P5PD<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port pull-down control bits:

0: Enable

1: Disable

3.2.5 R19C/P5IWE (P5 input change interrupt, wake-up enable register)

0X19C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5IWE	-	-	P5IWE<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 port input change wake-up control bit:

0: Disable

1: Enable

3.3 P6 port

P6 port is an 8-bit wide bidirectional port. The corresponding direction control register is P6CON. Setting a bit in P6CON to 1 (=1) can configure the corresponding pin as input. Clearing a bit in P6CON to 0 (=0) can configure the corresponding P6 pin as output.

The data register corresponding to the P6 port is PORT6. When the port is configured as an input port, reading the PORT6 register reads the state of the pins; when the port is configured as an output port, reading the PORT6 register reads the data of the P6 port.

Registers related to the P6 port include PORT6, P6CON, P6PH, P6PD, P6IWE, etc.

3.3.1 R18B/PORT6 (P6 data register)

0X18B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORT6	P6<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 port data control

3.3.2 R18E/P6CON (P6 control register)

0X18E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6CON	P6CON<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port input/output control bits:

0: Output

1: Input

3.3.3 R191/P6PH (P6 pull-up control register)

0X191	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PH	P6PH<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port pull-up control bits:

0: Enable

1: Disable

3.3.4 R194/P6PD (P6 Pull-Down Control Register)

0X194	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PD	P6PD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port pull-down control bit:

0: Enable

1: Disable

3.3.5 R19D/P6IWE (P6 input change interrupt, wake-up enable register)

0X19D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6IWE	P6IWE <7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 port input change wake-up control bit:

0: Disable

1: Enable

3.3.6 R1A1/P6AE (P6 analog port enable register)

0X1A1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6AE	-	TKOSC_OUT	P6AE <5:0>					
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R /W
Reset Value	0	0	0	0	0	0	0	0

Bit<5:0>: P6AE<5:0>-P6 port analog channel selection control bit:

0: Port set to GPIO

1: Port set to analog input

3.4 Port input change wakeup

JZ8PT2503/4 includes 14 programmable port input change wakeup I/O: P50～P55, P60～P67. The chip can enter sleep mode or idle mode by executing the "SLEEP" instruction. At this time, the CPU does not execute instructions. Port input change wakeup can continue the original process (execute DI before SLEEP) or perform the corresponding jump (execute EI before SLEEP) through program selection, and the corresponding interrupt enable control must be turned on. After port input change wakeup, it jumps to the interrupt service routine.

Port state change query method wakeup setting:

1. Set the port input change wakeup pin as input;
2. You can choose the internal pull-up or pull-down for the wake-up pin as needed.
3. Enable port input change to wake control P5IWE/P6IWE;
4. Execute the DI instruction without entering the interrupt address port;
5. Execute the "SLEEP" instruction, IDLE=0 to enter sleep mode or IDLE=1 to enter idle mode;
6. After waking up, execute the next instruction after SLEEP;

Port state change interrupt wake-up settings:

1. Set the port input change wakeup pin as input;
2. You can choose the internal pull-up or pull-down for the wake-up pin as needed.
3. Enable port input change to wake control P5IWE/P6IWE;
4. Enable port input change interrupt P5ICIE/P6ICIE;
5. Execute the "EI" instruction and wait to enter the interrupt address port;
6. Execute the "SLEEP" instruction, IDLE=0 to enter sleep mode or IDLE=1 to enter idle mode;
7. After waking up, it will enter the interrupt address port, and after exiting the interrupt, execute the next instruction after SLEEP;

3.5 Port Schmitt parameters

The Schmitt characteristics of the JZ8PT2503/4 ports are as follows (for reference only):

Port	SMT	
P50～P55	0.22*VDD	0.54*VDD
P60～P67	0.22*VDD	0.54*VDD

The above parameters are for reference only; please refer to the actual measured data of the target prototype.

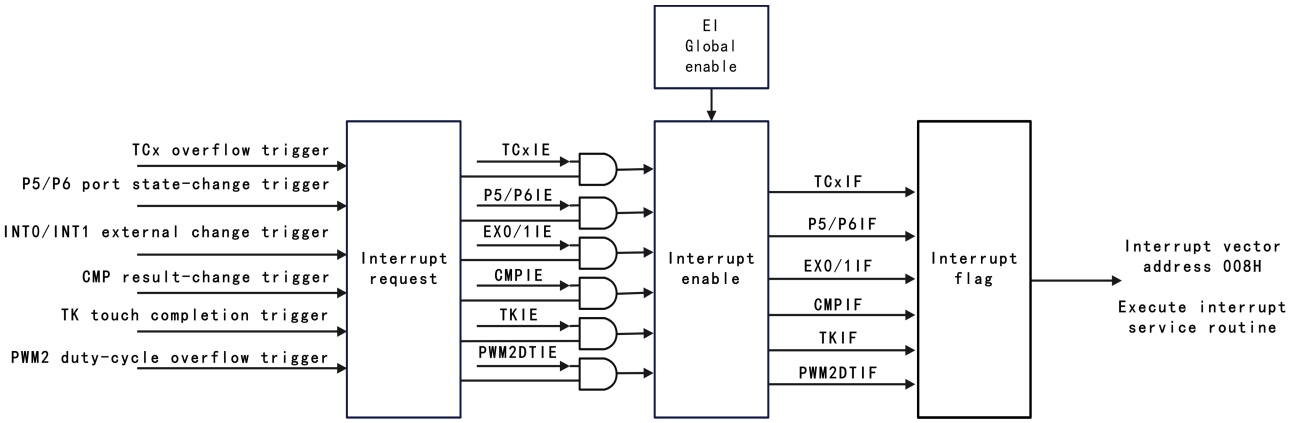
4. Interrupt

4.1 Overview of Interrupts

JZ8PT2503/4 has 10 interrupt sources. Regardless of which interrupt is used, the global interrupt must be enabled, that is, the "EI" instruction. The interrupt vector address is fixed at 008H. Below are the characteristics of each interrupt:

Interrupt sources	Enable Conditions	Interrupt Flag
TC0 Overflow Interrupt	EI + TC0IE=1	TC0IF
TC1 Overflow Interrupt	EI + TC1IE=1	TC1IF
TC2 Overflow Interrupt	EI + TC2IE=1	TC2IF
External Interrupt INT0	EI + INT0IE=1	INT0IF
External Interrupt INT1	EI + INT1IE=1	INT1IF
Port P5 Input Change Interrupt	EI + P5ICIE=1	P5ICIF
P6 port input change interrupt	EI + P6ICIE=1	P6ICIF
CMP comparison complete interrupt	EI + CMPIE=1	CMPIF
PWM2 duty cycle overflow interrupt	EI + PWM2DTIE=1	PWM2DTIF
TK detection complete interrupt	EI + TKIF=1	TKIF

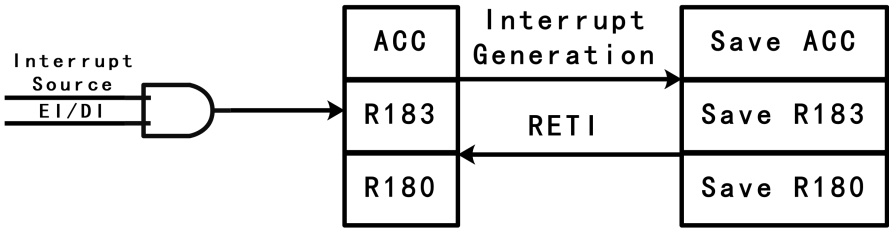
R1DA/R1DB are interrupt flag registers that record the interrupt flag bits after an interrupt request is generated. R1D6/R1D7 are interrupt enable control registers, where the permission and prohibition of interrupts are set in these two registers. The overall interrupt enable is set by the "EI" instruction, while the overall interrupt prohibition is set by the "DI" instruction. When an interrupt occurs, the execution of the next instruction will start from the interrupt vector address 008H. Before exiting the interrupt service routine, the corresponding interrupt flag bits must be cleared to avoid erroneous interrupt actions.



Interrupt Principle Schematic

4.2 Interrupt Context Protection

During the interrupt response process, the hardware has a built-in interrupt protection function that saves the contents of ACC, R183, and R180 until the interrupt service routine is exited, at which point the saved values are reloaded into ACC, R183, and R180. This is to prevent any instructions from changing the values of ACC, R183, and R180 during the execution of the interrupt subroutine, which could lead to errors when returning to the main program. As shown in the figure below:



Interrupt Context Protection Schematic

4.3 Interrupt Control Register

The interrupt enable control registers INTE0 and INTE1 are read-write registers that contain control bits for enabling interrupts such as INT, TC0 overflow interrupt, and port level change interrupt.

The interrupt flag registers INTF0 and INTF1 are read-write registers (only writable to 0). When the relevant interrupt enable bits are enabled and EI is activated, the interrupt flag bits will be set to 1 when the corresponding interrupt conditions occur. User software can clear the interrupt flag bits to 0.

External interrupts need to select the triggering method in the EXINTCON register.

4.3.1 R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	INT1S<1:0>		INT0S<1:0>		PWM2_PULSEEN	CAPS	TC0GATE<1:0>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:6>: INT1S<1:0>-INT1 mode selection bit

INT1S<1>	INT1S<0>	INT1 Mode Selection
0	0	Function Disabled

0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

Bit<5:4>:INT0S<1:0>-INT0 Mode Selection Bit

INT0S<1>	INT0S<0>	INT0 Mode Selection
0	0	Function Disabled
0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

4.3.2 R1D6/INTE0 (Interrupt Enable Control Register 0)

0X1D6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE0	-	PWM2DTIE	CMPIE	INT1IE	INT0IE	TKIE	P6ICIE	P5ICIE
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>：Unused

Bit<6>：PWM2DTIE - PWM2 Duty Cycle Interrupt Enable Bit

0: Disable

1：Enable(Must enable PWM2EN=1)

Bit<5>: CMPIE - CMP output flag change interrupt enable bit

0: Disable

1: Enable

Bit<4>: INT1IE - INT1 interrupt enable bit

0: Disable

1: Enable

Bit<3>: INT0IE - INT0 interrupt enable bit

0: Disable

1: Enable

Bit<2>: TKIE - TK detection end interrupt

0: Disable

1: Enable

Bit<1>: P6ICIE - P6IC interrupt enable bit

0: Disable

1: Enable

Bit<0>: P5ICIE - P5IC interrupt enable bit

0: Disable

1: Enable

4.3.3 R1D7/INTE1 (Interrupt Enable Control Register 1)

0X1D7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE1	-	-	-	-	-	TC2IE	TC1IE	TC0IE
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:3>:Unused

Bit<2>: TC2IE - TC2 Overflow Interrupt Enable Bit

0: Disable

1: Enable

Bit<1>: TC1IE - TC1 Overflow Interrupt Enable Bit

0: Disable

1: Enable

Bit<0>: TC0IE - TC0 Overflow Interrupt Enable Bit

0: Disable

1: Enable

4.3.4 R1DA/INTF0 (Interrupt Flag Register 0)

0X1DA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF0	-	PWM2DTIF	CMPIF	INT1IF	INT0IF	TKIF	P6ICIF	P5ICIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: Unused

Bit<6>: PWM2DTIF - PWM2 Duty Cycle Interrupt Enable Bit

0: Disable

1: Enable

Bit<5>: CMPIF - CMP Output Flag Change Interrupt Flag Bit

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<4>:INT1IF - INT1 interrupt flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<3>:INT0IF - INT0 interrupt flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<2>: TKIF - TK detection end interrupt flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<1>: P6 ICIF - P6IC interrupt enable bit

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<0>: P5 ICIF - P5IC interrupt flag

0: No Interrupt Triggered

1: Interrupt Triggered

4.3.5 R1DB/INTF1 (Interrupt Flag Register 1)

0X1DB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF1	-	-	-	-	-	TC2IF	TC1IF	TC0IF
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:3>:Unused

Bit<2>: TC2IF - TC2 interrupt flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<1>: TC1IF - TC1 interrupt flag

0: No Interrupt Triggered

1: Interrupt Triggered

Bit<0>: TC0IF - TC0 interrupt flag

0: No Interrupt Triggered

1: Interrupt Triggered

5. Reset

5.1 Overview of Reset Function

The JZ8PT2503/4 system provides four types of reset methods:

- Power-On Reset (POR)
- RESET pin low-level reset
- WDT watchdog overflow reset
- LVR low-voltage reset

When any of the above resets occur, all system registers are initialized to their reset values, the program stops running, and the program counter (PC) is set to zero. After the reset is complete, the system starts running again from vector 0000H.

Any reset situation requires a certain response time, and the system reset mechanism ensures the reliable reset of the MCU. The time required to complete the reset varies with different types of oscillators. Therefore, the rise time of VDD and the startup time of different oscillators are not fixed. The startup time of an RC oscillator is the shortest, while that of a crystal oscillator is longer. During the use of the user terminal, it is important to consider the application scenario's requirements for power-on reset time.

5.2 Power-On Reset (POR)

Power-on reset is closely related to LVR operation. The process of powering on the system presents a gradually rising curve and requires a certain amount of time to reach the normal voltage level.

- Power-on: The system detects the rise in power supply voltage and waits for it to stabilize;
- System initialization: All system registers are set to their initial values;
- Oscillator starts working: The oscillator begins to provide the system clock;
- Executing program: Power-up is complete, and the program starts running;

The power-on reset time is determined by the "Reset Time" selection in the OPTION, with selectable reset times of 4.5ms, 16ms, 64ms, 256ms, and 350us.

5.3 WDT watchdog reset

The watchdog reset is a protective setting for the system. The watchdog is enabled by default upon power-up, and under normal conditions, the program resets the watchdog timer. If an error occurs and the system enters an unknown state, the watchdog timer overflows, causing the system to reset. After the watchdog reset, the system restarts and enters normal operation.

- Watchdog timer status: The system checks whether the watchdog timer has overflowed; if it has, the system resets;
- System initialization: All system registers are set to their default initialization values;
- Oscillator starts working: The oscillator begins to provide the system clock;
- Executing program: Power-up is complete, and the program starts running;

Explanation of watchdog wake-up:

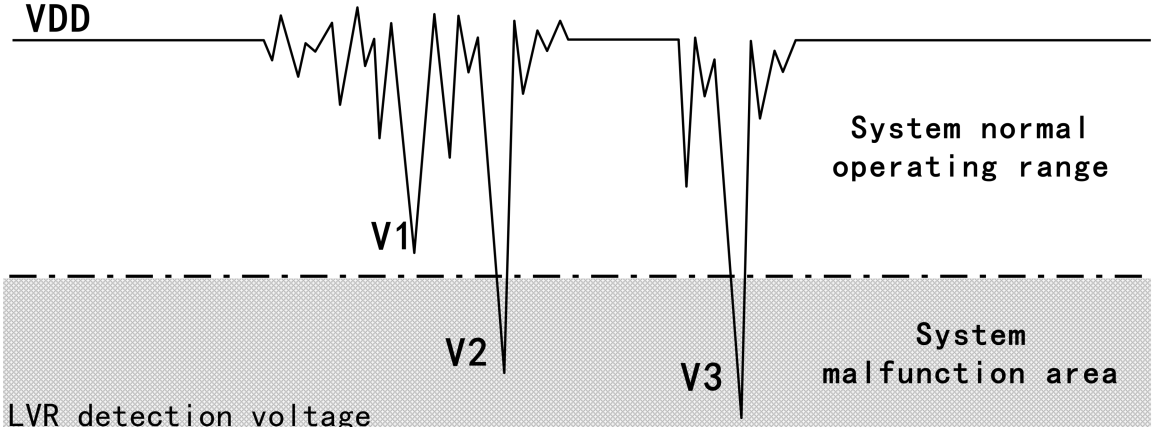
The watchdog reset can occur in both idle mode and sleep mode. After the system reset, the program execution starts from address 0X00. The user can check the time overflow bit of Bit4 in the R183 (STATUS) register; if it indicates WDT overflow, it can be determined that it is a watchdog reset. Note that the watchdog wake-up is essentially a special application of the watchdog reset. Watchdog wake-up time = option reset time * WDT prescaler

Watchdog Timer Application Precautions:

- Before resetting the watchdog, checking the status of the I/O ports and RAM can enhance the reliability of the program;
- Do not reset the watchdog during an interrupt, as this will prevent the detection of the main program's runaway condition;
- The program should only reset the watchdog once in the main program; this architecture maximizes the protective function of the watchdog.

5.4 LVR low-voltage reset

Power-off reset is aimed at situations where external factors cause a drop in system voltage (for example, interference or changes in external load). Power loss may lead to abnormal system operation or program execution errors.



A voltage drop may lead the system into a dead zone. The dead zone means that the power supply cannot meet the minimum operating voltage requirements of the system. The above diagram is a typical illustration of a power-off reset. In the diagram, VDD is severely disturbed, and the voltage value drops very low. The area above the dashed line indicates normal system operation, while the area below the dashed line indicates that the system enters an unknown operating state, referred to as the dead zone. When VDD drops to V1, the system remains in a normal state; when VDD drops to V2 and V3, the system enters the dead zone, which is prone to errors. The system may enter the dead zone in the following situations:

In DC applications:

DC applications generally use battery power. When the battery voltage is too low or the microcontroller drives a load, the system voltage may drop and enter the dead zone. At this point, the power supply will not further decrease to the LVR detection voltage, thus keeping the system in the dead zone.

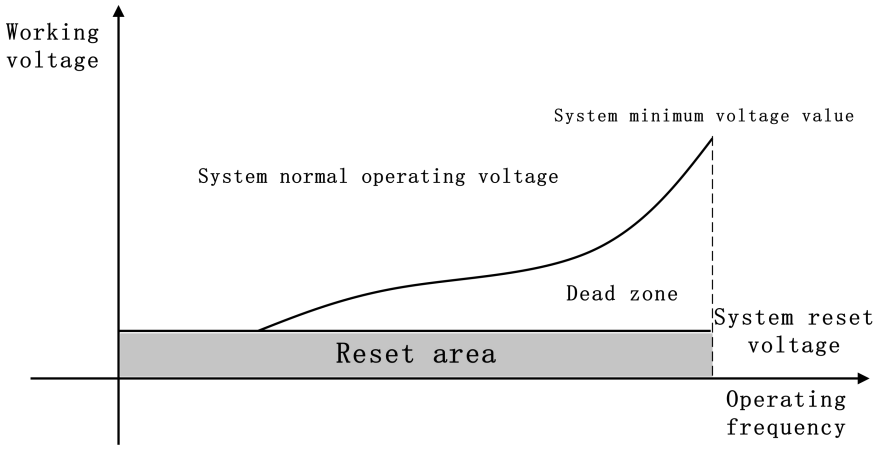
In AC applications:

When the system uses AC power, the DC voltage value is affected by noise in the AC power supply. When the external load is too high, such as when driving a motor, the interference generated by the load also affects the DC power supply. If VDD drops

below the minimum operating voltage due to interference, the system may enter an unstable operating state. In AC applications, the power-up and power-down times are relatively long. The power-up timing protection ensures that the system powers up normally, but the power-down process is similar to that in DC applications. After the AC power supply is turned off, the VDD voltage may slowly decrease and easily enter the dead zone.

5.5 Relationship between operating frequency and LVR low voltage detection

To improve the performance of the system's power-off reset, it is essential to first clarify the minimum operating voltage value of the system. The minimum operating voltage of the system is related to the execution speed, and the minimum operating voltage value varies at different execution speeds.



As shown in the figure above, the normal operating voltage region of the system is generally higher than the system reset voltage, which is determined by the Low Voltage Reset (LVR) level. When the execution speed of the system increases, the minimum operating voltage of the system also correspondingly increases. However, since the system reset voltage is fixed, a voltage region will appear between the minimum operating voltage and the system reset voltage where the system cannot operate normally and will not reset. This region is known as the dead zone.

To avoid the occurrence of dead zone voltage, it is necessary to select the corresponding LVR reset voltage point when choosing the operating frequency. As shown in the table below:

IRC Frequency	Clocks Division	LVR Reset Voltage Point
IRC-16MHz	2 Clocks	LVR=2.2V
IRC-8MHz	2 Clocks	LVR=2.0V
IRC-4MHz	2 Clocks	LVR=1.8V
IRC-1MHz	2 Clocks	LVR=1.8V

Note: 1. Operating frequency = Instruction cycle frequency = IRC frequency / Clocks division;

2. The corresponding values of this operating frequency and LVR reset voltage point are only recommended values. Users can adjust the reset voltage point appropriately based on the specific application during use.

3. LVR can be selected to be controlled by software to turn off, but it is only for testing purposes and not recommended for actual mass production.

5.6 Related Registers

5.6.1 R1AF/WDTCON (WDT, External Interrupt Control Register)

0X1AF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	WDTPSR<1:0>		LVREN	TKWE	CMPWE	INT1WE	INT0WE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Bit<7>: WDTE-WDT watchdog enable control

0: Disable

1: Enable

Bit<6:5>: WDTPSR<1:0>-WDT watchdog prescaler selection bits:

WDTPSR<1>	WDTPSR<0>	WDT frequency division coefficient
0	0	1:4
0	1	1:8
1	0	1:16
1	1	1:32

Bit<4>: LVREN -LVR Enable Control

0: Enable

1: Disable

6. System Clock and Operating Modes

The JZ8PT2503/4 integrates two types of oscillators: a high-speed RC oscillator (IHRC) and a low-speed RC oscillator (ILRC). The system clock can switch between high-speed and low-speed oscillators through the R188/CPUCON register. Switching oscillators allows the MCU to operate at different clock frequencies in four operating modes, which can control the operation of the oscillator, the execution of programs, and the functional power loss of the analog circuits.

High-Speed Mode: The system clock selects the internal high-speed clock, while the low-speed clock operates normally;

Low-Speed Mode: The system clock selects the internal low-speed clock, while the high-speed clock is paused;

Idle Mode: The system clock operates normally, while other parts of the system enter sleep mode (TC0, TC1, TC2, PWM2DT (no wake-up), TKWE; the selected system clock can continue to operate and wake up the system). It can also be awakened through P5IWE, P6IWE, INT0WE, INT1WE, and CMPWE;

Sleep mode: All functions are paused, and the system enters sleep mode, which can be awakened by TC0 (P62 input clock), P5IWE, P6IWE, INT0WE, INT1WE, CMPWE;

Functional module	High-speed mode	Low-speed mode	Idle mode	Sleep mode
IHRC	Run	Stop	Run	Stop
ILRC	Run	Run	Run	Stop
CPU instruction	Execute	Execute	Stop	Stop
TC0	Workable	Workable	Workable	Workable (P62 input clock)
TC1	Workable	Workable	Workable	Stop
TC2	Workable	Workable	Workable	Stop
Interrupt	All valid	All valid	All valid (TC0, TC1, TC2, PWMDT, TK select system clock)	TC0IE, P5ICIE, P6ICIE, EX0IE, EX1IE, CMPIE
Wake-up function	-	-	(TC0, TC1, TC2, TKWE system clock can wake up) P5IWE,P6IWE,INT0WE, INT1WE,CMPWE	TC0WE,P5IWE,P6IWE,INT0WE,INT1WE,CMPWE
Watchdog	WDT option	WDT	WDT option control	WDT option control

6.1 Internal RC oscillator

6.1.1 IHRC high-speed oscillator

The JZ8PT2503/4 provides an internal IHRC frequency configurable feature, with a default frequency of 8MHz.

The internal IHRC oscillator includes four frequency values: 1M/4M/8M/16MHz. By setting the configuration bits of the OPTION, the IHRC operating frequency can be selected, and below are their corresponding relationships:

RCM	IRC Frequency
1M	IHRC frequency selected as 1MHz
4M	IHRC frequency selected as 4MHz
8M	IHRC frequency selected as 8MHz
16M	IHRC frequency selected as 16MHz

JZ8PT2503/4 provides multiple frequency division options, which can be selected in OPTION, suitable for more occasions. As shown in the table below:

Clocks	Clocks Division
2clock	Frequency division is 2 clock
4 clock	Frequency division is 4 clock
8 clock	Frequency division is 8 clock
16 clock	Frequency division is 16 clock
32 clock	Frequency division is 32 clock

The IHRC system clock frequency can be fine-tuned by adding or subtracting 1 through the IHRCCAL register. Please refer to the "IHRC Frequency Fine-Tuning Parameter Description" for specific steps and frequency measurements.

6.1.2 ILRC Low-Speed Oscillator

JZ8PT2503/4 has a built-in ILRC low-speed oscillator that provides a stable 40KHz low-speed clock.

6.2 High-speed mode

The high-speed mode is the system's high-speed clock operating mode, with the system clock source provided by a high-speed RC oscillator. The program is executed. After a power-on reset or any reset trigger, the system enters high-speed mode to

execute the program. In high-speed mode, the high-speed oscillator operates normally, and power consumption is at its maximum.

- The program is executed, and all functions can be controlled;
- The system rate is high-speed;
- Both the high-speed oscillator and the internal low-speed oscillator operate normally;
- The high-speed mode can switch to low-speed mode;
- Entering sleep mode from high-speed mode, and returning to high-speed mode after waking up;
- Entering idle mode from high-speed mode, and returning to high-speed mode after waking up;

6.3 Low-speed mode

The low-speed mode is the system's low-speed clock operating mode. The system clock source is provided by a low-speed RC oscillator. The low-speed mode is controlled by the CLKMD bit of the CPU mode control register. When CLKMD=0, the system is in high-speed mode; when CLKMD=1, the system enters low-speed mode. After entering low-speed mode, the system cannot automatically disable the high-speed RC oscillator and must be disabled by setting SPTHX=1 to reduce power consumption.

- The program is executed, and all functions can be controlled;
- The system rate is low-speed;
- The internal low-speed oscillator is functioning normally, while the high-speed oscillator has stopped working.
- The low-speed mode can switch to high-speed mode;
- Transitioning from low-speed mode to sleep mode, and returning to low-speed mode after waking up;
- Transitioning from low-speed mode to idle mode, and returning to low-speed mode after waking up;

6.4 Idle mode

Idle mode is another ideal state. In sleep mode, all functions and hardware devices are disabled, but in idle mode, the system clock remains operational, and the power consumption in idle mode is greater than that in sleep mode. In idle mode, no programs are executed, but modules with wake-up functionality such as TC0, TC1, TC2, P5IWE, P6IWE, INT0WE, INT1WE, TKWE, and CMPWE continue to operate normally, with the clock sources for timers TC0, TC1, TC2, PWM2DT, and TKWE being the still-operational system clock. Whether to enter idle mode is determined by the system clock and the IDLE bit in the status control register; when IDLE=1, executing SLEEP will enter idle mode.

- The program stops executing, and all functions are disabled;
- Modules with wake-up functionality operate normally;
- The system clock operates normally;
- Transitioning from high-speed mode to idle mode, and returning to high-speed mode after waking up;
- Transitioning from low-speed mode to idle mode, and returning to low-speed mode after waking up;
- The wake-up methods in idle mode are P5IWE, P6IWE, INT0WE, INT1WE, TKWE, CMPWE;
- TC0, TC1, TC2, and PWMDT functions remain effective in idle mode;

6.5 Sleep mode

The sleep mode is the ideal state of the system, where no programs are executed, and the oscillator also stops working. The total power consumption of the chip is less than 1uA. The sleep mode can be awakened by TC0 (P62 input clock), P5IWE, P6IWE, INT0WE, INT1WE, and CMPWE. When entering sleep mode from high-speed mode or low-speed mode, it will return to the corresponding mode after being awakened. The system clock and the IDLE bit of the status control register control whether to enter sleep mode. When IDLE=0, executing SLEEP will enter sleep mode.

- The program stops executing, and all functions are disabled;
- All oscillators, including the external high-speed oscillator, internal high-speed oscillator, and internal low-speed oscillator, stop working;
- Power consumption is less than 1uA;

- Entering sleep mode from high-speed mode, it returns to high-speed mode after being awakened;
- Entering sleep mode from low-speed mode, it returns to low-speed mode after being awakened;
- The wake-up methods in sleep mode are TC0 (P62 input clock), P5IWE, P6IWE, INT0WE, INT1WE, and CMPWE;

6.6 Related Registers

6.6.1 R188/CPUCON (CPU mode control register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	PWM4_LEDEN	PWM1_LEDEN	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<5>: TC2WE - TC2 wake-up enable bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<4>: TC1WE - TC1 Wake-up Enable Bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<3>: TC0WE - TC0 wake-up enable bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<2>: STPHX - High-speed clock control bit

0: High-speed clock operates normally

1: Stop high-speed clock

Bit<1>: CLKMD - System clock control bit

0: System clock uses high-speed oscillator (IHRC) clock

1: System clock uses low-speed oscillator (ILRC) clock

When the system transitions from high-speed mode to low-speed mode, set CLKMD=1 first, then set STPHX=1;

When the system transitions from low-speed mode to high-speed mode, set STPHX=0 first, then set CLKMD=0.

Bit<0>: IDLE - Idle mode enable bit

0: The system enters sleep mode when executing the SLEEP instruction.

1: The system enters idle mode when executing the SLEEP instruction, and the system clock operates normally.

TC0 and PWM can continue to operate in idle mode if the system clock is selected, and can wake up the system.

6.6.2 R189/IHRCCAL (IHRC frequency trimming register)

0X189	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IHRCCAL	-	IHRCCAL<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	X	X	X	X	X	X	X

6.6.3 R1AF/WDTCON (WDT, External Interrupt Control Register)

0X1AF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	WDTPSR<1:0>		LVREN	TKWE	CMPWE	INT1WE	INT0WE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Bit<7>: WDTE-WDT watchdog enable control

0: Disable

1: Enable

Bit<6:5>: WDTPSR<1:0> - WDT watchdog prescaler selection bits:

WDTPSR<1>	WDTPSR<0>	WDT frequency division coefficient
0	0	1:4
0	1	1:8
1	0	1:16
1	1	1:32

Bit<3>: TKWE - TK wake-up enable bit

0: Disable

1: Enable

Bit<2>: CMPWE - CMP wake-up enable bit

0: Disable

1: Enable

Bit<1>: INT1WE - INT1 wake-up enable bit

0: Disable

1: Enable

Bit<0>: INT0WE - INT0Wake-up Enable Bit

0: Disable

1: Enable

7. Timer Counter

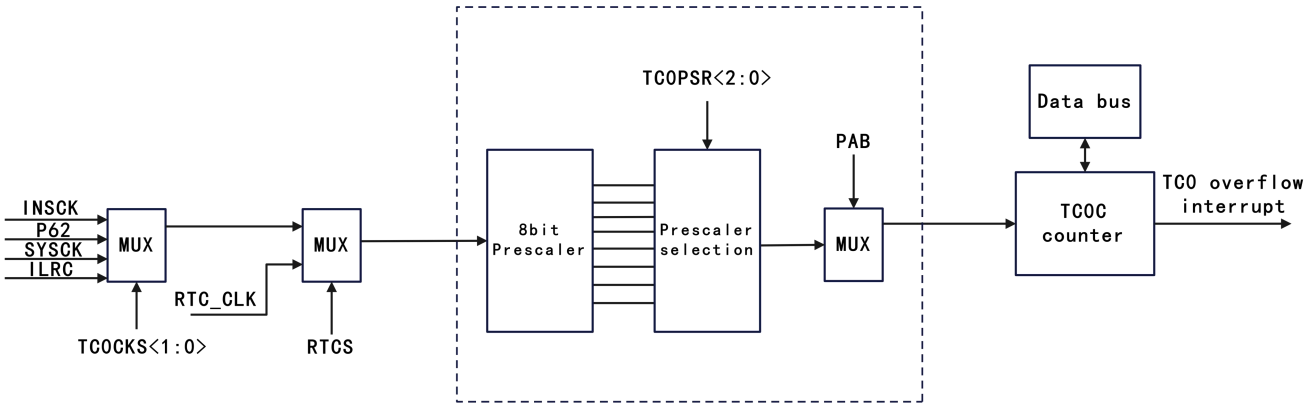
7.1 TC0 Timer Counter

The JZ8PT2503/4 provides an 8-bit timer counter as a prescaler for TC0. The PAB bit of the TC0CON register determines whether to prescale, and the TC0PSR<2:0> three bits determine the prescale ratio.

TC0 is an 8-bit up counter that operates as long as there is a clock. The clock source can be the instruction clock, system clock, or low-speed clock, and an external clock can also be selected (input via the P62 pin, with selectable trigger edge). The arrival of the clock increments the counter by 1.

TC0 count overflow can generate an interrupt signal.

In IDLE mode, the TC0 overflow interrupt can wake up the circuit, and after waking up, it can choose to enter the interrupt or continue executing the original program. In sleep mode, when TC0 is set to the P62 external input clock, it can interrupt overflow and wake up the circuit.



TC0 Structure Block Diagram

7.1.1 TC0 Timer Setting Instructions

1. Assign an initial value to the TC0C register TC0C;
2. Set the value of the TC0CON register (select clock source and prescaler);
3. To use as a counter, select the TC0 signal source as an external input signal in the TC0CON register;
4. After all configurations are set, finally enable the timer counter by setting TC0EN in the TC0CON register;

5. If interrupt functionality is required, set TC0IE (Bit0) in the INTE1 register to 1 and execute the EI instruction;
6. The system will automatically save ACC, STATUS, and RSR data when executing the interrupt service routine. After executing the RETI instruction, the data will be automatically restored. Before exiting the interrupt, the TC0 interrupt flag must be cleared;

7.1.2 TC0 Timer Calculation Explanation

The TC0 timing function is achieved by writing values to the TC0C register, assigning an initial value to the timer, which starts accumulating from the initial value until the timer overflows and generates an interrupt.

TC0 Timing Time Calculation Formula (select system clock):

$$\text{TC0 Timing duration} = (1/\text{Fsys}) \times (\text{TC0 prescaler}) \times (256 - \text{TC0 initial value})$$

Example:

Fosc=8 MHz, TC0 prescaler selection=8 prescaler, TC0 initial value=156;

$$\text{TC0 Timing duration} = (1/8) \times (8) \times (256 - 156) = 100\ \text{us}$$

TC0 timing time calculation formula (when selecting external input clock):

$$TC0\ \text{Timingduration} =$$

$$(1/\text{External input clock}) \times (\text{TC0 prescaler}) \times (256 - \text{TC0 initial value})$$

Example:

External input clock = 1 MHz, TC0 prescaler selection = 4 prescaler, TC0 initial value = 156;

$$\text{TC0 Timing duration} = (1/1) \times (4) \times (256 - 156) = 400\ \text{us}$$

7.1.3 TC0 Idle Mode Wake-up Description

In idle mode, the system instructions stop executing, while modules with wake-up functionality and the system clock operate normally, and other functions are disabled.

TC0 can wake up from idle mode by setting Bit 3 of the R188/CPUCON register, TC0WE, to 1. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC0 timer operates normally (selecting the system clock). When

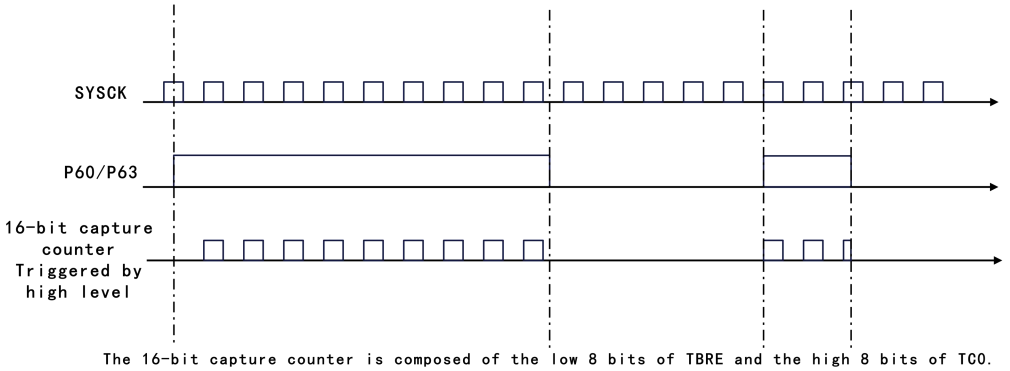
the TC0 timer overflows, the system is awakened. If TC0IE and EI are enabled, it will enter an interrupt after waking up; if DI is executed, it will execute the next instruction after waking up.

When the clock source is selected as the P62 external clock, enabling TC0WE = 1 and directly executing the SLEEP instruction can wake up the system.

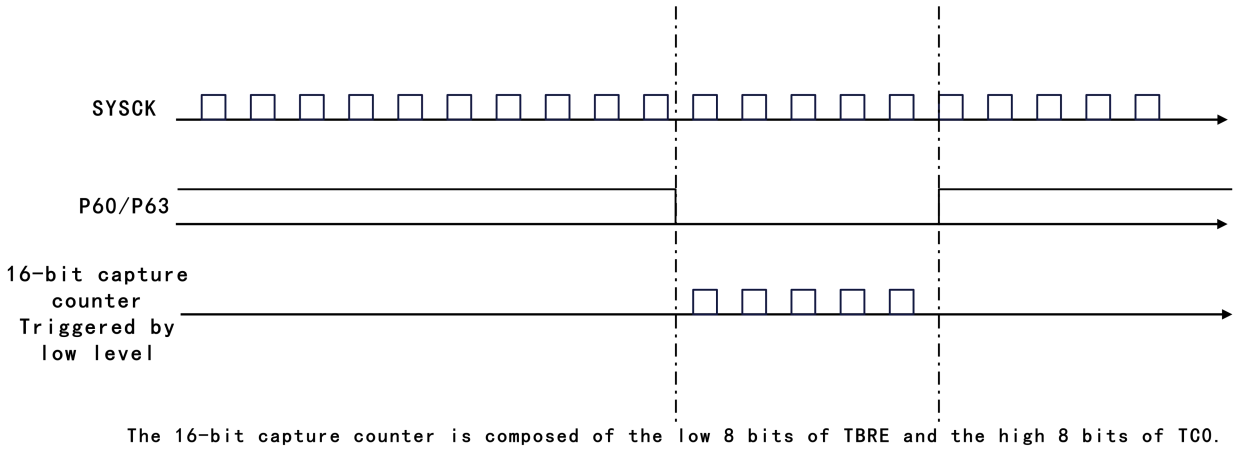
7.1.4 TC0 Port Level Capture Description

JZ8PT2503/4 provides P60/P63 port level capture functionality. By multiplexing the TC0 8-bit prescaler TPRE (as the low 8 bits of the level capture counter) and the 8-bit counter TC0C (as the high 8 bits of the level capture counter), a 16-bit level capture counter is formed. This works in conjunction with external interrupts to trigger interrupts on level changes, allowing the interrupt program to determine the capture time of the previous level. External interrupts can be selected for triggering edges through the R1AE/EXINTCON register INT1S<1:0>/ INT0S<1:0>.

P60/P63 port high-level capture functionality description. First, set the R1AE/EXINTCON register TC0GATE<0> = 1 to select the TC0 counter controlled by the external interrupt level. At the same time, select the external interrupt falling edge trigger function through INT1S<1:0>/ INT0S<1:0>, enabling the external interrupt. The TC0CON register selects the TC0 clock source as the system clock, and finally enable TC0EN = 1. When the P60/P63 port is at a high level, the TC0 prescaler and counter start counting, with the counting clock being the system clock. When the P60/P63 port is at a low level, the TC0 prescaler and counter stop counting, and the falling edge of the port triggers an external interrupt. The user can read the count values of the R185/TC0C and R1AD/TPRE registers in the interrupt program to calculate the level time.



P60/P63 port low-level capture is similar to high-level capture. First, set the R1AE/EXINTCON register TC0GATE<0> = 1 to select the TC0 counter controlled by the external interrupt level. At the same time, select the external interrupt rising edge trigger function through INT1S<1:0>/ INT0S<1:0>, enabling the external interrupt. The TC0CON register selects the TC0 clock source as the system clock, and finally enable TC0EN = 1. When the P60/P63 port is at a low level, the TC0 prescaler and counter start counting, with the counting clock being the system clock. When the P60/P63 port is at a high level, the TC0 prescaler and counter stop counting, and the rising edge of the port triggers an external interrupt. The user can read the count values of the R185/TC0C and R1AD/TPRE registers in the interrupt program to calculate the level time.



7.1.5 TC0 Related Registers

7.1.5.1 R184/TC0CON (TC0 Control Register)

0X184	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CON	TC0EN	TC0CKS<1:0>		TC0EDG	TC0PTEN	TC0PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC0EN - TC0 Timer Count Enable Bit

0: Disable TC0

1: Enable TC0

Bit<6:5>: TC0CKS<1:0>-TC0 signal source selection bit

00: Instruction Clock

01: External Input Signal (P62)

10: System Clock

11: ILRC Clock (Low-Speed Oscillator)

Bit<4>: TC0EDG - TC0 Signal Edge Selection Bit

0: TC0 Pin Signal Changes from High to Low Increments by 1

1: TC0 Pin Signal Changes from Low to High Increments by 1

Bit<3>: TC0PTEN - Prescaler Enable Bit

0: Disable TC0 Prescaler

1: Enable TC0 Prescaler

Bit<2:0>: TC0PSR<2:0> - TC0 Prescaler Selection Control Bit:

TC0PSR<2>	TC0PSR<1>	TC0PSR<0>	TC0 Prescaler Coefficient
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

7.1.5.2 R185/TC0C (TC0 8-bit Counter Register)

0X185	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0C	TC0C<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

7.1.5.3 R188/CPUCON (CPU mode control register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	PWM4_LEDEN	PWM1_LEDEN	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<3>: TC0WE - TC0 wake-up enable bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<0>: IDLE - Idle mode enable bit

0: The system enters sleep mode when executing the SLEEP instruction.

1: The system enters idle mode when executing the SLEEP instruction, and the system clock operates normally.

TC0 can continue to operate in idle mode if the system clock is selected, and it can wake up the system.

7.1.5.4 R1AD/TPRE (TC0 Prescaler)

0X1AD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TPRE	TPRE<7:0>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Captured data low 8 bits

7.1.5.5 R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	INT1S<1:0>		INT0S<1:0>		PWM2_PULSEEN	CAPS	TC0GATE<1:0>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:6>: INT1S<1:0>-INT1 mode selection bit

INT1S<1>	INT1S<0>	INT1 mode selection
0	0	Function Disabled
0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

Bit<5:4>:INT0S<1:0>-INT0 Mode Selection Bit

INT0S<1>	INT0S<0>	INT0 Mode Selection
0	0	Function Disabled
0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

Bit<2>: CAPS - TC0 level capture port selection

0: Use INT0 capture

1: Use INT1 capture

Bit<0>: TC0GATE<0> - TC0 capture gate enable bit

0: Disable

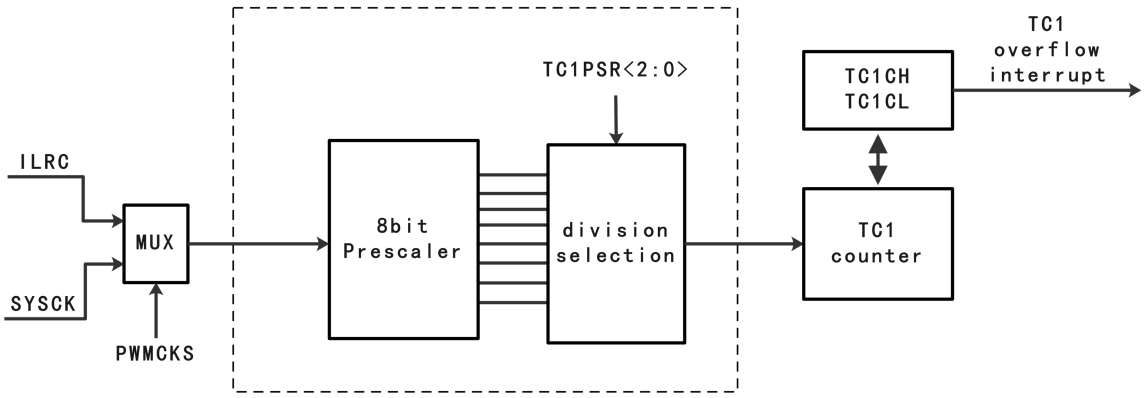
1: Enable gate control, INT0/1 as capture source

7.2 TC1 Timer Counter

TC1 Timer Counter provides an 8-bit prescaler, with the three bits TC1PSR<2:0> in the TC1CON register determining the prescale ratio.

TC1 is a 12-bit up counter. The TC1 timer must enable TC1EN to operate, and the clock source can be either the system clock or the low-speed clock. With each clock cycle, the counter increments by 1. The TC1 count value matches the TC1PRD setting to generate an overflow. If TC1IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service routine.

In IDLE mode, the TC1 interrupt can wake up the circuit (the clock is the system clock). After waking up, it can choose to enter the interrupt or continue executing the original program.



TC1 Block Diagram

7.2.1 TC1 Timer Setting Instructions

1. Assign an initial value to the TC1PRD<11:0> register;
2. Set the TC1CON register, configuring the prescale ratio as needed;
3. Enable the TC1IE in the R1D7/INTE1 register to turn on interrupt enable and execute the EI instruction;
4. Enable TC1EN to start counting the TC1 timer;
5. The system's interrupt service routine will automatically save the ACC, STATUS, and RSR data. After executing the RETI instruction, the data will be automatically restored, and the TC1 interrupt flag must be cleared before exiting the interrupt.

7.2.2 TC1 Timing Calculation Explanation

The TC1 timing function is achieved by writing a value to TC1PRD<11:0>. The timer starts counting from the initial value of 0x01 and continues to accumulate until the timer count matches the TC1PRD<11:0> value, at which point an overflow triggers the execution of the interrupt service routine.

TC1 Timing Calculation Formula:

$$\text{TC1 Timing duration} = (1/\text{Fosc}) \times (\text{TC1 Prescaler}) \times (\text{TC1PRD})$$

Example:

Fosc = 16 MHz, TC1 Prescaler Selection = 16, TC1PRD Value = 512;

$$\text{TC1 Timing duration} = (1/16) \times (16) \times （512） = 512\text{us}$$

7.2.3 TC1 Idle Mode Wake-up Explanation

TC1 can wake up from idle mode by enabling the R188/CPUCON register Bit 4 (TC1WE) and selecting the TC1 clock source as the system clock. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC1 timer operates normally. After the TC1 timer overflows, the system is awakened. If TC1IE and EI are enabled, it will enter an interrupt after waking up; if DI is executed, it will execute the next instruction after waking up.

7.2.4 TC1 Related Registers

There are three registers related to TC1: the low 8-bit count compare register (TC1PRDL), the high 4-bit count compare register (TC1PRDTH), and the control register (TC1CON). The TC1WE bit in the CPUCON register enables control of waking up from IDLE mode.

7.2.4.1 R188/CPUCON (CPU mode control register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	PWM4_LEDEN	PWM1_LEDEN	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<4>: TC1WE - TC1 Wake-up Enable Bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<0>: IDLE - Idle mode enable bit

0: The system enters sleep mode when executing the SLEEP instruction.

1: The system enters idle mode when executing the SLEEP instruction, and the system clock operates normally.

TC1 can continue to operate in idle mode if the system clock is selected and can wake up the system.

7.2.4.2 R1B0/TC1CON(TC1 Control Register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GATE	TC1CKS	TC1PTEN	TC1PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC1EN - TC1 Counter Enable Control

(If the TC1PRD register is set, TC1 will reset when counting to the preset value, and TC1 will start counting from 1)

0: Disable

1: Enable

Bit<6>: TC21EN-TC1, TC2 counter simultaneous enable control bit

0: Disable

1: Enable

Bit<4>: TC1CKS - TC1 Clock Selection

0: System Clock

1: Low-Speed Clock

Bit<3:0>: TC1PTEN, TC1PSR2 - TC1PSR0 Prescaler Selection Bits:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	TC1 Prescaler Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

7.2.4.3 R1B1/TC1PRDL (TC1 Timer Count Low 8-bit Register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Low 8 bits of TC1 timer count

7.2.4.4 R1B5/TC1PRDTH (High 4 bits of TC1 timer count and high 4 bits of PWM3 duty cycle register)

0X1B5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<11:8>				PWM3DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

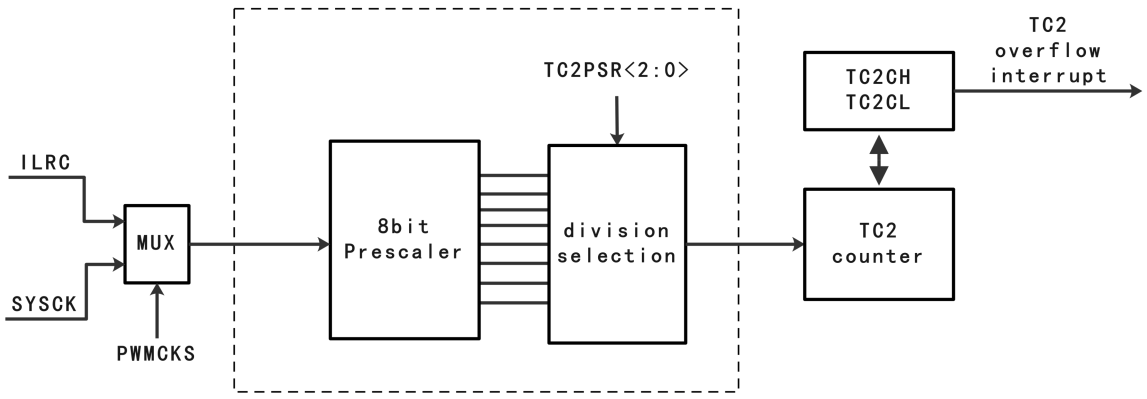
High 4 bits of TC1 timer count

7.3 TC2 timer counter

TC2 timer counter provides an 8-bit prescaler, with the three bits TC2PSR<2:0> in the TC2CON register determining the prescale ratio.

TC2 is a 12-bit up counter. The TC2 timer must be enabled with TC2EN to operate, and the clock source can be either the system clock or a low-speed clock. With each clock cycle, the counter increments by 1. The TC2 count value matches the TC2PRD setting to produce an overflow. If TC2IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service routine.

In IDLE mode, the TC2 interrupt can wake up the circuit (with the clock being the system clock). After waking up, it can choose to enter the interrupt or continue executing the original program.



TC2 Block Diagram

7.3.1 TC2 Timing Setting Instructions

1. Assign an initial value to the TC2PRD<11:0> register;
2. Set the TC2CON register and configure the prescaler as needed;
3. Enable the TC2IE interrupt by setting the R1D7/INTE1 register and execute the EI instruction;
4. Enable TC2EN to start the TC2 timer counting;
5. The system will automatically save ACC, STATUS, and RSR data when executing the interrupt service routine. After executing the RETI instruction, the data will be automatically restored. Before exiting the interrupt, the TC2 interrupt flag must be cleared;

7.3.2 TC2 Timing Calculation Instructions

The TC2 timing function works by writing values to TC2PRD<11:0>. The timer starts counting from the initial value of 0x01 until the timer count matches the TC2PRD<11:0> value, at which point it overflows and executes the interrupt service routine.

TC2 Timer Calculation Formula:

$$\text{TC2 Timing duration} = (1/\text{Fosc}) \times (\text{TC2 Prescaler}) \times (\text{TC2PRD})$$

Example:

Fosc=16 MHz, TC2 Prescaler Selection=16 Prescaler, TC2PRD Value=512;

$$\text{TC2 Timing duration} = (1/16) \times (16) \times （512） = 512\text{us}$$

7.3.3 TC2 Idle Mode Wake-up Description

TC2 can wake up from idle mode by enabling Bit 5 of the R188/CPUCON register, TC2WE, and selecting the TC2 clock source as the system clock. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC2 timer operates normally. After the TC2 timer overflows, the system is awakened. If TC2IE and EI are enabled, it will enter an interrupt after waking up; if DI is executed, it will execute the next instruction after waking up.

7.3.4 TC2 Related Registers

There are three registers related to TC2: the low 8-bit count compare register (TC2PRDL), the high 4-bit count compare register (TC2PRDTH), and the control register (TC2CON). The TC2WE in the CPUCON register enables control of waking up from IDLE mode.

7.3.4.1 R188/CPUCON (CPU mode control register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	PWM4_LEDEN	PWM1_LEDEN	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<5>: TC2WE - TC2 wake-up enable bit

0: Wake-up disabled

1: Wake-up enabled, can wake up from idle mode

Bit<0>: IDLE - Idle mode enable bit

0: The system enters sleep mode when executing the SLEEP instruction.

1: The system enters idle mode when executing the SLEEP instruction, and the system clock operates normally.

TC2 can continue to operate in idle mode if the system clock is selected and can wake up the system.

7.3.4.2 R1B8/TC2CON (TC2 Control Register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC2EN-TC2/PWM456 counter enable control

0: Disable

1: Enable

Bit<4>: TC2CKS-TC2 clock selection

0: System Clock

1: Low-Speed Clock

Bit<3:0>: TC2PTEN, TC2PSR2～TC2PSR0 prescaler selection bits:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 Prescaler Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

7.3.4.3 R1B9/TC2PRDL (TC2 Timer Count Low 8-bit Register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 Timer Count Low 8-bit

7.3.4.4 R1BD/TC2PRDTH (TC2 Timer Count High 4-bit and PWM6 Duty Cycle High 4-bit Register)

0X1BD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD<11:8>				PWM6DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 Timer Count High 4-bit

8. PWM Pulse Width Modulation

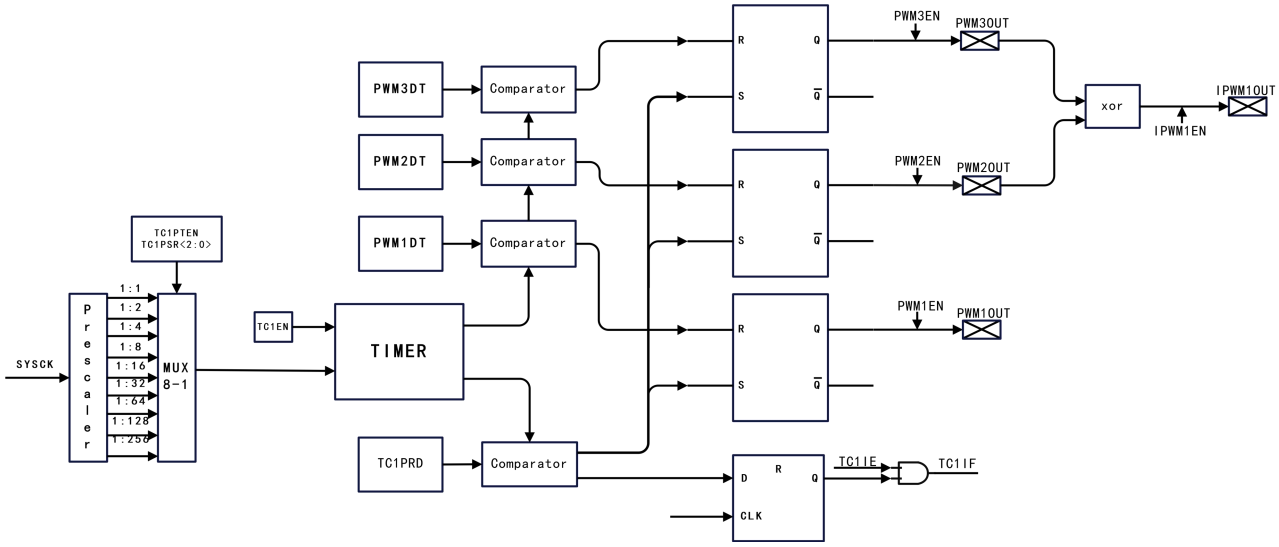
JZ8PT2503/4 provides 2 sets of 12-bit TC1 and TC2 counters. Each set of counters can be divided into three PWM channels to generate pulse width modulation signals. The PWM output waveform is determined by the period and duty cycle, while the transmission rate is determined by the period. The chip provides dead-time complementary output, with IPWM1 being the result of XORing PWM2 and PWM3, and PWM1 serving as the dead-time complementary signal. (IPWM4 is the same as IPWM1)

PWM has a period overflow interrupt, which can jump to the interrupt when enabled.

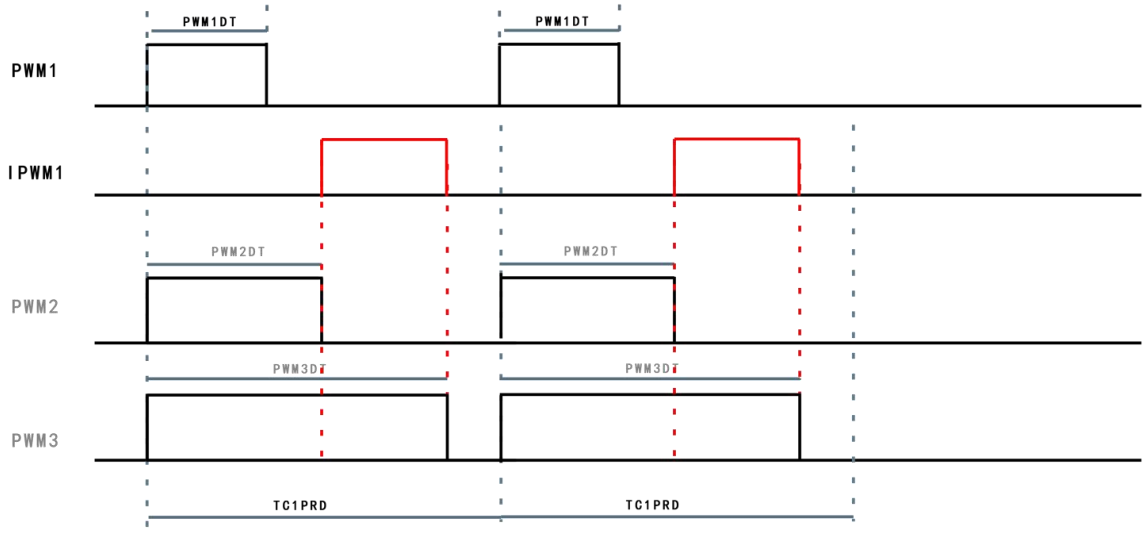
In IDLE (idle mode), TC1 and TC2 can wake up the system by selecting TC1CKS=0 and TC2CKS=0 in the TC1 and TC2 control registers, and enabling TC1WE and TC2WE in the CPU mode control register.

8.1 PWM internal structure and timing

The following internal structure diagram is for reference only and does not represent the actual circuit.



PWM working structure circuit



Timing description of 3-channel common period PWM and IPWM

8.2 PWM period and duty cycle

PWM provides a 12-bit clock counter with an 8-bit programmable prescaler, serving as the baud rate clock generator for the PWM module. The counter function can be enabled by setting TCxEN in the PWM control register. The prescaler settings for the counter can be configured using the TCxPSR<2:0> control bits. PWMxE and IPWMxE enable the PWM function and the PWM complementary function, respectively.

The PWM period is set by writing values to the TCxPRDL (low eight bits) and TCxPRDTH (high four bits) period registers. When the counter value equals the PRD value, the following events occur in the next increment period:

- Counter reset;
- Set the corresponding PWM output pin to high level;
- Generate PWM period overflow interrupt (if enabled);
- The PWM duty cycle is latched from the PWMxDTL/TCxPRDTH register to the DT/TIMER compare register;

PWM period calculation formula:

$$\text{PWM period} = (\text{PRD}) \times (\text{PWM_CK}) \times (\text{PWM prescaler})$$

Example:

PWMxRD=100, Fosc=16MHz, PWMCKS=1, PWM prescaler selection=2 prescaler;

$$\text{PWM period} = (100) \times (1/16) \times (2) = 12.5\ \text{us}$$

The PWM duty cycle is written to the PWM duty cycle register, and when the counter value overflows and resets to zero, the value of PWMxDT is latched to the DT/TIMER compare register. When the value of the DT/TIMER compare register equals the value of the TIMER counter, the PWM output pin is set to low level. The value of PWMxDT can be written at any time, but the value of the DT/TIMER compare register is only written during period overflow:

PWM duty cycle calculation formula:

$$\text{PWM duty} = (\text{DT}) \times (\text{PWM_CK}) \times (\text{PWM prescaler})$$

Example:

PWMxDT=50, Fosc=16MHz, PWMCKS=1, PWM prescaler selection=2 prescaler;

$$\text{PWM duty} = (50) \times (1/16) \times (2) = 6.25\ \text{us}$$

8.3 PWM idle mode wake-up description

In idle mode, CPU instructions stop executing, modules with wake-up functionality and the system clock operate normally, while other functions are disabled.

PWM can wake up from idle mode by setting TC1/TC2WE wake-up enable and selecting the clock source as the system clock (SYSCK). Set the corresponding period or duty cycle interrupt enable, set IDLE (R188) to 1, and use the SLEEP instruction to put the system into idle mode while the PWM timer operates normally.

When the corresponding interrupt condition is met, the system is awakened. If EI is enabled, it enters the interrupt after waking up; if DI is enabled, it executes the next instruction after waking up.

8.4 PWM Comparator Gating Description

The gating function of PWM1 is controlled by the PWM1GATE of the TC1CON register. When PWM1GATE=1, the PWM1 output is controlled by the comparator result, and when CMP_FLAG=0, it outputs the PWM waveform.

The gating function of PWM4 is controlled by the PWM4GATE<1:0> of the TC2CON register. When PWM4GATE<0>=1, the PWM4 output is controlled by the comparator result, and when CMP_FLAG=0, it outputs the PWM waveform. When PWM4GATE<1>=1, the PWM4 output

is controlled by the external interrupt EXINT (P60), and when EXINT=1, it outputs the PWM waveform.

8.5 IPWM Waveform and Buzzer Setting Description

The IPWM waveform is not directly inverted; instead, by enabling IPWM1EN, the outputs of PWM2 and PWM3 are XORed before outputting. If IPWM1EN is enabled at this time, the output selection control bit can choose to output from P61/P67 through PWM2; enabling PWM3EN allows the output selection control bit to choose from P60/P50 through PWM3. It also supports simultaneous output of the IPWM1 waveform from two ports.

Similarly, enabling IPWM4EN outputs the result of XORing PWM5 and PWM6. If PWM5EN is enabled at this time, the output selection control bit can choose to output from P64/P54 through PWM5; enabling PWM6EN allows the output selection control bit to choose from P63/P53 through PWM6. It also supports simultaneous output of the IPWM4 waveform from two ports.

The PWM module also includes a buzzer function. Users can enable PWM output for the buzzer through the control bit BZXEN (R1B7, R1BF). The buzzer can be port-selected through PWM1S (R1B7) and PWM4S (R1BF), outputting from P60/P53 and P50/P62, respectively. It is important to note that to enable the buzzer, PWM1EN and PWM4EN must be cleared, and the corresponding output ports must be set to output.

8.6 PWM2DT Interrupt and Single Trigger Description

PWM2DT provides the function of triggering interrupts based on duty cycle. After enabling PWM2DTIE (R1D6) and executing the PWM2EN+EI instruction, it can enter the interrupt program based on the configured PWM2 duty cycle.

PWM2 can be configured for single pulse output. By setting the EXINTCON register PWM2_PULSEEN bit to 1, a single PWM2 waveform can be output. After one output, PWM2 stops outputting and remains at a low level. In this mode, the duty cycle can be configured to trigger an interrupt once.

8.7 PWM-related registers

The JZ8PT2503/4 chip has two built-in sets of 12-bit PWM, each configurable for 3 channels with common period and independent duty cycle. Each PWM group can set a pair of complementary PWM outputs.

8.7.1 R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	INT1S<1:0>		INT0S<1:0>		PWM2_PULSEEN	CAPS	TC0GATE<1:0>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<3>: PWM2_PULSEEN—PWM2 single pulse enable bit

0: Disable

1: Enable

8.7.2 R1B0/TC1CON(TC1 Control Register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GATE	TC1CKS	TC1PTEN	TC1PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC1EN - TC1/PWM123 counter enable control

(If the TC1PRD register is set, TC1 will reset when counting to the preset value, and TC1 will start counting from 1)

0: Disable

1: Enable

Bit<6>: TC21EN - TC1/PWM123, TC2/PWM456 counter simultaneous enable control bit

0: Disable

1: Enable

Bit<5>: PWM1GATE - PWM1 gate output enable control bit

0: No restriction

1: PWM1 output is controlled by the comparator result. When CMPOUT=0, PWM waveform is output; when CMPOUT=1, PWM1 remains at a low level.

Bit<4>: TC1CKS - TC1 Clock Selection

0: System Clock

1: Low-Speed Clock

Bit<3:0>: TC1PTEN, TC1PSR2 - TC1PSR0 Prescaler Selection Bits:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	TC1 Prescaler Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

8.7.3 R1B1/TC1PRDL (TC1/PWM123 period low 8-bit register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Low 8 bits of TC1 (PWM1, PWM2, PWM3) period

8.7.4 R1B2/PWM1DTL (PWM1 Duty Cycle Low 8-bit Register)

0X1B2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DTL	PWM1DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM1 Duty Cycle Low 8-bit

8.7.5 R1B3/PWM2DTL (PWM2 Duty Cycle Low 8-bit Register)

0X1B3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2DTL	PWM2DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM2 Duty Cycle Low 8-bit

8.7.6 R1B4/PWM3DTL (PWM3 Duty Cycle Low 8-bit Register)

0X1B4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM3DTL	PWM3DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM3 duty cycle low 8 bits

8.7.7 R1B5/TC1PRDTH (PWM123 period high 4 bits and PWM3 duty cycle high 4 bits register)

0X1B5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<11:8>				PWM3DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM2, PWM3) period high 4 bits and PWM3 duty cycle high 4 bits

8.7.8 R1B6/PWM12DTH (PWM12 duty cycle high 4 bits register)

0X1B6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM12DTH	PWM2DT<11:8>				PWM1DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM2 duty cycle high 4 bits, PWM1 duty cycle high 4 bits

8.7.9 R1B7/PWMCON1 (PWM control register 1)

0X1B7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON1	BZ1EN	PWM3S	PWM2S	PWM1S	IPWM1EN	PWM3EN	PWM2EN	PWM1EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ1EN - BZ1 waveform output enable control bit

0: Disable

1: Output BZ1 waveform (BZ1EN=1, PWM1EN=0 must be set)

(Set P66/P62 to output in order to output BZ1 waveform)

Bit<6>: PWM3 output selection control bit

0: PWM3 outputs from P60

1: PWM3 outputs from P50

Bit<5>: PWM2 output selection control bit

0: PWM2 outputs from P61

1: PWM2 outputs from P67

Bit<4>: PWM output selection control bit

0: PWM1 outputs from P62

1: PWM1 outputs from P66

Bit<3>: IPWM1EN - IPWM1 enable control bit

0: Disable

1: Output PWM2 and PWM3 XOR

(Select output port based on PWM2EN (P61/P67) or PWM3EN (P60/P50))

Bit<2>: PWM3EN - PWM3 enable control bit

0: Disable

1: Output PWM3 waveform enable

(The corresponding port must be set to output to output PWM3 waveform)

Bit<1>: PWM2EN - PWM2 enable control bit

0: Disable

1: Output PWM2 waveform enable

(The corresponding port must be set to output to output PWM2 waveform)

Bit<0>: PWM1EN - PWM1 enable control bit

0: Disable

1: Output PWM1 waveform enable

(The corresponding port must be set to output in order to output the PWM1 waveform, and BZ1EN=0)

8.7.10 R1B8/TC2CON (TC2 Control Register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC2EN-TC2/PWM456 counter enable control

0: Disable

1: Enable

Bit<6:5>: PWM4GATE<1:0> - PWM4 gate output enable control bits

PWM4GATE<1>	PWM4GATE<0>	PWM4 gate output enable control selection
0	0	No restrictions
0	1	PWM4 output is controlled by the comparator result; when CMPOUT=0, it outputs the PWM waveform, and when CMPOUT=1, PWM4 remains at a low level
1	0	PWM4 output is controlled by the external interrupt INT (P60); when INT=1, it outputs the PWM waveform
1	1	Configuration prohibited

Bit<4>: TC2CKS-TC2 clock selection

0: System Clock

1: Low-Speed Clock

Bit<3:0>: TC2PTEN, TC2PSR2～TC2PSR0 prescaler selection bits:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 Prescaler Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

8.7.11 R1B9/TC2PRDL (TC2/PWM456 period low 8-bit register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 (PWM4, PWM5, PWM6) low 8 bits of the cycle

8.7.12 R1BA/PWM4DTL (PWM4 Duty Cycle Low 8-bit Register)

0X1BA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM4DTL	PWM4DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM4 Duty Cycle Low 8-bit

8.7.13 R1BB/PWM5DTL (PWM5 Duty Cycle Low 8-bit Register)

0X1BB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM5DTL	PWM5DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM5 Duty Cycle Low 8-bit

8.7.14 R1BC/PWM6DTL (PWM6 Duty Cycle Low 8-bit Register)

0X1BC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM6DTL	PWM6DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM6 duty cycle low 8 bits

8.7.15 R1BD/TC2PRDTH (PWM456 period high 4 bits and PWM6 duty cycle high 4 bits register)

0X1BD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD<11:8>				PWM6DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 (PWM4, PWM5, PWM6) period high 4 bits and PWM6 duty cycle high 4 bits

8.7.16 R1BE/PWM45DTH (PWM45 duty cycle high 4 bits register)

0X1BE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM45DTH	PWM5DT<11:8>				PWM4DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM5 duty cycle high 4 bits, PWM4 duty cycle high 4 bits

8.7.17 R1BF/PWMCON2 (PWM control register 2)

0X1BF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON2	BZ2EN	PWM6S	PWM5S	PWM4S	IPWM4EN	PWM6EN	PWM5EN	PWM4EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ2EN - BZ2 waveform output enable control bit

0: Disable

1: Output BZ2 waveform (BZ2EN=1, PWM4EN=0 must be set)

(Set P65/P55 as output to output BZ2 waveform)

Bit<6>: PWM6S-PWM6 output selection control bit

0: PWM6 outputs from P63

1: PWM6 outputs from P53

Bit<5>: PWM5S-PWM5 output selection control bit

0: PWM5 outputs from P64

1: PWM5 outputs from P54

Bit<4>: PWM4S-PWM4 output selection control bit

0: PWM4 outputs from P65

1: PWM4 outputs from P55

Bit<3>: IPWM4EN-IPWM4 enable control bit

0: Disable

1: Output PWM5 and PWM6 XOR

(Select output port based on PWM5EN (P64/P54) or PWM6EN (P63/P53))

Bit<2>: PWM6EN - PWM6 enable control bit

0: Disable

1: Output PWM6 waveform enable

(The corresponding port must be set to output to output the PWM6 waveform)

Bit<1>: PWM5EN - PWM5 enable control bit

0: Disable

1: Output PWM5 waveform enable

(The corresponding port must be set to output to output the PWM5 waveform)

Bit<0>: PWM4EN - PWM4 enable control bit

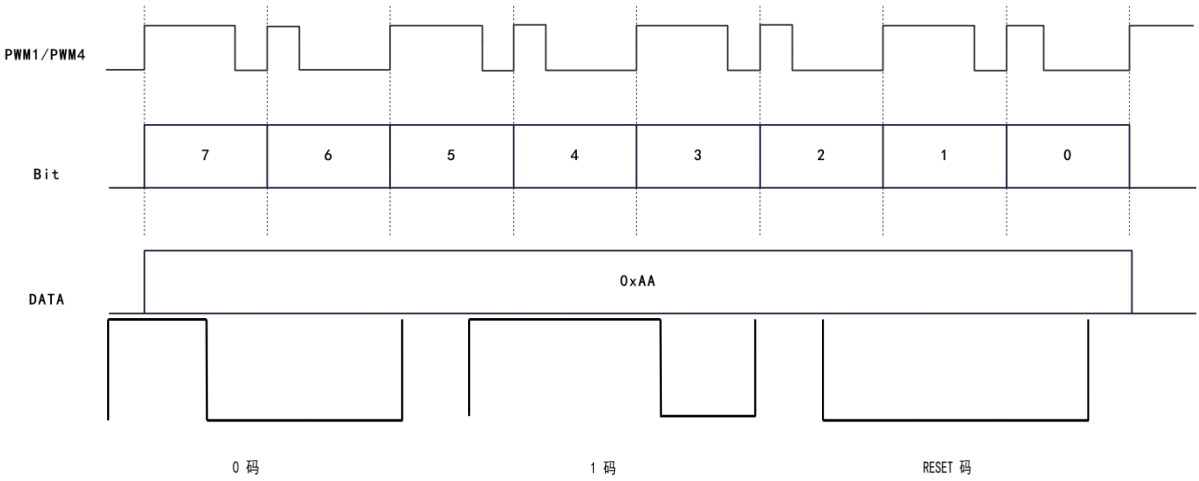
0: Disable

1: Output PWM4 waveform enable

(The corresponding port must be set to output in order to output the PWM4 waveform, and BZ2EN=0)

9. Single-wire cascading LED

The JZ8PT2503/4 supports 2-channel single-wire cascading LED driving, controlling the cascading timing through PWM1 and PWM4 ports. The timing diagram for cascading LED driving is as follows:



Single-wire cascading LED timing description

PWM1 and PWM4 are two independent single-wire cascading LED driving controls. When using PWM1 as the LED driving control, the high-level time for the 0 code type is set by the PWM1 duty cycle register, the high-level time for the 1 code type is set by the PWM2 duty cycle register, the period of the code type data is set by the TC1PRD period register, and the data sent is set by the PWM3 duty cycle register. After enabling PWM1_LEDEN (R188/CPUCON) + TC1EN, the transmission of 8-bit cascading data begins, and the data is output from the PWM1 port. After the transmission of the 8-bit cascading data is completed, TC1EN is automatically reset to zero, and resetting TC1EN again starts the transmission of the next 8-bit cascading data.

When using PWM4 as the LED driving control, the high-level time for the 0 code type is set by the PWM4 duty cycle register, the high-level time for the 1 code type is set by the PWM5 duty cycle register, the period of the code type data is set by the TC2PRD period register, and the data sent is set by the PWM6 duty cycle register. After enabling PWM4_LEDEN (R188/CPUCON) + TC2EN, the transmission of 8-bit cascading data begins, and the data is output from the PWM4 port. After the transmission of the 8-bit cascading data is completed, TC2EN is automatically reset to zero, and resetting TC2EN again starts the transmission of the next 8-bit cascading data.

9.1 Related Registers

9.1.1 R188/CPUCON (CPU mode control register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	PWM4_LEDEN	PWM1_LEDEN	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM4_LEDEN - PWM4 LED cascading control bit

0: Disable

1: Enable

Bit<6>: PWM1_LEDEN - PWM1 LED cascading control bit

0: Disable

1: Enable

9.1.2 R1B0/TC1CON(TC1 Control Register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GATE	TC1CKS	TC1PTEN	TC1PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC1EN - PWM1 cascading LED data transmission control bit

0: Disable (automatically cleared to 0 after transmission ends)

1: Enable (Send LED data)

Bit<4>: TC1CKS - TC1 Clock Selection

0: System Clock

1: Low-Speed Clock

Bit<3:0>: TC1PTEN, TC1PSR2 - TC1PSR0 Prescaler Selection Bits:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR<0>	TC1 Prescaler Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

9.1.3 R1B1/TC1PRDL (TC1/PWM123 period low 8-bit register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: Symbol period time

9.1.4 R1B2/PWM1DTL (PWM1 Duty Cycle Low 8-bit Register)

0X1B2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DTL	PWM1DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: PWM1-0 high level time

9.1.5 R1B3/PWM2DTL (PWM2 Duty Cycle Low 8-bit Register)

0X1B3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2DTL	PWM2DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: PWM1-1 high level time

9.1.6 R1B4/PWM3DTL (PWM3 Duty Cycle Low 8-bit Register)

0X1B4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM3DTL	PWM3DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: PWM1-cascade LED data transmission

9.1.7 R1B7/PWMCON1 (PWM control register 1)

0X1B7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON1	BZ1EN	PWM3S	PWM2S	PWM1S	IPWM1EN	PWM3EN	PWM2EN	PWM1EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<4>: PWM output selection control bit

0: PWM1 outputs from P62

1: PWM1 outputs from P66

Bit<0>: PWM1EN - PWM1 enable control bit

0: Disable

1: Output PWM1 waveform enable

(The corresponding port must be set to output in order to output the PWM1 waveform, and BZ1EN=0)

9.1.8 R1B8/TC2CON (TC2 Control Register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC2EN-PWM4 cascade LED data transmission control bit

0: Disable (automatically cleared to 0 after transmission ends)

1: Enable (Send LED data)

Bit<4>: TC2CKS-TC2 clock selection

0: System Clock

1: Low-Speed Clock

Bit<3:0>: TC2PTEN, TC2PSR2～TC2PSR0 prescaler selection bits:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 Prescaler Coefficient
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

9.1.9 R1B9/TC2PRDL (TC2/PWM456 period low 8-bit register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: PWM4-symbol period time

9.1.10 R1BA/PWM4DTL (PWM4 Duty Cycle Low 8-bit Register)

0X1BA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM4DTL	PWM4DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: PWM4-0 high level time

9.1.11 R1BB/PWM5DTL (PWM5 Duty Cycle Low 8-bit Register)

0X1BB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM5DTL	PWM5DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: PWM4-1 high level time

9.1.12 R1BC/PWM6DTL (PWM6 Duty Cycle Low 8-bit Register)

0X1BC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM6DTL	PWM6DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: PWM4-LED cascade data transmission

9.1.13 R1BF/PWMCON2 (PWM control register 2)

0X1BF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON2	BZ2EN	PWM6S	PWM5S	PWM4S	IPWM4EN	PWM6EN	PWM5EN	PWM4EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<4>: PWM4S-PWM4 output selection control bit

0: PWM4 outputs from P65

1: PWM4 outputs from P55

Bit<0>: PWM4EN - PWM4 enable control bit

0: Disable

1: Output PWM4 waveform enable

(The corresponding port must be set to output in order to output the PWM4 waveform, and BZ2EN=0)

10. CDC touch key detection

10.1 Touch Detection Overview

The touch key detection of JZ8PT2503/4 is based on the self-capacitance sensing principle, which can replace traditional mechanical keys, achieving better dustproof, waterproof, and sealed isolation effects while also being aesthetically pleasing. Compared to traditional keys, it has a longer lifespan and lower maintenance costs, making it more suitable for most applications.

Touch Resources:

- 12 touch channels available
- Internal capacitance configurable
- Reference voltage selectable

10.2 Touch Precautions

- Connect 104 to the power ground and add a 10uF capacitor if necessary, placing the capacitor as close to the MCU as possible;
- Output and touch should be separated or not on the same side;
- The ground line of the touch chip should not be shared with other circuits and should be connected separately to the grounding point of the board's power input;
- When designing the layout, try to place the touch MCU at the center position of multiple touch buttons to reduce sensitivity differences between different buttons;
- When the touch channel is conditional, a 1K~5K resistor should be connected in series, and the resistor should be placed close to the MCU touch channel pin;
- The distance between each touch PAD should be as large as possible (greater than 3mm), and the projection area of the touch button should be hollowed out. It is strongly recommended not to place components and routing that are not part of the TK network, and the distance between the routing of different touch channels should be maintained at more than twice the line width (recommended to keep above 0.5mm);
- The connection from the touch button should be as short and thin as possible, with a recommended line width of 6-15mil (the thinner, the better, if the PCB manufacturing process allows). It is not recommended to have a line width greater

than 0.3mm, and the shorter the line length, the better (length should not exceed 300mm);

- The front and back of the touch button should avoid passing through jumpers or routing of other networks as much as possible;
- Functionality can be simulated for reference, but sensitivity must be tested on the actual board;

11. CMP Comparator

The JZ8PT2503/4 has a built-in hardware comparator that can compare any two of the input pin, internal resistor divider V_{internal R}, and Vref, selecting one as the positive input and the other as the negative input. The negative input of the comparator can be P62, P60, P63, P65, the divider resistor (selected by CMPRS<5:0>), or Vref. When Vref is selected as the input, the internal reference voltage is selected through the TKVS register TKVS<2:0>. The positive input of the comparator can be P61, P65, the divider resistor (selected by CMPRS<5:0>), or Vref. (The same port cannot be used as both positive and negative inputs simultaneously, and the divider resistor input source cannot be used as both positive and negative at the same time.)

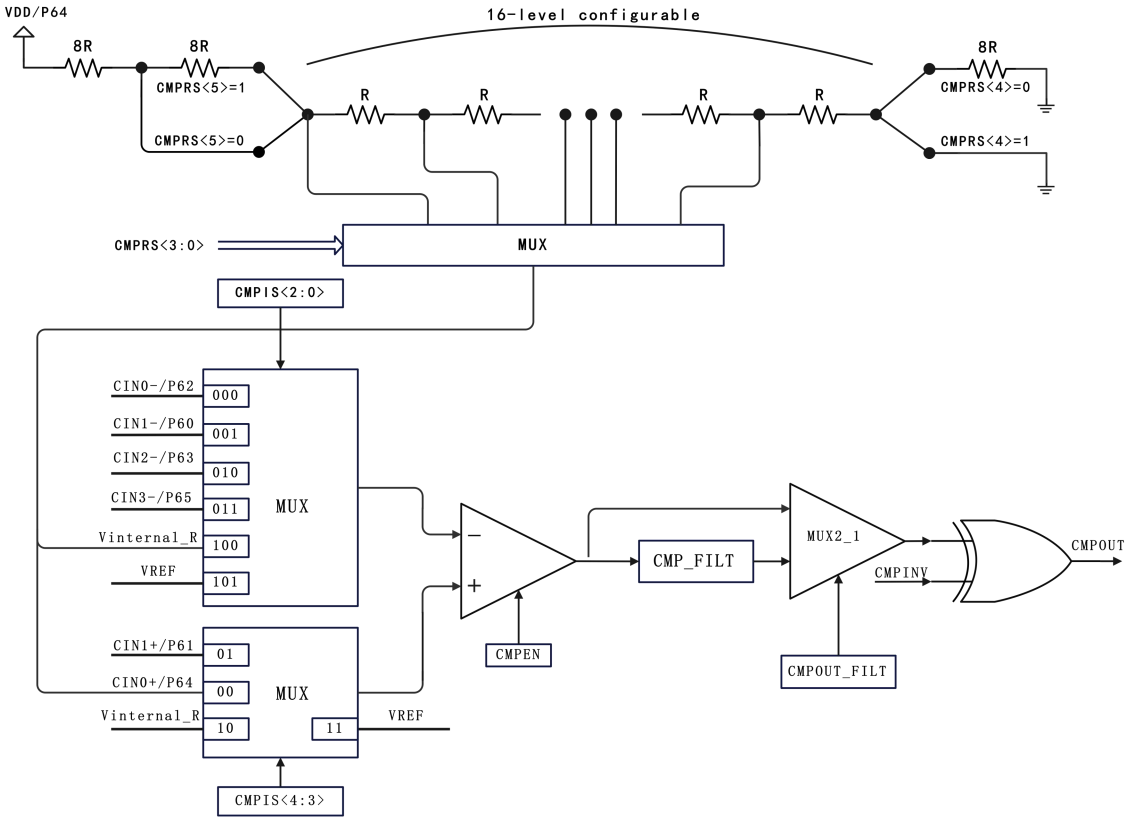
The divider resistor can be configured through the CMPCON control register to select the input voltage source as either the P64 port input or VDD.

The output result of the comparator can be selected to output from the P60 port, supporting output inversion. The chip supports digital filtering of the output result, which can be selected in OPTION. When not outputting, the CMPOUT status bit can be checked.

The comparator supports triggering interrupts based on output result changes, enabling CMPIE to generate interrupt signals.

The comparator supports output result change wake-up, enabling CMPWE to wake up from idle mode and sleep mode. In idle mode and sleep mode, if CMPEN is enabled, it will enable the low-speed oscillator, increasing sleep power consumption.

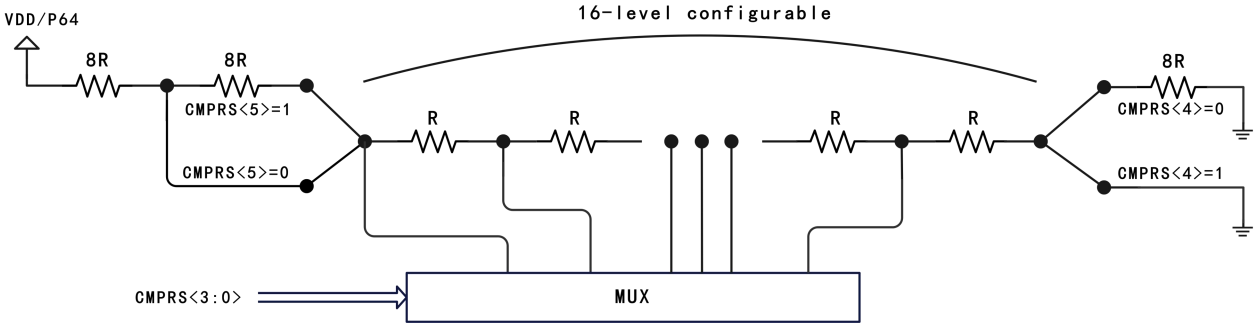
The comparator allows the selection of the comparator hysteresis function level in the 【OPTION】, and the hysteresis function is only effective on the falling edge of the comparison result.



Comparator Schematic Explanation

11.1 Voltage output Vinternal R from the voltage divider resistor

The voltage output Vinternal R is composed of a series of resistors, which can generate different levels of reference voltage. CMPRS<5:0> collectively determines the magnitude of Vinternal R. CMPRS<5> and CMPRS<4> select the maximum and minimum values of Vinternal R, while CMPRS<3:0> is used to select the desired voltage level, which is divided into 16 equal parts between the maximum and minimum values of Vinternal R, chosen by CMPRS<3:0>.



Comparator Calibration Diagram

Example 1: CMPRS<5>=0, CMPRS<4>=0

Value range: $V_{\text{internal R}} = (3/4) * \text{VDD} \sim (1/4) * \text{VDD} + (1/32) * \text{VDD}$

Calculation formula:$V_{\text{internal R}} = (1/4) * VDD + \frac{(n+1)}{32} * VDD$

Example 2: CMPRS<5>=0, CMPRS<4>=1

Value range:$V_{\text{internal R}} = (2/3) * VDD \sim (1/24) * VDD$

Calculation formula:$V_{\text{internal R}} = \frac{(n+1)}{24} * VDD$

Example 3: CMPRS<5>=1, CMPRS<4>=0

Value range:$V_{\text{internal R}} = (3/5) * VDD \sim (1/5) * VDD + (1/40) * VDD$

Calculation formula:$V_{\text{internal R}} = (1/5) * VDD + \frac{(n+1)}{40} * VDD$

Example 4: CMPRS<5>=1, CMPRS<4>=1

Value range:$V_{\text{internal R}} = (1/2) * VDD \sim (1/32) * VDD$

Calculation formula:$V_{\text{internal R}} = \frac{(n+1)}{32} * VDD$

n=CMPRS<3:0>

11.2 Comparator Function Configuration

When using the comparator, CMPEN must be enabled (this will activate the ILRC used for filtering the output result CMPOUT, which will increase power consumption). Set CMPIS<5:0> to select the positive and negative input sources, and configure the positive and negative ports as inputs. The same port cannot be used as both positive and negative inputs simultaneously, and the voltage divider resistor input source cannot be used as both positive and negative at the same time.

If a resistor divider is selected as the input source, configure the CMPRS<5:0> register as needed to select the desired voltage output V_internal R for comparison.

Example 1:

Select P62 as the negative input and V_internal R voltage as (18/32)*VDD for the positive input. Choose the configuration with V_internal R set to CMPRS<5>=0, CMPRS<4>=0, and CMPRS<3:0>=4b’1001 (n=9) to obtain

V_internal R = (1/4)*VDD + [(9+1)/32]*VDD = (18/32)*VDD

Once the configuration is complete, enable Bit7 CMPEN of the control register CMPCON0 (R1C8) to start the comparison. The comparison result can be output through P60 by configuring Bit7 CMPOE of the control register CMPCON1 (R1C9) (P60 must be set as output). The output result can also be inverted by configuring Bit6 CMPINV of this control register.

11.3 RFC Resistor Frequency Conversion Description

JZ8PT2503/4 has a built-in RFC resistor frequency conversion function, which controls the TC0 count based on the comparison results of the comparator to achieve time counting of external voltage changes.

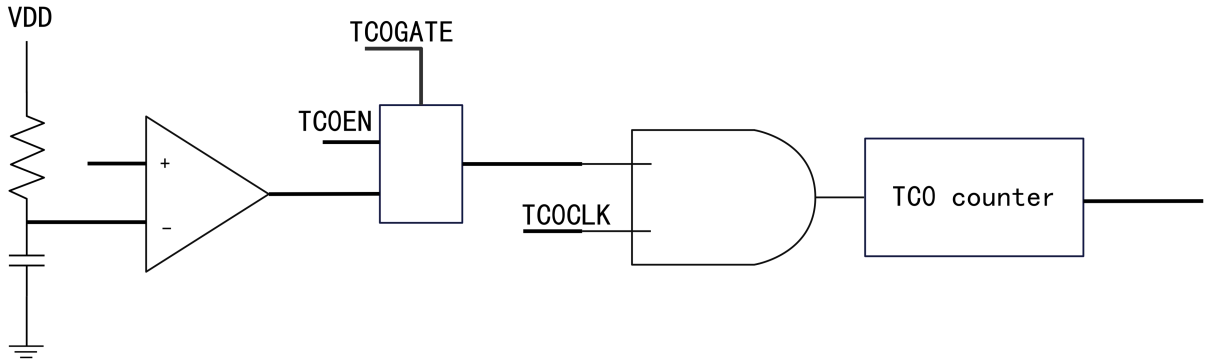
RFC Principle:

The change in voltage at the RFC port affects the output result of the comparator. When the TC0GATE<1> bit of the EXINTCON register is enabled, the TC0 count is controlled by the output result CMPOUT of the comparator. When the RFC port voltage is lower than the positive voltage of the comparator, CMPOUT=1 and TC0 starts counting; when the RFC port voltage is higher than the positive voltage of the

comparator, CMPOUT=0 and TC0 stops counting. The TC0 count value records the time it takes for the RFC port voltage to charge to the preset voltage value (the positive voltage of the comparator).

Application Steps:

1. Set the P6AE register to select the analog port of the comparator;
2. Set the CMPCON0 and CMPCON1 registers to define the positive input source of the comparator as a fixed voltage and the negative input source of the comparator as an external port (as shown in the diagram);
3. Set the TC0GATE<1> bit of the EXINTCON register, so that the TC0 count is controlled by the output result CMPOUT of the comparator;
4. Set the port output of the negative input source of the comparator to low level to discharge the port capacitor;
5. Clear the initial value of the TC0 timer;
6. Set the port of the negative input source of the comparator to an analog input port and start sampling the RFC port voltage;
7. Read the TC0 count value and calculate the charging time for the RFC port;



RFC Structure Description Diagram

11.4 Related Registers

11.4.1 R184/TC0CON (TC0 Control Register)

0X184	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CON	TC0EN	TC0CKS<1:0>		TC0EDG	TC0PTEN	TC0PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC0EN - TC0 Timer Count Enable Bit

0: Disable TC0

1: Enable TC0

Bit<6:5>: TC0CKS<1:0>-TC0 signal source selection bit

00: Instruction Clock

01: External Input Signal (P62)

10: System Clock

11: ILRC Clock (Low-Speed Oscillator)

Bit<4>: TC0EDG - TC0 Signal Edge Selection Bit

0: TC0 Pin Signal Changes from High to Low Increments by 1

1: TC0 Pin Signal Changes from Low to High Increments by 1

Bit<3>: TC0PTEN - Prescaler Enable Bit

0: Disable TC0 Prescaler

1: Enable TC0 Prescaler

Bit<2:0>: TC0PSR<2:0> - TC0 Prescaler Selection Control Bit:

TC0PSR<2>	TC0PSR<1>	TC0PSR<0>	TC0 Prescaler Coefficient
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

11.4.2 R185/TC0C (TC0 8-bit Counter Register)

0X185	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0C	TC0C<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

11.4.3 R1AD/TPRE (TC0 Prescaler)

0X1AD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TPRE	TPRE<7:0>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

11.4.4 R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	INT1S<1:0>		INT0S<1:0>		PWM2_PULSEEN	CAPS	TCOGATE<1:0>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<1>: TCOGATE<1> - TCO Capture Gate Enable Bit

0: Disable

1: Enable gate, CMPOUT as capture source

11.4.5 R1C4/TKVS (VREF Voltage Selection Register)

0X1C4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TKVS	TKCAPS<2:0>			TKVLS<1:0>		TKVS<2:0>		
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<4:3>: TKVLS<1:0> - VREF Comparison Voltage Selection Bit

TKVLS<1>	TKVLS<0>	Comparative Voltage
0	0	0.5*VCHG
0	1	0.625*VCHG
1	0	0.75*VCHG
1	1	0.875*VCHG

Bit<2:0>: TKVS<2:0>-VCHG Voltage Selection Bit

TKVS<2>	TKVS<1>	TKVS<0>	VCHG Voltage
0	0	0	1V
0	0	1	2V
0	1	0	3V
0	1	1	4V
1	0	0	VDD

11.4.6 R1C9/CMPCON0 (CMP Control Register 0)

0X1C8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON0	CMPEN	CMPOUT	CMPRS<5:0>					
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPEN - CMP Enable Control Bit

0: Disable

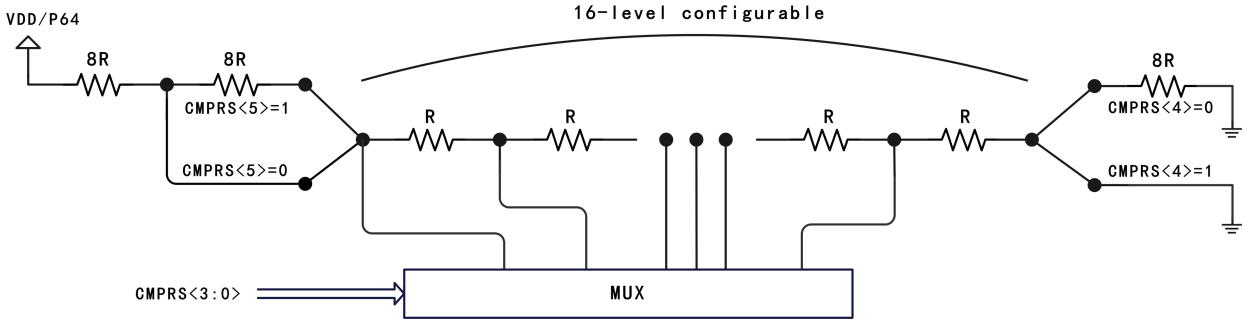
1: Enable

Bit<6>: CMPOUT-CMP result output bit

0: The positive voltage of the comparator is less than the negative voltage

1: The positive voltage of the comparator is greater than the negative voltage

Bit<5:0>: CMPRS<5:0> - Comparator adjustment bits



For example, when CMPCON1=0x17, the TKVS register TKVS<2:0> selects 2V, TKVLS<1:0> selects 0.5*VCHG, the positive side of the comparator selects VDD resistor divider, and the negative side of the comparator selects VREF (2V*0.5=1V). Different resistor divider levels CMPRS<5:0> correspond to different detection voltages, as shown in the table below:

CMPRS	Detection Voltage	CMPRS	Detection Voltage	CMPRS	Detection Voltage	CMPRS	Detection Voltage
00H	3.556	10H	24.000	20H	4.444	30H	32.000
01H	3.200	11H	12.000	21H	4.000	31H	16.000
02H	2.909	12H	8.000	22H	3.636	32H	10.667
03H	2.667	13H	6.000	23H	3.333	33H	8.000
04H	2.462	14H	4.800	24H	3.077	34H	6.400
05H	2.286	15H	4.000	25H	2.857	35H	5.333
06H	2.133	16H	3.429	26H	2.667	36H	4.571
07H	2.000	17H	3.000	27H	2.500	37H	4.000
08H	1.882	18H	2.667	28H	2.353	38H	3.556
09H	1.778	19H	2.400	29H	2.222	39H	3.200
0AH	1.684	1AH	2.182	2AH	2.105	3AH	2.909
0BH	1.600	1BH	2.000	2BH	2.000	3BH	2.667
0CH	1.524	1CH	1.846	2CH	1.905	3CH	2.462
0DH	1.455	1DH	1.714	2DH	1.818	3DH	2.286
0EH	1.391	1EH	1.600	2EH	1.739	3EH	2.133
0FH	1.333	1FH	1.500	2FH	1.667	3FH	2.000

Note: The gray part is prohibited for voltage detection.

11.4.7 R1CA/CMPCON1 (CMP Control Register 1)

0X1CA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON1	CMPOE	CMPINV	CMPIS<5:0>					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPOE - Comparator result output enable

0:P60 as GPIO

1: Comparator result output from P60

Bit<6>: CMPINV-CMPOUT output result inverted

0: No inversion

1: Inversion

Bit<5>: CMPIS<5> - Voltage input from voltage divider resistor

0: VDD

1: P64 input

Bit<4:3>: CMPIS<4:3> - Comparator positive input source selection

CMPIS<4>	CMPIS<3>	Positive Input Source
0	0	CIN0+/P61
0	1	CIN1+/P64
1	0	Resistor Voltage Divider
1	1	VREF

Bit<2:0>: CMPIS<2:0> - Negative Input Source Selection for Comparator

CMPIS<2>	CMPIS<1>	CMPIS<0>	Negative Input Source
0	0	0	CIN0-/P62
0	0	1	CIN1-/P60
0	1	0	CIN2-/P63
0	1	1	CIN3-/P65
1	1	0	Resistor Voltage Divider
1	1	1	VREF

12. OPTION Configuration Table

CODE OPTION	Option	Function Description
Watchdog	Enable	Watchdog WDT Enable
	Disable	Watchdog WDT disabled
Clocks Division	2 Clocks	Instruction Clock Division Select 2 Clocks
	4 Clocks	Instruction Clock Division Select 4 Clocks
	8 Clocks	Instruction Clock Division Select 8 Clocks
	16 Clocks	Instruction Clock Division Select 16 Clocks
	32 Clocks	Instruction Clock Division Select 32 Clocks
IRC Frequency	1M	IRC frequency selection 1M
	4M	IRC frequency selection 4M
	8M	IRC frequency selection 8M
	16M	IRC frequency selection 16M
Low voltage reset option	Enable: LVR always	Default LVR function is always enabled
	Enable: Software control	LVR enable bit is software configurable
Low voltage reset	LVR=1.8V	Low voltage reset point selection 1.8V
	LVR=2.0V	Low Voltage Reset Point Selection 2.0V
	LVR=2.2V	Low Voltage Reset Point Selection 2.2V
	LVR=2.4V	Low Voltage Reset Point Selection 2.4V
	LVR=2.7V	Low Voltage Reset Point Selection 2.7V
	LVR=3.0V	Low Voltage Reset Point Selection 3.0V
	LVR=3.3V	Low Voltage Reset Point Selection 3.3V
	LVR=3.6V	Low voltage reset point selection 3.6V
	Disable	Disable LVR function, for testing only, not for mass production
OTP page selection	Use 2K	ROM selection 2K storage space
	Use first 1K	ROM selection first 1K storage space
	Use last 1K	ROM selection last 1K storage space
P63 pull-up	Disable	Pull-up on P63 port is prohibited
	Enable	P63 port pull-up enable
P63 port	RST	P63 port as external reset port
	GPIO	P63 port as general input/output port
P64 port	as instruction clock output port	P64 port as instruction clock output port, program cannot control
	as GPIO	P64 port as general input/output port
Reset Time (WDT Prescaler Selection Default Value)	PWRT=4.5ms WDT=8.5ms	Reset Setup Time=4.5ms, WDT Overflow Time=8.5ms
	PWRT=16ms, WDT=32ms	Reset Setup Time=16ms, WDT Overflow Time=32ms
	PWRT=64ms, WDT=128ms	Reset Setup Time=64ms, WDT Overflow Time=128ms
	PWRT=256ms, WDT=512ms	Reset establishment time = 256ms, WDT overflow time = 512ms

	PWRT=350us WDT=8.5ms	Reset establishment time=350us, WDT overflow time=8.5ms
	PWRT=350us WDT=32ms	Reset establishment time=350us, WDT overflow time=32ms
	PWRT=350us WDT=128ms	Reset establishment time=350us, WDT overflow time=128ms
	PWRT=350us WDT=512ms	Reset establishment time=350us, WDT overflow time=512ms
CMP_FILT	Enable	Comparator result digital filtering enable
	Disable	Comparator result digital filtering prohibited
Comparator hysteresis (Offset voltage)	20mV	The comparator hysteresis voltage is 20mV
	40mV	The comparator hysteresis voltage is 40mV
	60mV	The comparator hysteresis voltage is 60mV
	80mV	The comparator hysteresis voltage is 80mV

13. Instruction Set

Instruction	Instruction Action	Flag Impact
ADD A,R	A+R→A	Z,C,DC
ADD R,A	A+R→R	Z,C,DC
AND A,R	A&R→A	Z
AND R,A	A&R→R	Z
CLRA	0→A	Z
CLR R	0→R	Z
INVA R	/R→A	Z
INV R	/R→R	Z
DA	A register adjusted to BCD value	C
DECA R	R-1→A	Z
DEC R	R-1→R	Z
DJA R	R-1→A, skip if zero	-
DJ R	R-1→R, skip if zero	-
INCA R	R+1→A	Z
INC R	R+1→R	Z
IJA R	R+1→A, skip if zero	-
IJ R	R+1→R, skip if zero	-
MOV R,A	A→R	-
MOV A,R	R→A	Z
MOV R,R	R→R	Z
OR A,R	A∨VR→A	Z
OR R,A	A∨VR→R	Z
SUB A,R	R-A→A	Z,C,DC
SUB R,A	R-A→R	Z,C,DC
XOR A,R	A⊕R→A	Z
XOR R,A	A⊕R→R	Z
BTC R,b	0→R(b)	-
BTS R,b	1→R(b)	-
JBTC R,b	if R(b)=0, skip	-
JBTS R,b	if R(b)=1, skip	-
LCR R	R(n)→R(n+1),R(7)→C, C→R(0)	C
LCA R	R(n)→A(n+1),R(7)→C, C→A(0)	C

RCR R	R(n)→R(n-1),R(0)→C, C→R(7)	C
RCA R	R(n)→A(n-1),R(0)→C, C→A(7)	C
SWAP R	R(0-3) ↔ R(4-7)	-
SWAPA R	R(0-3)→A(4-7),R(4-7)→A(0-3)	-
ADD A,k	A+k→A	Z,C,DC
AND A,k	A&k→A	Z
MOV A,k	k→A	-
OR A,k	A∨k→A	Z
SUB A,k	k-A→A	Z,C,DC
XOR A,k	A⊕k→A	Z
CALL k	PC+1→[SP], (Page,k)→PC	-
DI	Disable Interrupt	-
EI	Enable Interrupt	-
JMP k	K (Page,k)→PC	-
NOP	No Operation	-
RET	[Top of Stack]→PC	-
RETI	[Top of Stack]→PC, Enable Interrupt	-
RETL k	k→A,[stack top]→PC	-
SLEEP	0→WDT, oscillator stops oscillating (sleep mode)	T,P
CWDT	0→WDT	T,P
TBRD R	Machine code bit7～0 to ACC Machine code bit15～8 to R (general-purpose register)	-

14. Electrical characteristics

14.1 Limit parameters

Operating temperature..... -40℃～85℃
Storage temperature..... -65℃～150℃
Input voltage..... Vss-0.3V～Vdd+0.5V
Output voltage..... Vss-0.3V～Vdd+0.5V
Operating voltage..... 1.8V～5.5V

14.2 DC electrical characteristics

(VDD =5V, operating temperature=25℃, unless otherwise specified)

Symbol	Parameter description	Condition	Minimum	Typical	Maximum	Unit
IRC1	IRC1 (after calibration)	OPTION select 16MHz	-	16	-	MHz
IRC2	IRC2 (after calibration)	OPTION select 8MHz	-	8	-	MHz
IRC3	IRC3 (after calibration)	OPTION select 4MHz	-	4	-	MHz
IRC4	IRC4 (after calibration)	OPTION select 1MHz	-	1	-	MHz
IRC5	IRC5 (after calibration)	OPTION select 910KHz	-	910	-	KHz
IOH1	Output high-level drive (except P63)	Ioh=4.4V	16	17	18	mA
IOH2	Output high-level drive (P63)	Ioh=4.4V	21	22	23	mA
IOL2	Output low-level drive	Iol=0.6V	26	30	32	mA
IPH	Pull-up resistor	Pull-up enabled, input grounded	50	55	60	kΩ
IPD	Pull-down resistor	Pull-down enabled, input connected to VDD	50	55	60	kΩ
Isb1	Shutdown current 1	Input connected to VDD, output floating	-	-	1	μA
Isb2	Shutdown Current 2	Connect input to VDD, output floating, WDT enabled	-	-	10	μA
Isb3	Shutdown current 3	Connect input to VDD, output floating, CMP enabled	-	14	-	μA
Iop1	Operating current 1 (VDD=5V)	IRC=16MHz 4clock	-	-	2	mA
Iop2	Operating current 2 (VDD=5V)	IRC=1MHz 2clock	-	0.25	-	mA
LVR	Low Voltage Reset (1M/32T)	Select LVR Reset Point	Vlvr-0.2	Vlvr	Vlvr+0.2	V

14.3 VREF Characteristics

(VDD = 5V, VSS = 0V, Ta = -40 to 85℃)

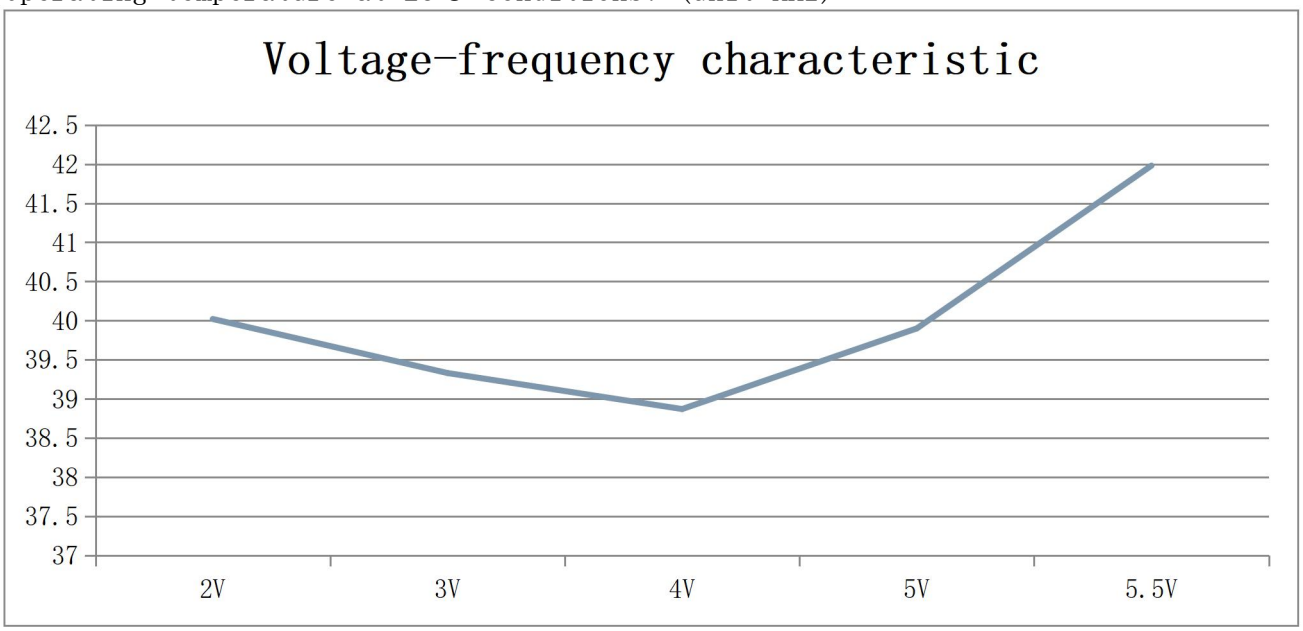
Symbol	Parameter description	Condition	Minimum	Typical	Maximum	Unit
VDD	Supply Voltage	-	2.2	-	5.5	V
IVDD	DC supply current	No load	-	-	250	μA
VREF	Reference voltage output	1V, 2V, 3V, 4V	-	±1	1.75	%
Warm up Time	Reference voltage preparation time	VDD=VDDmin-5.5V ,Cload=19.2pf, Rload-15.36KΩ	-	38	50	μs
VDDmin	Minimum supply voltage	-	-	VREF+0.2	-	V

14.4 Characteristic curve diagram

The curves listed in this chapter are for design reference only. Some of the data provided may exceed the specified operating range of the chip. To ensure the normal operation of the chip, please strictly refer to the electrical characteristics description.

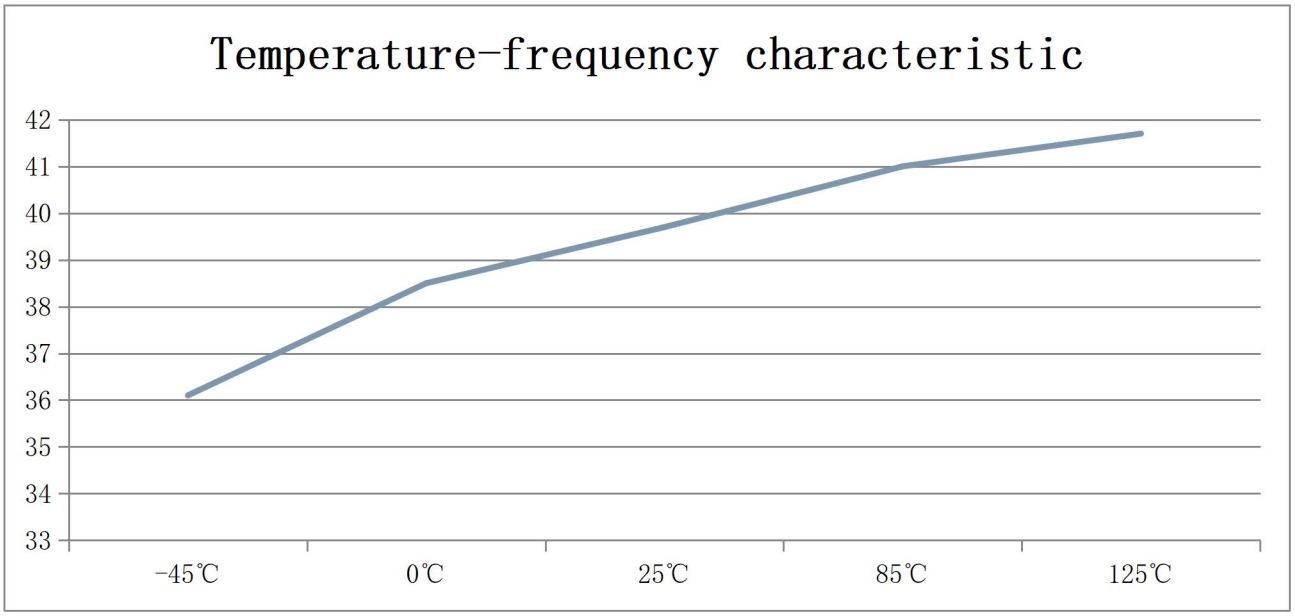
14.4.1 Internal low-speed oscillator - frequency characteristic curve

Operating temperature at 25℃ conditions: (unit KHz)



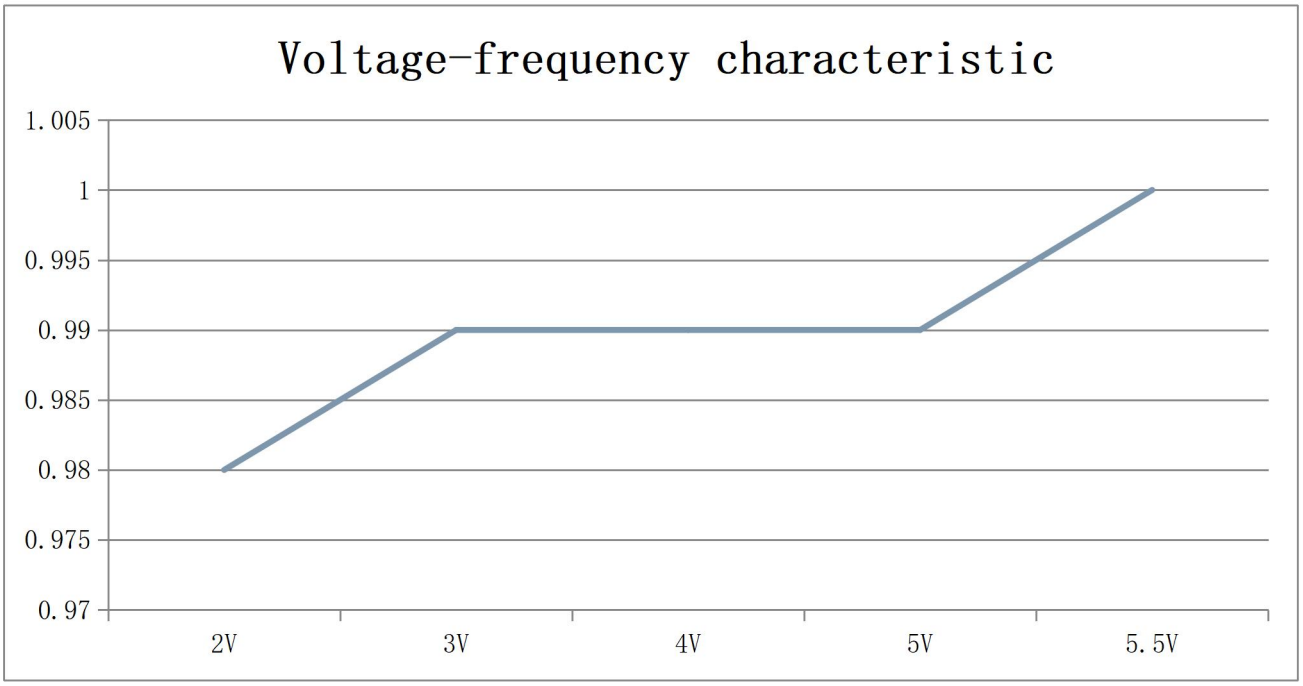
14.4.2 Internal Low-Speed Oscillator - Temperature Frequency Characteristic Curve

Operating Voltage at 5V Condition: (Unit KHz)



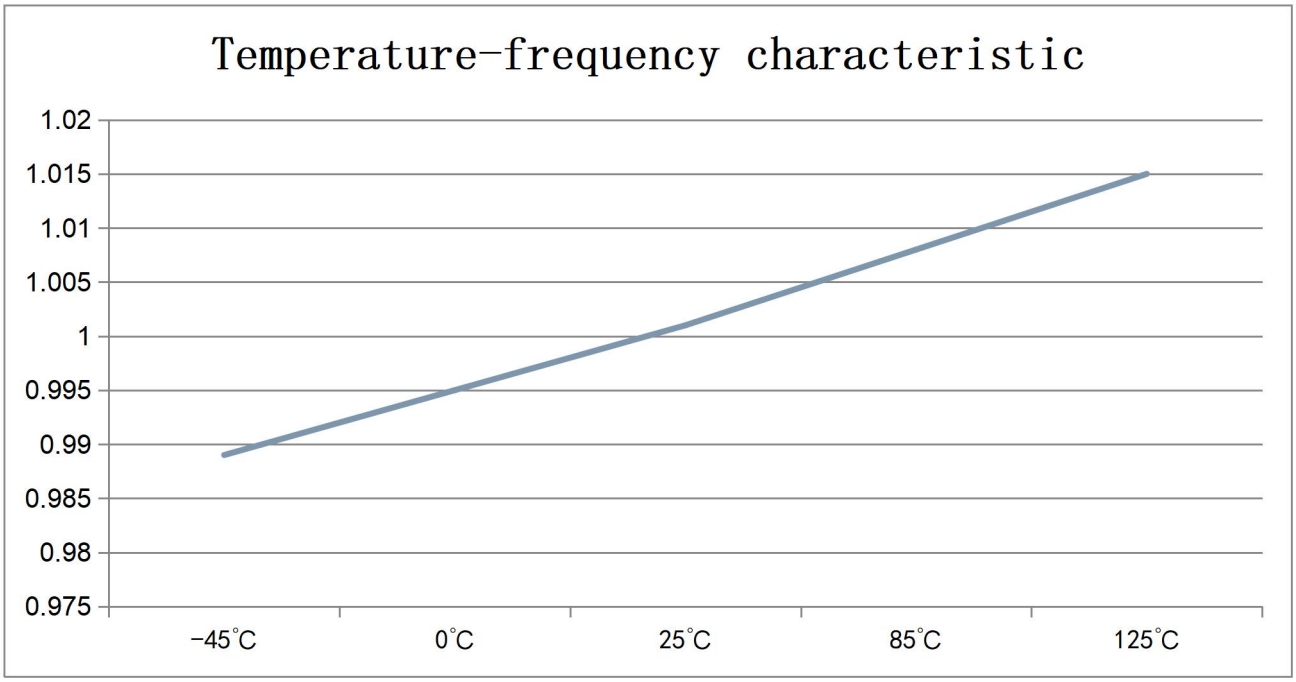
14.4.3 Internal 1MHz RC Oscillator - Pressure Frequency Characteristic Curve

Operating Temperature at 25℃ Condition: (Unit MHz)



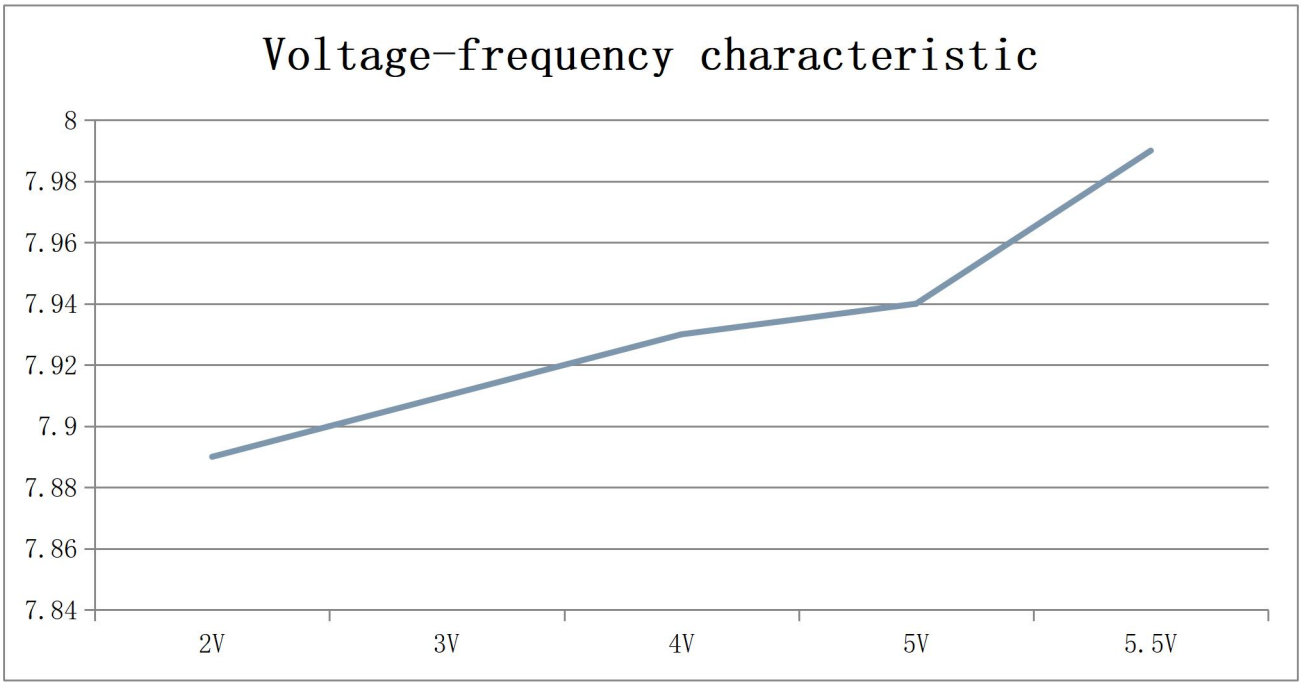
14.4.4 Internal 1MHz RC Oscillator - Temperature Frequency Characteristic Curve

Operating Voltage at 5V Condition: (Unit MHz)



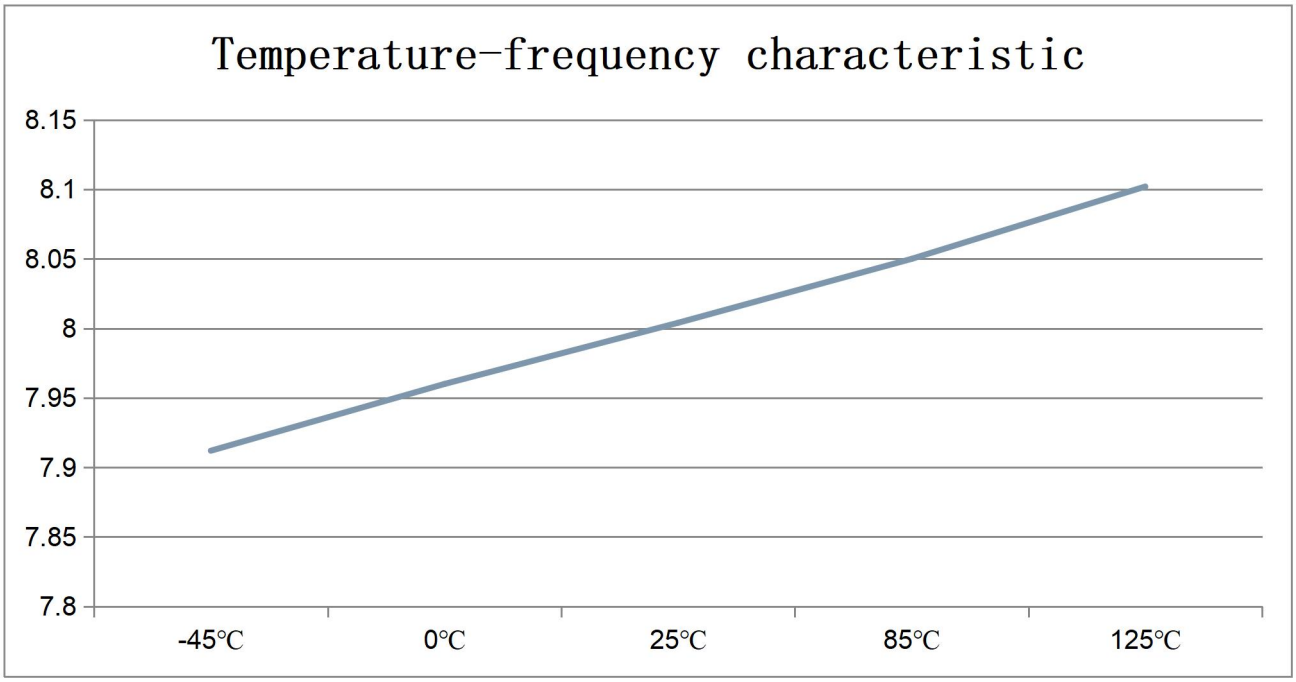
14.4.5 Internal 8MHz RC Oscillator - Pressure Frequency Characteristic Curve

Operating Temperature at 25℃ Condition: (Unit MHz)



14.4.6 Internal 8MHz RC Oscillator - Temperature Frequency Characteristic Curve

Operating Voltage at 5V Condition: (Unit MHz)



14.5 IHRC Frequency Fine-Tuning Parameter Description

The parameter description is for reference only regarding the trend of changes, and there may be deviations in practice.

IHRCCAL Adjustment Value (Hexadecimal)	IHRC 8MHz Adjustment Ratio (Percentage based on 8MHz)
00	-32.04%
01	-31.84%
02	-31.58%
03	-31.39%
04	-31.06%
05	-30.86%
06	-30.59%
07	-30.39%
08	-30.01%
09	-29.80%
0A	-29.54%
0B	-29.33%
0C	-28.98%
0D	-28.76%
0E	-28.48%
0F	-28.28%
10	-27.96%
11	-27.74%
12	-27.44%
13	-27.21%
14	-26.86%
15	-26.63%
16	-26.31%
17	-26.10%
18	-25.68%
19	-25.43%
1A	-25.11%
1B	-24.88%
1C	-24.49%
1D	-24.25%
1E	-23.93%
1F	-23.70%
20	-23.61%
21	-23.35%
22	-23.03%
23	-22.78%
24	-22.38%
25	-22.11%
26	-21.76%
27	-21.50%

28	-21.03%
29	-20.75%
2A	-20.40%
2B	-20.13%
2C	-19.69%
2D	-19.40%
2E	-19.03%
2F	-18.76%
30	-18.38%
31	-18.08%
32	-17.66%
33	-17.38%
34	-16.93%
35	-16.63%
36	-16.21%
37	-15.93%
38	-15.36%
39	-15.06%
3A	-14.65%
3B	-14.34%
3C	-13.83%
3D	-13.50%
3E	-13.46%
3F	-13.14%
40	-13.09%
41	-12.79%
42	-12.73%
43	-12.39%
44	-11.88%
45	-11.53%
46	-11.09%
47	-10.76%
48	-10.15%
49	-9.78%
4A	-9.33%
4B	-8.98%
4C	-8.41%
4D	-8.04%
4E	-7.55%
4F	-7.19%
50	-6.69%
51	-6.30%
52	-5.81%
53	-5.41%
54	-4.80%

55	-4.40%
56	-3.86%
57	-3.45%
58	-2.75%
59	-2.30%
5A	-1.75%
5B	-1.31%
5C	-0.68%
5D	-0.22%
5E	0.34%
5F	0.76%
60	0.85%
61	1.30%
62	1.89%
63	2.35%
64	3.05%
65	3.54%
66	4.14%
67	4.64%
68	5.45%
69	5.98%
6A	6.61%
6B	7.14%
6C	7.90%
6D	8.44%
6E	9.14%
6F	9.66%
70	10.33%
71	10.91%
72	11.60%
73	12.15%
74	12.98%
75	13.58%
76	14.33%
77	14.90%
78	15.90%
79	16.54%
7A	17.33%
7B	17.96%
7C	18.90%
7D	19.58%
7E	20.39%
7F	21.03%
80	-1.30%
81	-1.03%

82	-0.66%
83	-0.36%
84	0.09%
85	0.36%
86	0.76%
87	1.04%
88	1.57%
89	1.86%
8A	2.26%
8B	2.60%
8C	3.09%
8D	3.42%
8E	3.81%
8F	4.10%
90	4.53%
91	4.89%
92	5.35%
93	5.70%
94	6.20%
95	6.59%
96	7.01%
97	7.36%
98	7.93%
99	8.31%
9A	8.76%
9B	9.13%
9C	9.65%
9D	10.03%
9E	10.50%
9F	10.84%
A0	10.89%
A1	11.28%
A2	11.74%
A3	12.09%
A4	12.65%
A5	13.03%
A6	13.51%
A7	13.88%
A8	14.53%
A9	14.96%
AA	15.46%
AB	15.86%
AC	16.50%
AD	16.91%
AE	17.45%

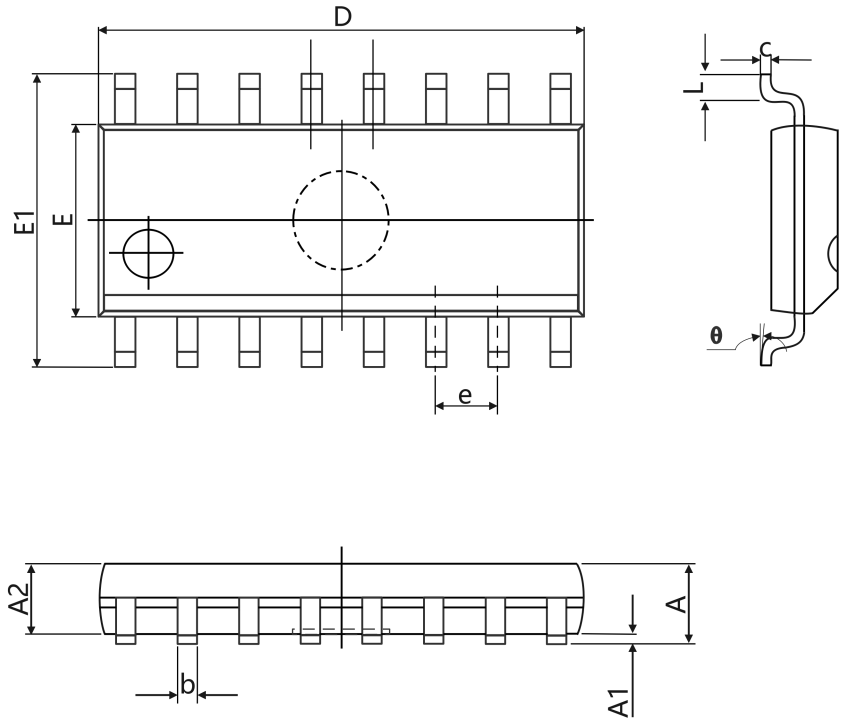
AF	17.84%
B0	18.38%
B1	18.81%
B2	19.35%
B3	19.79%
B4	20.48%
B5	20.91%
B6	21.49%
B7	21.93%
B8	22.65%
B9	23.13%
BA	23.70%
BB	24.15%
BC	24.81%
BD	25.25%
BE	25.38%
BF	25.88%
C0	25.88%
C1	26.38%
C2	26.50%
C3	27.00%
C4	27.63%
C5	28.13%
C6	28.75%
C7	29.25%
C8	30.13%
C9	30.63%
CA	31.25%
CB	31.88%
CC	32.63%
CD	33.13%
CE	33.88%
CF	34.38%
D0	35.13%
D1	35.63%
D2	36.38%
D3	37.00%
D4	37.75%
D5	38.38%
D6	39.13%
D7	39.75%
D8	40.75%
D9	41.38%
DA	42.13%
DB	42.75%

DC	43.75%
DD	44.38%
DE	45.25%
DF	45.88%
E0	45.88%
E1	46.63%
E2	47.38%
E3	48.13%
E4	49.13%
E5	49.75%
E6	50.63%
E7	51.38%
E8	52.50%
E9	53.25%
EA	54.25%
EB	55.00%
EC	56.13%
ED	56.88%
EE	57.75%
EF	58.63%
F0	59.50%
F1	60.38%
F2	61.38%
F3	62.25%
F4	63.38%
F5	64.25%
F6	65.38%
F7	66.25%
F8	67.63%
F9	68.63%
FA	69.75%
FB	70.75%
FC	72.00%
FD	72.88%
FE	74.00%
FF	75.00%

15. Package Size

15.1 16PIN Package Size

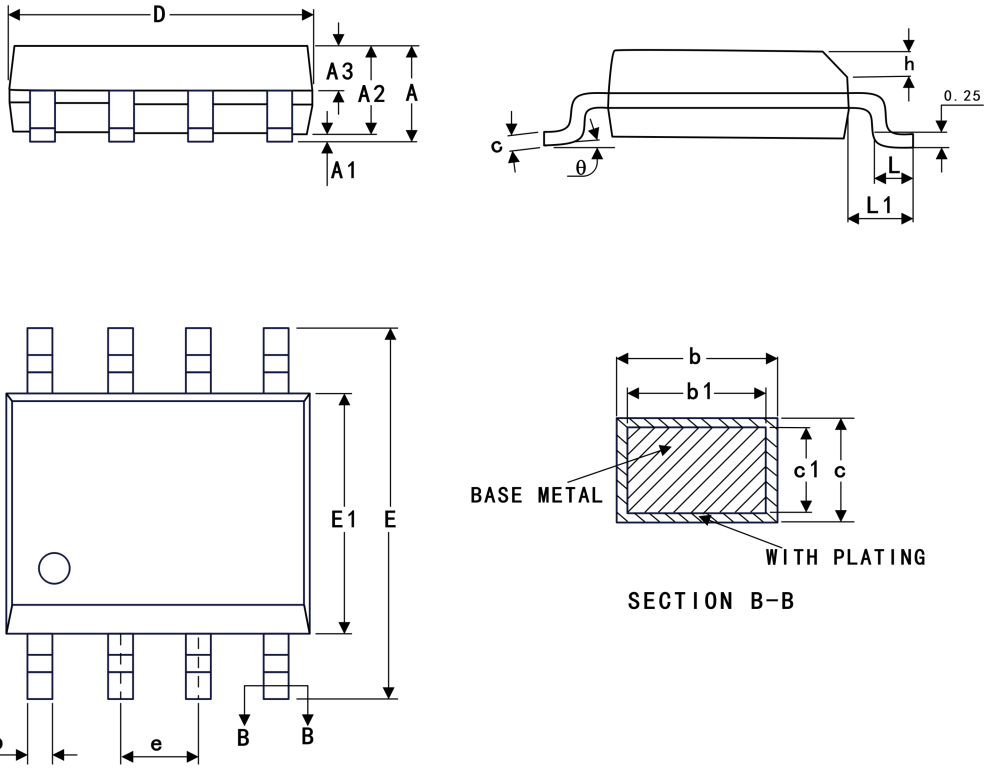
SOP16 (mm)



SYMBOL	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

15.2 8PIN package size

SOP8 (mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	-	0.50
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	-	8°