JZ8M2632

8-bit MTP Microcontroller

User Data Manual

Version V2.4

Disclaimer

Wuxi Jinzer Technology Co., Ltd. (hereinafter referred to as Wuxi Jinzer Technology) reserves the right to further explain improvements regarding the reliability, functionality, and design of the products in this specification. Wuxi Jinzer Technology is not obligated to be responsible for any direct, indirect, special, or consequential damages resulting from the use of the information or content in this user manual. The applications mentioned in this user manual are for illustrative purposes only, and the company does not guarantee that these applications are applicable without further testing. The software mentioned in this specification (if any) is legally provided under authorization or confidentiality agreements and may only be used or copied under the terms of those agreements. Wuxi Jinzer Technology's products are not specifically designed for use in life-supporting devices, apparatus, or systems. Wuxi Jinzer Technology's products do not support and prohibit applications in these areas. The content of this user manual is subject to change without notice. For specific update information, please refer to the company's official website www.wxjzkj.com.

Modification Record Description

Version Number	Modification Description	Remarks
V1.0	Release of the initial version	
V1.1	Corrected the description of PWM function and low-speed clock frequency, revised the pinout diagram for SOP8, added SOP14 pinout	
V1.2	Revised option settings and on-board programming instructions	
V1.3	Added notes on option [Power-up time selection] and QFN16 pinout, modified AD conversion time description	
V1.4	Corrected the pinout diagram for SOP8, added chip notes	
V1.5	Corrected description errors	
V1.6	Modified the description of the programming pins	
V1.7	Added pinout diagram for JZ8M2632B	
V1.8	Modified the pinout diagram for JZ8M2632B and added pinout diagram for JZ8M2632C	
V1.9	Corrected description errors and rearranged LED numbers	
V2.0	Corrected description errors	
V2.1	Added JZ8M2632B _SOP14 pinout	
V2.2	Changed JZ8M2632B _SOP14 model to JZ8M2632A_SOP14	
V2.3	Corrected error description and added notes on EEPROM storage AD adjustment values	
V2.4	Changed special pin name to JZ8M2632_xx X , added JZ8M2632_SOP16B pinout	

Notes:

1、When using the PWM2 duty cycle interrupt, the PWM2EN bit must be enabled in order to enter the interrupt normally.

2、Before sleeping, the AD reference must be switched to VDD; otherwise, there will be power consumption.

3. Precautions for programming option [Power-up Time Selection]:

1) If [Power-up Time Selection] is set to [Fast Power-up], then [Reset Time] can be chosen arbitrarily;

2) If [Power-up Time Selection] is set to [Slow Power-up], then [Reset Time] must be one of [PWRT=13ms/51ms/205ms];

3) If during the first programming, [Power-up Time Selection] is set to [Fast Power-up] + [PWRT=350us], and during the second programming, [Power-up Time Selection] is desired to be [Slow Power-up], then it is necessary to first program "[Fast Power-up] + [PWRT=13ms]" once (the purpose is to program the chip with a long reset time), and then select [Slow Power-up] for programming;

4. The four addresses 0XFF/0XFE/0XFD/0XFC of EEPROM are used for internal storage, with 0XFF/0XFE storing the reference voltage benchmark value of 2V. 0XFD/0XFC stores the 0.254VDD channel value; for specific usage, please consult FAE.

Table of Contents

1 Chip Introduction 8
1.1 Functional Characteristics 8
1.2 Pin Assignment 9
1.3 Pin Description 13
1.4 System Block Diagram 15
2 Memory Structure 16
2.1 Program Storage Area Structure 16
2.2 Data Storage Area 17
2.2.1 Data Storage Area Structure 17
2.2.2 Overview of Special Function Registers 17
3 Function Description 18
3.1 Operation Register 18
3.1.1 R180/RSR (RAM Select Register) 18
3.1.2 R181/PCH (Program Counter High Register) 18
3.1.3 R182/PCL (Program Counter Low Register) 18
3.1.4 R183/STATUS (Status Flag Register) 20
3.1.5 R184/TC0CON (TC0 Control Register) 21
3.1.6 R185/TC0C (TC0 8-bit Counter Register) 22
3.1.7 R186/TBRDH (Table Pointer High Register) 22
3.1.8 R187/TBRDL (Table pointer low register) 22
3.1.9 R188/CPUCON (CPU mode control register) 22
3.1.10 R189/IHRCCAL (IHRC frequency calibration register) 23
3.1.11 R18A/P5 (P5 Data Register) 24
3.1.12 R18B/P6 (P6 Data Register) 24
3.1.13 R18D/P5CON (P5 Control Register) 24
3.1.14 R18E/P6CON (P6 control register) 24
3.1.15 R190/P5PH (P5 pull-up control register) 25
3.1.16 R191/P6PH (P6 pull-up control register) 25
3.1.17 R193/P5PD (P5 pull-down control register) 25
3.1.18 R194/P6PD (P6 pull-down control register) 25
3.1.19 R19C/P5IWE (P5 input change interrupt, wake-up enable register) 26
3.1.20 R19D/P6IWE (P6 Input Change Interrupt, Wake-up Enable Register) 26
3.1.21 R1A0/P5AE (P5 analog port enable register) 26
3.1.22 R1A1/P6AE (P6 analog port enable register) 26
3.1.23 R1A3/ADATH (ADC data high 8-bit register) 27
3.1.24 R1A4/ADATL (ADC data low 8-bit register) 27
3.1.25 R1A6/ADCON0 (ADC Control Register 0) 27
3.1.26 R1A7/ADCON1 (ADC Control Register 1) 28
3.1.27 R1AD/TPRE(TC0 Pre-divider) 29
3.1.28 R1AE/EXINTCON (External Interrupt Control Register) 29
3.1.29 R1AF/WDTCON (WDT, external interrupt control register) 30
3.1.30 R1B0/TC1CON (TC1 Control Register) 31

3.1.31 R1B1/TC1PRDL (TC1/PWM123 Period Low 8-bit Register) 31
3.1.32 R1B2/PWM1DTL (PWM1 Duty Cycle Low 8-bit Register) 32
3.1.33 R1B3/PWM2DTL (PWM2 Duty Cycle Low 8-bit Register) 32
3.1.34 R1B4/PWM3DTL (PWM3 Duty Cycle Low 8-bit Register) 32
3.1.35 R1B5/TC1PRDTH (TC1/PWM123 Period High 4-bit and PWM3 Duty Cycle High 4-bit Register) 32
3.1.36 R1B6/PWM21DTH (PWM21 duty cycle high 4 bits register) 32
3.1.37 R1B7/PWMCON1 (PWM control register 1) 33
3.1.38 R1B8/TC2CON(TC2 Control Register) 34
3.1.39 R1B9/TC2PRDL(TC2/PWM456 Low 8-bit Period Register) 35
3.1.40 R1BA/PWM4DTL(PWM4 Duty Cycle Low 8-bit Register) 35
3.1.41 R1BB/PWM5DTL(PWM5 Duty Cycle Low 8-bit Register) 35
3.1.42 R1BC/PWM6DTL (PWM6 low 8 bits duty cycle register) 35
3.1.43 R1BD/TC2PRDTH (TC2/PWM456 high 4 bits of period and PWM6 high 4 bits of duty cycle register) 35
3.1.44 R1BE/PWM54DTH (PWM54 Duty Cycle High 4-bit Register) 36
3.1.45 R1BF/PWMCON2 (PWM Control Register 2) 36
3.1.46 R1C0/LEDRAM0 (LEDRAM register 0) 37
3.1.47 R1C1/LEDRAM1 (LEDRAM register 1) 37
3.1.48 R1C2/LEDRAM2 (LEDRAM Register 2) 37
3.1.49 R1C3/LEDRAM3 (LEDRAM Register 3) 38
3.1.50 R1C4/LEDRAM4 (LEDRAM Register 4) 38
3.1.51 R1C5/LEDRAM5 (LEDRAM Register 5) 38
3.1.52 R1C6/LEDCON (LED Control Register) 38
3.1.53 R1C7/LEDDT (LED Duty Cycle Register) 39
3.1.54 R1C8/CMPCON0 (CMP Control Register 0) 39
3.1.55 R1C9/CMPCON1 (CMP Control Register 1) 40
3.1.56 R1CA/E2PCON (EEPROM Control Register) 41
3.1.57 R1CB/E2PDATL (EEPROM Data Low 8-bit Register) 42
3.1.58 R1CC/E2PDATH (EEPROM Data High 8-bit Register) 42
3.1.59 R1D6/INTE0 (Interrupt Enable Control Register 0) 42
3.1.60 R1D7/INTE1 (Interrupt Enable Control Register 1) 43
3.1.61 R1DA/INTF0 (Interrupt Flag Register 0) 44
3.1.62 R1DB/INTF1 (Interrupt Flag Register 1) 45
3.1.63 R1FF/IAR (Indirect Addressing Register) 45
3.2 Interrupt 46
3.2.1 Interrupt Context Protection 47
3.3 Reset 48
3.3.1 Overview of Reset Function 48
3.3.2 POR Power-On Reset 48
3.3.3 WDT watchdog reset 49
3.3.4 LVR Low Voltage Reset 50
3.3.5 Relationship between operating frequency and LVR low voltage detection 51
3.4 Operating mode 53

3.4.1 High-speed mode 54
3.4.2 Low-speed mode 54
3.4.3 Idle mode 55
3.4.4 Sleep mode 55
3.5 System Clock 57
3.5.1 Internal IHRC Oscillator 57
3.5.2 Internal ILRC Oscillator 57
3.6 I/O port 58
3.6.1 GPIO internal structure diagram 58
3.6.2 Port input change wake-up 59
3.6.3 Port Schmitt parameters 59
3.7 Timer Counter 60
3.7.1 TC0 Timer Counter 60
3.7.1.1 TC0 Timer Setting Instructions 60
3.7.1.2 TC0 Timer Calculation Explanation 61
3.7.1.3 TC0 Idle Mode Wake-Up Description 61
3.7.2 TC1 Timer Counter 62
3.7.2.1 TC1 Timer Setting Description 63
3.7.2.2 TC1 Timing Calculation Description 63
3.7.2.3 TC1 Idle Mode Wake-up Description 63
3.7.3 TC2 Timer Counter 64
3.7.3.1 TC2 Timer Configuration Instructions 64
3.7.3.2 TC2 Timer Calculation Description 65
3.7.3.3 TC2 Idle Mode Wake-up Description 65
3.8 PWM Pulse Width Modulation 66
3.8.1 PWM Internal Structure and Timing 66
3.8.2 PWM Cycle and Duty Cycle 67
3.8.3 PWM idle mode wake-up description 68
3.8.4 PWM comparator gating description 68
3.8.5 IPWM waveform and Buzzer settings description 69
3.8.6 PWM2DT interrupt and (single) trigger ADC description 69
3.9 LED single-line cascading 71
3.10 ADC Analog-to-Digital Conversion 73
3.10.1 Explanation of ADC Power Supply Voltage Detection 74
3.10.2 Explanation of ADC Analog-to-Digital Conversion Settings 75
3.11 LED Dot Matrix Driver 76
3.11.1 LED Function Description 76
3.11.2 LED Dot Matrix Driver Setup Instructions 79
3.12 CMP Comparator 80
3.12.1 Voltage output Vinternal R of the voltage divider 81
3.12.2 Comparator configuration 82
3.12.3 VREF Usage 83
3.13 RFC Resistance Frequency Conversion 84
3.14 TC0 Port Level Capture 85

3.15 EEPROM and ISP Programming 87
3.15.1 EEPROM Read and Write Operations 87
3.15.2 ISP Programming 88
4 OPTION Configuration Table 90
5 Instruction Set 92
6 Electrical Characteristics 94
6.1 Limit Parameters 94
6.2 Electrical Characteristics 94
6.3 AD Conversion Characteristics 96
6.4 Characteristic Curves 97
6.4.1 Internal Low-Speed Oscillator - Frequency Characteristics Curve 97
6.4.2 Internal Low-Speed Oscillator - Temperature Characteristics Curve 97
6.4.3 Internal 16MHz RC Oscillator - Frequency Characteristics Curve 98
6.4.4 Internal 16MHz RC oscillator - Temperature frequency characteristic curve 98
6.5 IHRC frequency tuning parameter description 99
7 Package Size 103
7.1 16PIN package size 103
7.2 14PIN Package Dimensions 105
7.3 10PIN package size 106
7.4 8PIN package size 107

1 Chip Introduction

1.1 Functional Characteristics

CPU configuration

- 2K×16-Bit MTP ROM
- 176×8-Bit SRAM
- 256×16-Bit EEPROM
- 8-level stack space
- 8-level programmable voltage reset (LVR)
  1.8V, 2.0V, 2.2V, 2.5V
  2.9V, 3.3V, 3.6V, 3.8V
- Operating current less than 2 mA (8MHz/5V)
- Operating current less than 10 uA (40KHz/3V)
- Sleep current less than 1 uA (sleep mode)

I/O Configuration

- 2 groups of 14 bidirectional I/O ports: P5, P6
- Wake-up ports: P5, P6
- 14 programmable pull-up I/O pins
- 14 programmable pull-down I/O pins
- External interrupt:
  INT0:P60 INT1:P50

Working voltage

- Working voltage range:
  V_{LVR}2.2V～5.5V|Fcpu=0～8MHz
  V_{LVR}1.8V～5.5V|Fcpu=0～4MHz
  V_{LVR}1.8V～5.5V|Fcpu=0～2MHz

Operating frequency range

- Internal IHRC oscillation circuit:
  16MHz/8MHz/4MHz/1MHz
- Internal ILRC oscillation circuit:
  40KHz(5V)/41KHz(3V)
- Clock cycle frequency division selection:
  2Clock, 4Clock, 8Clock,
  16Clock, 32Clock

Peripheral Module

- 8-bit counter TC0 with capture function
- 6 channels, 2 groups of 12-bit PWM with dead-time complementary
- 14-channel 12-bit ADC analog-to-digital converter
- 1 comparator CMP
- PWM can trigger AD sampling
- LED dot matrix driver supports up to 6*7
- 2-channel RGB LED cascade controller (drives dreamcolor lights)

Interrupt source

- TC0 overflow interrupt
- External interrupt 1
- External interrupt 0
- P6 port input change interrupt
- P5 port input change interrupt
- ADC conversion complete interrupt
- PWM1 cycle match/TC1 timing interrupt
- PWM4 cycle match/TC2 timing interrupt
- PWM2 duty cycle match interrupt
- CMP status change interrupt
- E2P write complete interrupt

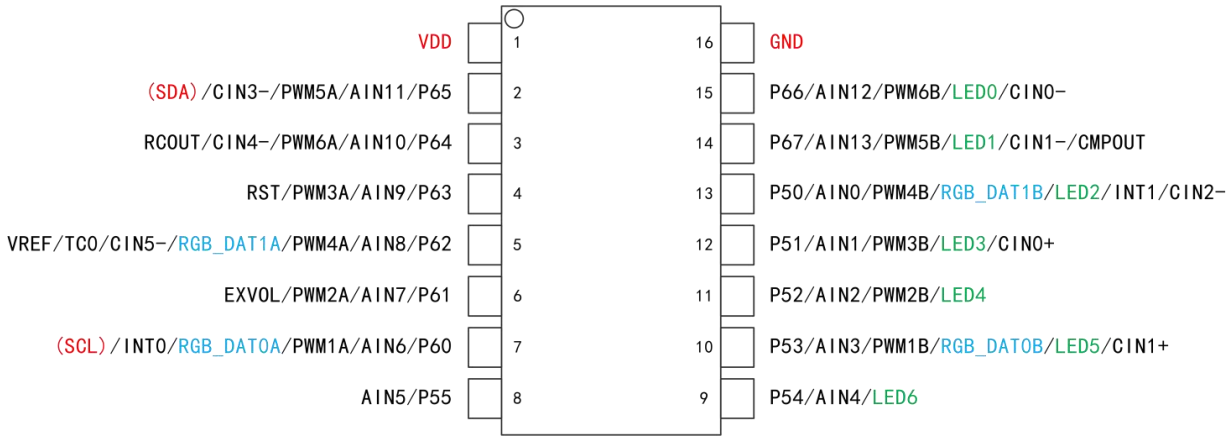
Characteristic

- Programmable WDT timer
- Four working modes switching
- Support Type-C port upgrade, support live burning

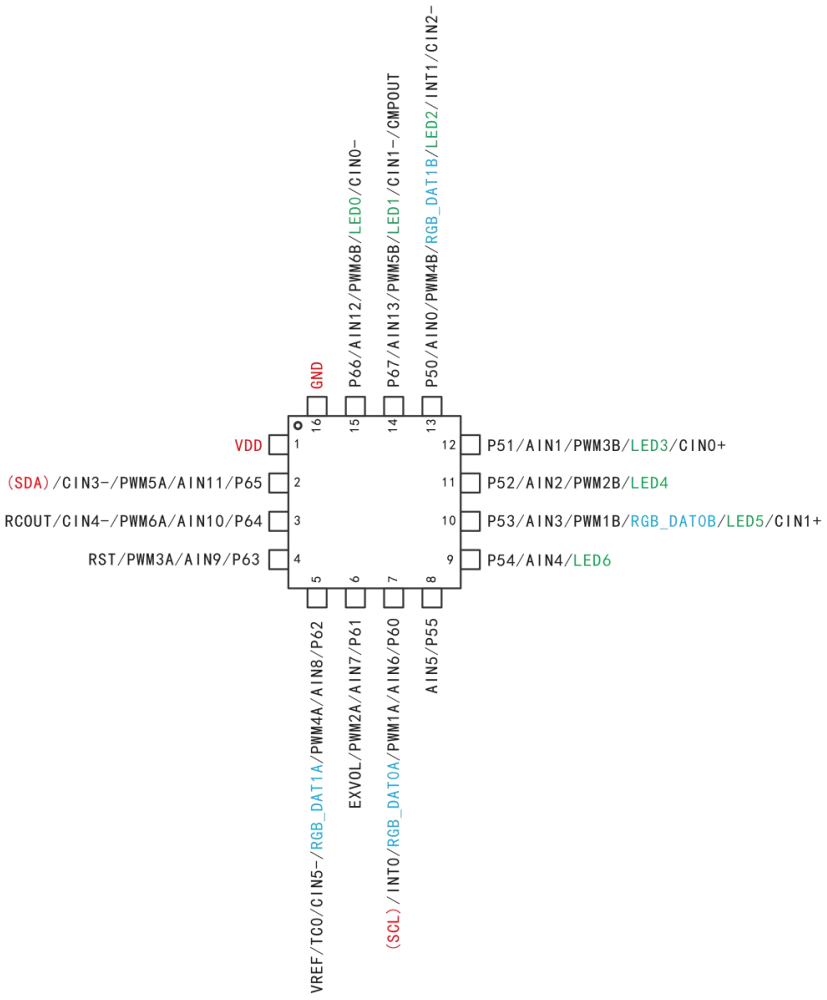
Package type

- JZ8M2632-SOP16/QFN16
- JZ8M2632-SOP14
- JZ8M2632-MSOP10
- JZ8M2632-SOP8
- JZ8M2632-SOP14A
- JZ8M2632-SOP16B
- JZ8M2632-SOP8B
- JZ8M2632-SOP14C
- JZ8M2632-SOP8C

1.2 Pin Assignment

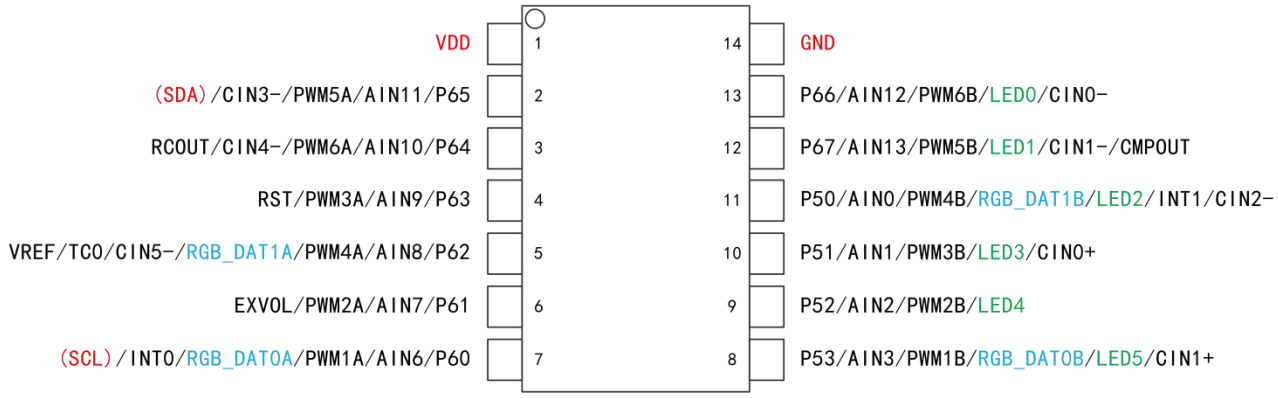


JZ8M2632-16 Pin Diagram

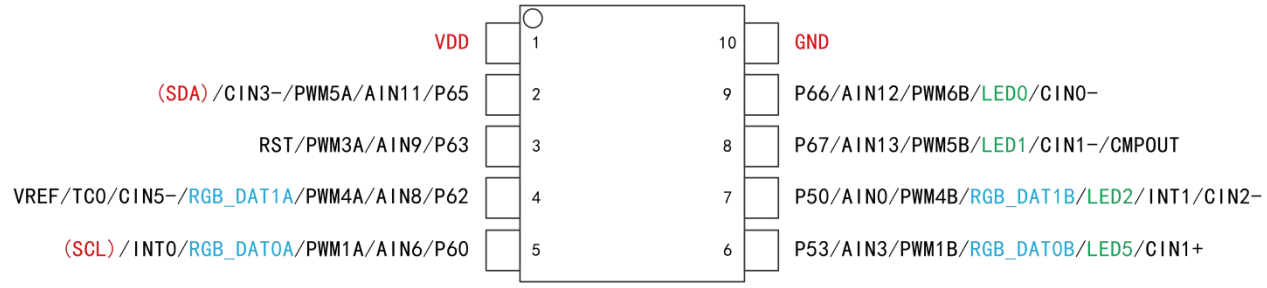


JZ8M2632-QFN16 Pin Diagram

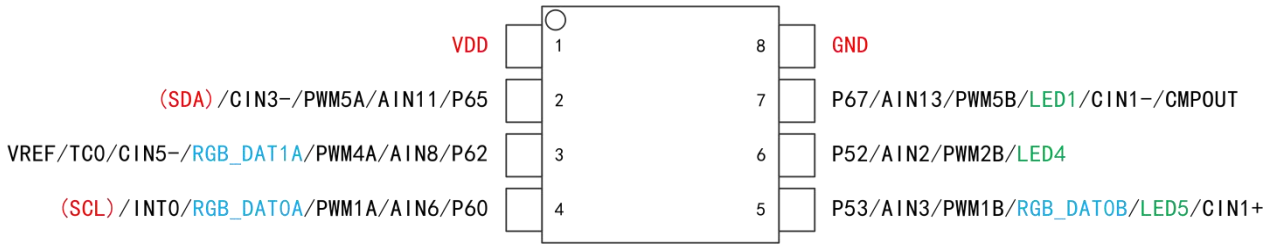
Note: The programming pins are P60 and P65.



JZ8M2632-14 Pin Diagram

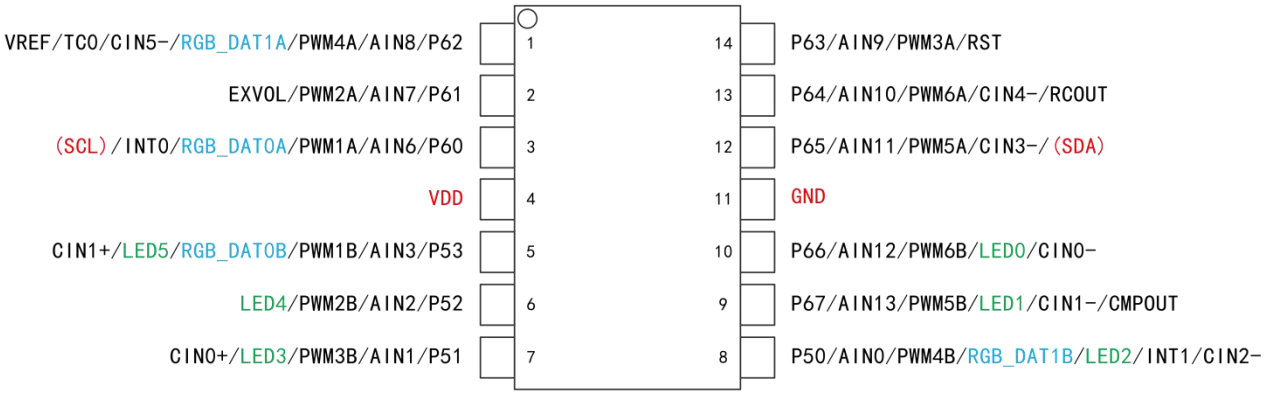


JZ8M2632-MSOP10 Pin Diagram

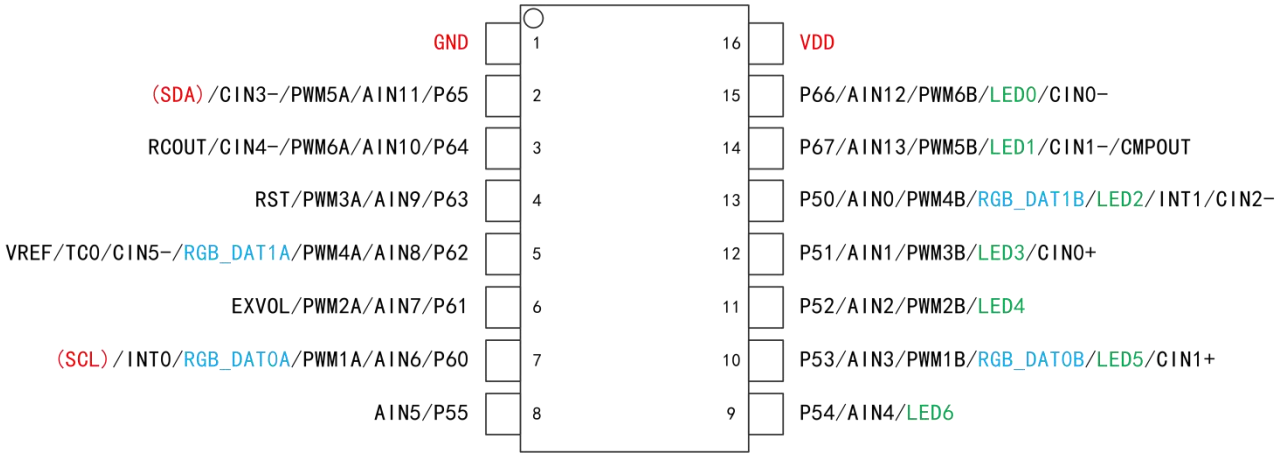


JZ8M2632-8 Pin Diagram

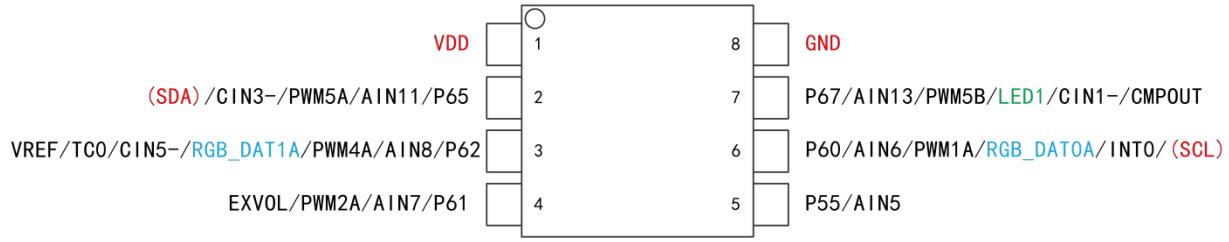
Note: The programming pins are P60 and P65.



JZ8M2632-14A Pin Diagram

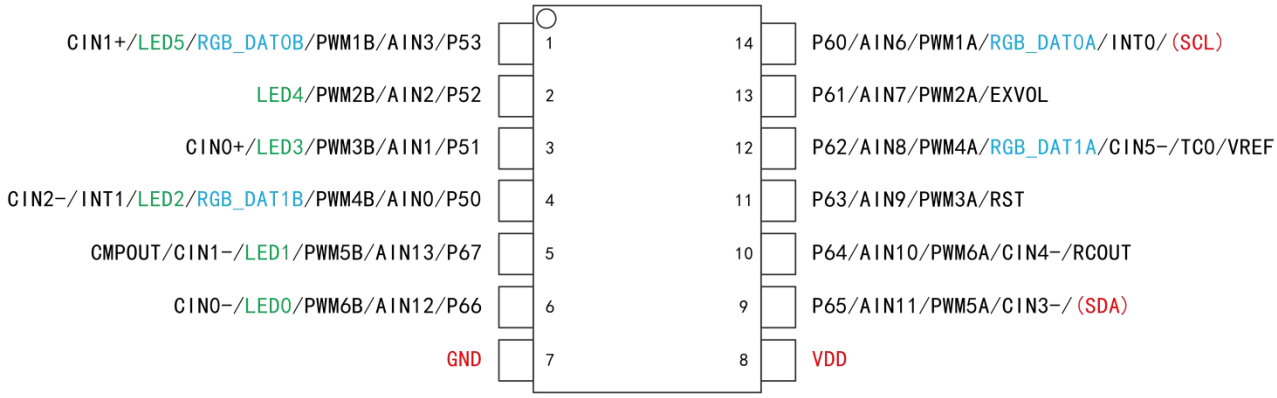


JZ8M2632-16B Pin Diagram

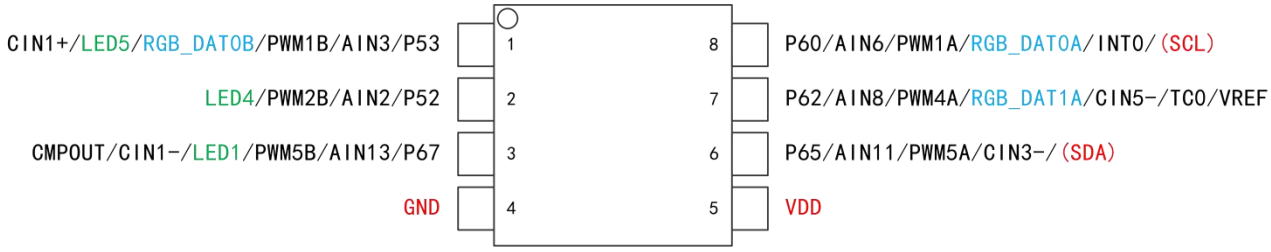


JZ8M2632-8B Pin Diagram

Note: The programming pins are P60 and P65.



JZ8M2632-14C Pinout Diagram



JZ8M2632-8C Pinout Diagram

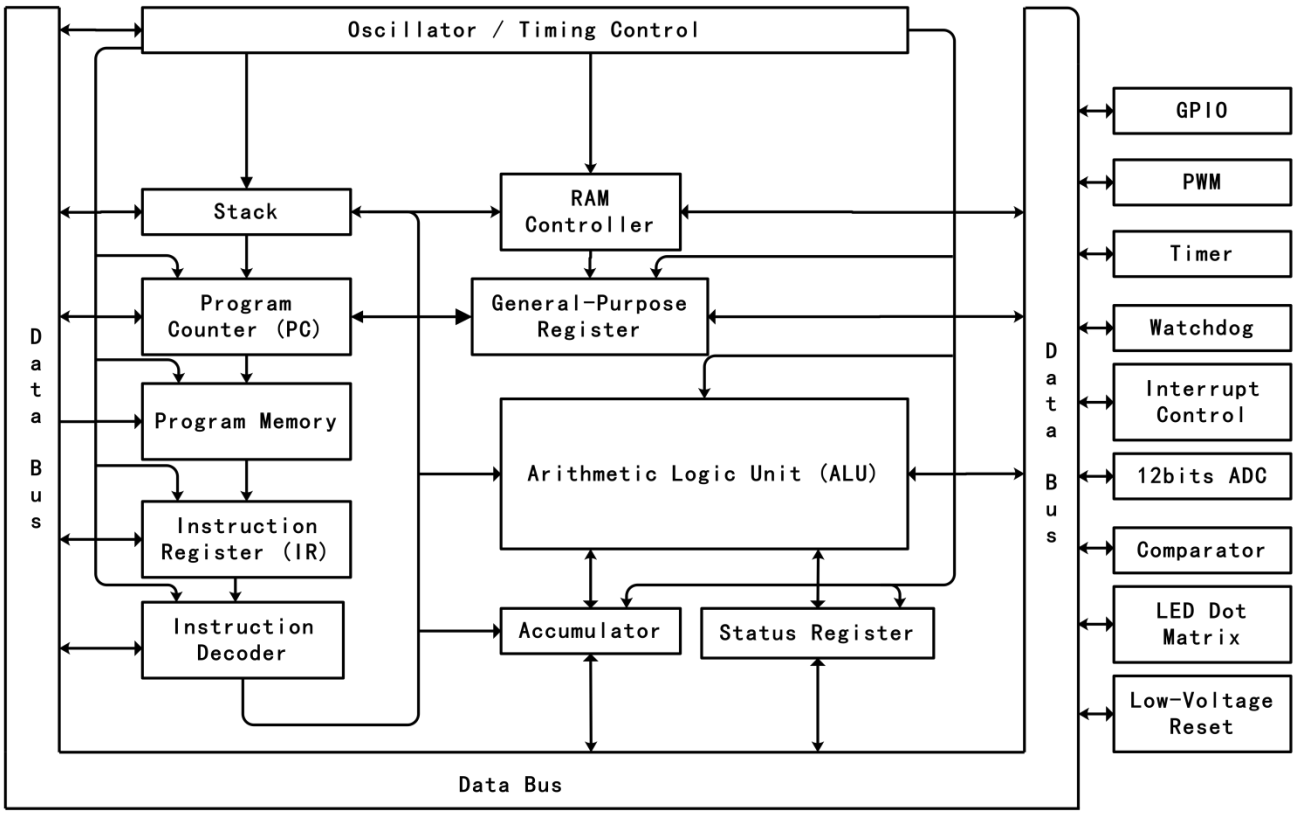
Note: The programming pins are P60 and P65.

1.3 Pin Description

Serial number	Pin Name	I/O	Function Description
P50	P50	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhanced secondary optional
	AIN0	AN	ADC Input Channel
	PWM4B	O	PWM4B Output
	RGB_DAT1B	O	Rainbow Drive Output Pin
	LED2	O	LED2 Output
	CIN2-	I	CMP Negative Input Source
	INT1	I	External Interrupt 1 Input Port
P51	P51	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhanced secondary optional
	AIN1	AN	ADC Input Channel
	PWM3B	O	PWM3B Output
	LED3	O	LED3 Output
	CIN0+	I	CMP Positive Input Source
P52	P52	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhanced secondary optional
	AIN2	AN	ADC Input Channel
	PWM2B	O	PWM2B output
	LED4	O	LED4 output
P53	P53	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhanced secondary optional
	AIN3	AN	ADC Input Channel
	PWM1B	O	PWM1B output
	RGB_DAT0B	O	Rainbow Drive Output Pin
	LED5	O	LED5 output
	CIN1+	I	CMP Positive Input Source
P54	P54	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhanced secondary optional
	AIN4	AN	ADC Input Channel
	LED6	O	LED6 output
P55	P55	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	AIN5	AN	ADC Input Channel
P60	P60	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	AIN6	AN	ADC Input Channel
	PWM1A	O	PWM1A output
	RGB_DAT0A	O	Rainbow Drive Output Pin
	INT0	I	External interrupt 0 input

	SCL	I	Programming clock port
P61	P61	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	AIN7	AN	ADC Input Channel
	PWM2A	O	PWM2A output
	EXVOL	I	CMP resistor voltage divider input port
P62	P62	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	AIN8	AN	ADC Input Channel
	PWM4A	O	PWM4A output
	RGB_DAT1A	O	Rainbow Drive Output Pin
	CIN5-	I	CMP Negative Input Source
	TCO	I	TCO external clock input port
	VREF	AN	ADC external reference voltage input port
P63	P63	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	AIN9	AN	ADC Input Channel
	PWM3A	O	PWM3A output
	RST	I	external reset input port
P64	P64	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	AIN10	AN	ADC Input Channel
	PWM6A	O	PWM6A output
	CIN4-	I	CMP Negative Input Source
	RCOUT	O	Internal instruction clock frequency output
P65	P65	I/O	GPIO, programmable pull-up/pull-down, port wake-up
	AIN11	AN	ADC Input Channel
	PWM5A	O	PWM5A output
	SDA	I	Programming Data Port
P66	P66	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhanced secondary optional
	AIN12	AN	ADC Input Channel
	PWM6B	O	PWM6B Output
	LED0	O	LED0 Output
	CIN0-	I	CMP Negative Input Source
P67	P67	I/O	GPIO, programmable pull-up/pull-down, port wake-up, drive enhanced secondary optional
	AIN13	AN	ADC Input Channel
	PWM5B	O	PWM5B output
	LED1	O	LED1 output
	CIN1-	I	CMP Negative Input Source
	CMPOUT	O	CMP result output
VDD	VDD	--	Power supply
GND	GND	--	Ground

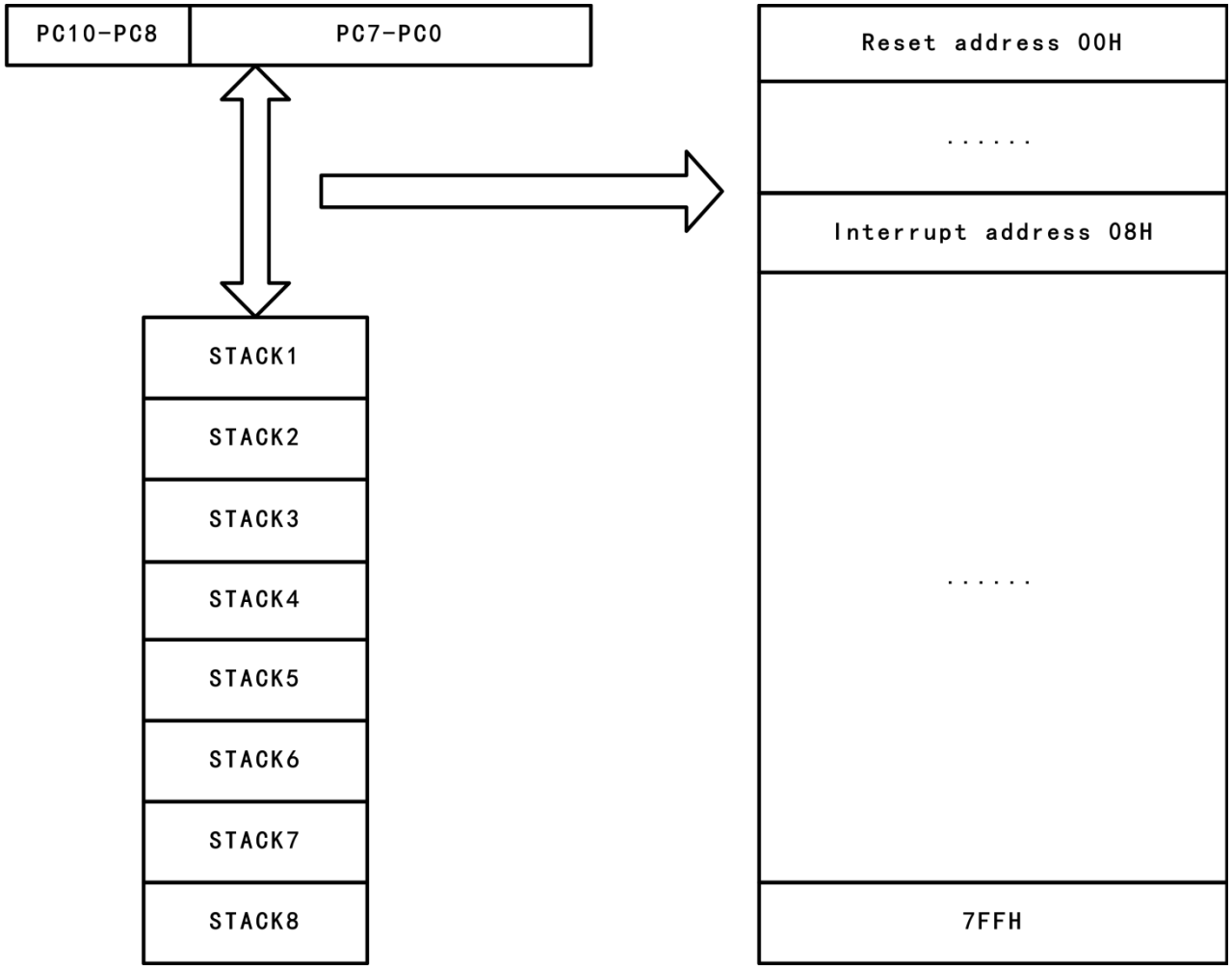
1.4 System Block Diagram



System Circuit Block Diagram

2 Memory Structure

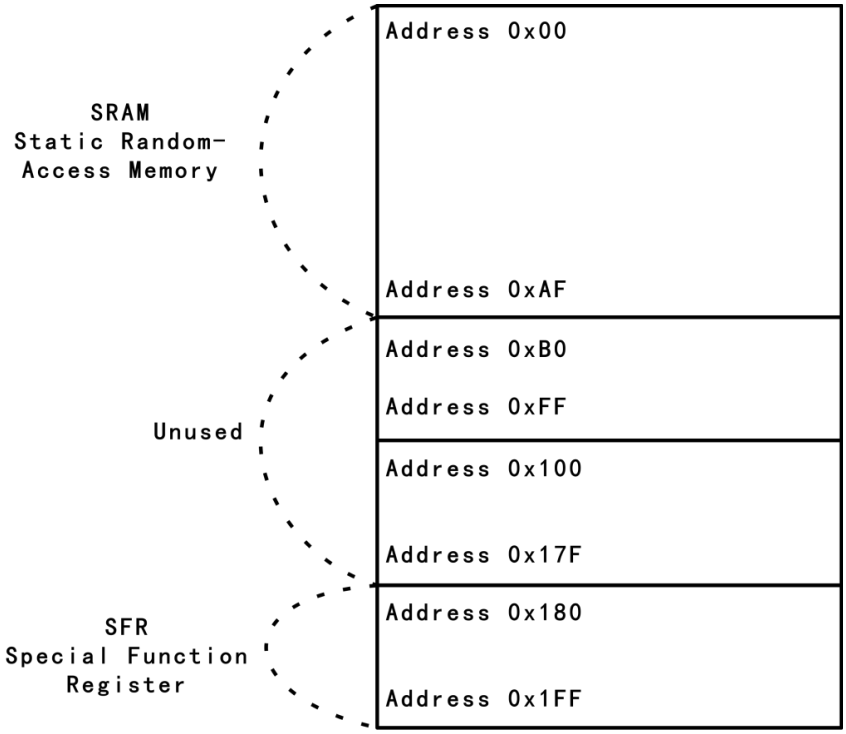
2.1 Program Storage Area Structure



Program Storage Area Structure Diagram

2.2 Data Storage Area

2.2.1 Data Storage Area Structure



Data Storage Area

2.2.2 Overview of Special Function Registers

Address	0X18_	0X19_	0X1A_	0X1B_	0X1C_	0X1D_	0X1E_	0X1F_
0	RSR	P5PH	P5AE	TC1CON	LEDRAM0			
1	PCH	P6PH	P6AE	TC1PRDL	LEDRAM1			
2	PCL			PWM1DTL	LEDRAM2			
3	STATUS	P5PD	ADATH	PWM2DTL	LEDRAM3			
4	TC0CON	P6PD	ADATL	PWM3DTL	LEDRAM4			
5	TC0C			TC1PRDTH	LEDRAM5			
6	TBRDH		ADCON0	PWM21DTH	LEDCON	INTE0		
7	TBRDL		ADCON1	PWMCON1	LEDDT	INTE1		
8	CPUCON			TC2CON	CMPCON0			
9	IHRCCAL			TC2PRDL	CMPCON1			
A(10)	P5			PWM4DTL	E2PCON	INTF0		
B(11)	P6			PWM5DTL	E2PDATL	INTF1		
C(12)		P5IWE		PWM6DTL	E2PDATH			
D (13)	P5CON	P6IWE	TPRE	TC2PRDTH				
E (14)	P6CON		EXINTCON	PWM54DTH				
F(15)			WDTCON	PWMCON2				IAR

3 Function Description

3.1 Operation Register

3.1.1 R180/RSR (RAM Select Register)

0X180	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSR	RSR<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

RSR<7:0> is used to select the SRAM register address in indirect addressing mode (addressing range: 0x00～0xAF).

The RSR register is used in conjunction with the R1FF register to perform indirect addressing operations. Users can place the address corresponding to a certain register into the RSR register, and then access the indirect addressing register R1FF, at which point the address will point to the SRAM corresponding to the address in RSR.

3.1.2 R181/PCH (Program Counter High Register)

0X181	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCH	-	-	-	-	-	PC<10:8>		
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

3.1.3 R182/PCL (Program Counter Low Register)

0X182	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCL	PC<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

The Program Counter (PC) is a pointer used to record the instruction that the CPU needs to process during each instruction cycle. During the CPU's operation cycle, the PC advances the instruction pointer to the program memory, and then the pointer increments by 1 to enter the next cycle. The JZ8M2632 has an 11-bit wide Program Counter (PC), with the low byte coming from the writable PCL register and the high byte coming from the readable PCH register.

The stack is used to record the instruction pointer for program returns. When a subroutine is called, the PC pushes the instruction pointer onto the stack. When the return instruction is to be executed, the stack sends the instruction pointer back to the PC to continue the original process. The JZ8M2632 has an 8-level stack that occupies neither program storage space nor data storage space, and the stack pointer cannot be read or written.

Details of the Program Counter (PC) and stack are as follows:

(1) The registers PC and the built-in 8-level stack are both 11 bits wide, used for addressing 2K×16Bit MTP ROM.

(2) Generally, the PC increments by one; during reset, all bits of the PC are cleared to zero.

(3) The instruction "JMP" allows for the direct loading of an 11-bit address, then pushes PC+1 onto the stack. Therefore, the JMP instruction allows the PC to jump to any location in the program.

(4) The instruction "CALL" allows for loading an 11-bit address into the PC, then pushes PC+1 onto the stack. Therefore, the entry address of the subroutine can be located at any position in the program.

(5) Executing the "RET" instruction sends the top data from the stack to the PC.

(6) Executing the "ADD PCL,A" instruction adds a relative address to the current PC, incrementing the ninth bit and above of the PC sequentially.

(7) Executing the "MOV PCL,A" instruction loads an address from the "A" register into the low 8 bits of the PC, while the ninth bit and above of the PC remain unchanged.

(8) Any instruction that writes a value to PCL (except for the "ADD PCL,A" instruction) (e.g., "MOV PCL,A", "BTC PCL,1") will keep the ninth and tenth bits of the PC unchanged.

(9) Any instruction other than "TBRD R" is a single instruction cycle.

(10) The stack operates like a circular buffer, meaning that after pushing 8 times, the data pushed on the 9th time will overwrite the data from the 1st push, and the data pushed on the 10th time will overwrite the data from the 2nd push, and so on.

3.1.4 R183/STATUS (Status Flag Register)

0X183	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	RST	GIE	-	T	P	Z	DC	C
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	1	1	X	X	X

Bit<7>: RST - Reset or Wake-up Flag

0: Other Reset Types

1: Wake-up triggered by pin state change

Bit<6>: GIE - Interrupt Enable Flag

0: Masked by DIT instruction or hardware interrupt

1: Interrupt enabled by EIT/RTI instruction

Bit<5>: Unused

Bit<4>: T - Time Overflow Bit

0: WDT watchdog overflow

1: Execute the "SLEEP" and "CWDT" instructions or low voltage reset

Bit<3>: P-Power Down Flag

0: Execute the "SLEEP" instruction

1: Power-on reset or execute the "CWDT" instruction

The events affecting T/P are shown in the table below:

Type	RST	T	P
Power-on reset	0	1	1
Press RESET in working mode	0	Hold	Hold
RESET wake-up	0	1	0
WDT watchdog overflow in	0	0	Hold
WDT watchdog overflow wake-up	0	0	0
Port input change wake-up	1	1	0
Execute CWDT instruction	Hold	1	1
Execute SLEEP instruction	Hold	1	0

Bit<2>: Z - Set to "1" when the result of arithmetic or logical operation is zero

0: When the result of arithmetic or logical operation is not zero

1: When the result of arithmetic or logical operation is zero

Bit<1>: DC - Auxiliary carry flag

0: No carry generated in the low four bits during addition; / Borrow generated in the low four bits during subtraction

1: When performing addition, there is a carry in the lower four bits; / When performing subtraction, there is no borrow in the lower four bits.

Bit<0>: C-carry flag

0: No carry generated in the high four bits during addition; / Borrow generated in the high four bits during subtraction

1: Carry generated in the high four bits during addition; / No borrow generated in the high four bits during subtraction

3.1.5 R184/TC0CON (TC0 Control Register)

0X184	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0CON	TC0EN	TC0CKS<1:0>		TC0EDG	TC0PTEN	TC0PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC0EN - TC0 Timer Count Enable Bit

0: Disable TC0

1: Enable TC0

Bit < 6:5 >: TC0CKS<1:0> - TC0 Signal Source Selection Bit

00: Instruction Clock

01: External Input Signal (P62)

10: System Clock

11: ILRC Clock (Low-Speed Oscillator)

Bit<4>: TC0EDG - TC0 Signal Edge Selection Bit

0: TC0 Pin Signal Changes from High to Low, Increment by 1

1: The TC0 pin signal changes from low to high, incrementing by 1

Bit<3>: TC0PTEN - Pre-divider Enable Bit

0: Disable TC0 Pre-divider

1: Enable TC0 Pre-divider

Bit<2:0>: TC0PSR<2:0> - TC0 Pre-divider Selection Control Bits:

TC0PSR<2>	TC0PSR<1>	TC0PSR<0>	TC0 Division Factor
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64

1	1	0	1:128
1	1	1	1:256

3.1.6 R185/TC0C (TC0 8-bit Counter Register)

0X185	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC0C	TC0C<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.7 R186/TBRDH (Table Pointer High Register)

0X186	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDH	-	-	-	-	-	RBIT<10:8>		
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<2:0>: RBIT<10:8>-TBRD pointer address high 3 bits.

3.1.8 R187/TBRDL (Table pointer low register)

0X187	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBRDL	RBIT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: RBIT<7:0>-TBRD pointer address low 8 bits.

Note: RBIT<7:0> is used to select the low 8 bits of the table ROM address in table lookup mode.

3.1.9 R188/CPUCON (CPU mode control register)

0X188	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CPUCON	PWM4_LEDEN	PWM1_LEDEN	TC2WE	TC1WE	TC0WE	STPHX	CLKMD	IDLE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM4_LEDEN-PWM4 LED cascade control 位

0: Disable

1: Enable

Bit<6>: PWM1_LEDEN - PWM1 LED cascading control bit

0: Disable

1: Enable

Bit<5>: TC2WE - TC2 Wake-up Enable Bit

0: Wake-up Disabled

1: Wake-up Enabled, can wake up from Idle Mode

Bit<4>: TC1WE - TC1 Wake-up Enable Bit

0: Wake-up Disabled

1: Wake-up Enabled, can wake up from Idle Mode

Bit<3>: TC0WE - TC0 Wake-up Enable Bit

0: Wake-up Disabled

1: Wake-up Enabled, can wake up from Idle Mode

Bit<2>: STPHX - High-Speed Clock Control Bit

0: High-Speed Clock Operating Normally

1: Stop High-Speed Clock

Bit<1>: CLKMD - System Clock Control Bit

0: System Clock Uses High-Speed Oscillator (IHRC) Clock

1: The system clock uses a low-speed oscillator (ILRC) clock.

When the system transitions from high-speed mode to low-speed mode, set CLKMD=1 first, then set STPHX=1.

When the system transitions from low-speed mode to high-speed mode, set STPHX=0 first, then set CLKMD=0.

Bit<0>: IDLE - Idle mode enable bit.

0: The system enters sleep mode when executing the SLEEP instruction.

1: The system enters idle mode when executing the SLEEP instruction, and the system clock operates normally.

TC0 and PWM can continue to operate in idle mode if the system clock is selected, and can wake up the system.

3.1.10 R189/IHRCCAL (IHRC frequency calibration register)

0X189	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IHRCCAL	-	IHRCCAL<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	X	X	X	X	X	X	X

IHRC High-Speed Oscillator Frequency Fine-Tuning

3.1.11 R18A/P5 (P5 Data Register)

0X18A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5	-	-	P5<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 Port Data Control

3.1.12 R18B/P6 (P6 Data Register)

0X18B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6	P6<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 Port Data Control

3.1.13 R18D/P5CON (P5 Control Register)

0X18D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5CON	-	-	P5CON<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port input/output control bits:

0: Output

1: Input

3.1.14 R18E/P6CON (P6 control register)

0X18E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6CON	P6CON<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port input/output control bits:

0: Output

1: Input

3.1.15 R190/P5PH (P5 pull-up control register)

0X190	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PH	-	-	P5PH<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port pull-up control bit:

0: Enable

1: Disable

3.1.16 R191/P6PH (P6 pull-up control register)

0X191	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PH	P6PH<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port pull-up control bit:

0: Enable

1: Disable

3.1.17 R193/P5PD (P5 pull-down control register)

0X193	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5PD	-	-	P5PD<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P5 port pull-down control bits:

0: Enable

1: Disable

3.1.18 R194/P6PD (P6 pull-down control register)

0X194	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6PD	P6PD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

P6 port pull-down control bits:

0: Enable

1: Disable

3.1.19 R19C/P5IWE (P5 input change interrupt, wake-up enable register)

0X19C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5IWE	-	-	P5IWE<5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 port input change wake-up control bits:

0: Disable

1: Enable

3.1.20 R19D/P6IWE (P6 Input Change Interrupt, Wake-up Enable Register)

0X19D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6IWE	P6IWE <7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P6 port input change wake-up control bit:

0: Disable

1: Enable

3.1.21 R1A0/P5AE (P5 analog port enable register)

0X1A0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5AE	-	-	P5AE <5:0>					
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

P5 port analog channel selection control bit:

0: Port set as GPIO

1: Port set as analog input

3.1.22 R1A1/P6AE (P6 analog port enable register)

0X1A1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6AE	P6AE <7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R /W
Reset Value	0	0	0	0	0	0	0	0

P6 port analog channel selection control bit:

0: Port set as GPIO

1: Port set as analog input

3.1.23 R1A3/ADATH (ADC data high 8-bit register)

0X1A3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATH	ADAT<11:4>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	X	X	X	X	X	X	X	X

Bit<7:0>: ADAT<11:4> - AD conversion result high 8 bits

3.1.24 R1A4/ADATL (ADC data low 8-bit register)

0X1A4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADATL	ADAT<7:0>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	X	X	X	X	X	X	X	X

Bit<7:0>: ADAT<7:0> - Low 8 bits of AD conversion result

3.1.25 R1A6/ADCON0 (ADC Control Register 0)

0X1A6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON0	ADIS<3:0>				ADAT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Reset Value	0	0	0	0	X	X	X	X

Bit<7:4>: ADIS<3:0> - AD input channel selection

ADIS<3>	ADIS<2>	ADIS<1>	ADIS	Channel Selection
0	0	0	0	AIN0/P50
0	0	0	1	AIN1/P51
0	0	1	0	AIN2/P52
0	0	1	1	AIN3/P53
0	1	0	0	AIN4/P54
0	1	0	1	AIN5/P55
0	1	1	0	AIN6/P60
0	1	1	1	AIN7/P61
1	0	0	0	AIN8/P62
1	0	0	1	AIN9/P63

1	0	1	0	AIN10/P64
1	0	1	1	AIN11/P65
1	1	0	0	AIN12/P66
1	1	0	1	AIN13/P67
1	1	1	0	0.254VDD
1	1	1	1	GND

Bit<3:0>: ADAT<11:8> - High 4 bits of AD conversion result

3.1.26 R1A7/ADCON1 (ADC Control Register 1)

0X1A7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON1	ADRUN	ADEN	ADPSR<1:0>		ADCGATE	VREF<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: ADRUN

0: ADC no sampling or sampling ended

1: ADC starts sampling

Bit<6>: ADEN

0: ADC disabled (turn off ADC in sleep mode, otherwise there will be power consumption)

1: ADC enabled

Bit<5:4>: ADPSR<1:0> - ADC clock division selection (Fosc is the system clock frequency)

ADPSR<1>	ADPSR<0>	ADC Clock
0	0	Fosc/16
0	1	Fosc/4
1	0	Fosc/64
1	1	Fosc/1

Bit<3>: ADCGATE - ADC Gate Control Selection Bit

0: Gate disabled, enabled by software ADCEN

1: Gate enabled, ADC sampling enabled triggered by the falling edge of PWM2 duty cycle

Note: The clock level that triggers ADRUN is maintained for half a PWM2 clock cycle. In applications, avoid triggering level times greater than the ADC conversion cycle.

Bit<2:0>: VREF<2:0> - Reference voltage selection

VREF<2>	VREF<1>	VREF<0>	Reference
0	0	0	VDD

0	0	1	Reference 2V
0	1	0	Reference 3V
0	1	1	Reference 4V
1	1	1	VREFS (P62)

3.1.27 R1AD/TPRE(TC0 Pre-divider)

0X1AD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TPRE	TPRE<7:0>							
Read/Write	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

3.1.28 R1AE/EXINTCON (External Interrupt Control Register)

0X1AE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXINTCON	INT1S<1:0>		INT0S<1:0>		PWM2_PULSE_EN	CAPS	TC0GATE<1:0>	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:6>: INT1S<1:0> - INT1 Mode Selection Bit

INT1S<1>	INT1S<0>	INT1 Mode Selection
0	0	Function Disabled
0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

Bit<5:4>: INT0S<1:0> - INT0 Mode Selection Bit

INT0S<1>	INT0S<0>	INT0 Mode Selection
0	0	Function Disabled
0	1	Rising Edge Trigger
1	0	Falling Edge Trigger
1	1	Level Change Trigger

Bit<3>: PWM2_PULSE_EN - PWM2 single pulse mode enable bit

0: Disable

1: Enable (outputs a single duty cycle pulse in single pulse mode; after the pulse ends, PWM2EN hardware is set to 0)

Bit<2>: CAPS - TC0 level capture port selection

0: Use INT0 capture

1: Use INT1 capture

Bit<1:0>: TC0GATE<1:0> - TC0 capture gate enable bit

TCOGATE <1>	TCOGATE <0>	TC0 capture gate enable selection
0	0	Disabled
0	1	Enable gate control, INT0/1 as capture source
1	0	Enable gate control, CMPOUT as capture source
1	1	Disable configuration usage

3.1.29 R1AF/WDTCON (WDT, external interrupt control register)

0X1AF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCON	WDTE	WDTPSR<1:0>		LVREN	ADCWE	CMPWE	INT1WE	INT0WE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	0	0	0	0	0	0	0

Bit<7>: WDTE-WDT watchdog enable control

0: Disable

1: Enable

Bit<6:5>: WDTPSR<1:0>-WDT prescaler selection bits:

WDTPSR<1>	WDTPSR<0>	WDT prescaler factor
0	0	1:4
0	1	1:8
1	0	1:16
1	1	1:32

Bit<4>: LVREN - LVR enable control

0: Enable

1: Disable

Bit<3>: ADCWE - ADC wake-up enable bit

0: Disable

1: Enable

Bit<2>: CMPWE - CMP wake-up enable bit

0: Disable

1: Enable

Bit<1>: INT1WE - INT1 wake-up enable bit

0: Disable

1: Enable

Bit<0>: INT0WE - INT0 Wake-up Enable Bit

0: Disable

1: Enable

3.1.30 R1B0/TC1CON (TC1 Control Register)

0X1B0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1CON	TC1EN	TC21EN	PWM1GATE	TC1CKS	TC1PTEN	TC1PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC1EN - TC1/PWM123 Counter Enable Control

0: Disable

1: Enable (If the TC1PRD register is set, TC1 resets when it counts to the preset value, and TC1 starts counting from 1)

Bit<6>: TC21EN-TC1/PWM123, TC2/PWM456 counter simultaneous enable control bit

0: Disable

1: Enable

Bit<5>: PWM1GATE-PWM1 gate output enable control bit

0: No restriction

1: PWM1 output is controlled by the comparator result; when CMPOUT=0, PWM waveform is output, and when CMPOUT=1, PWM1 remains low.

Bit<4>: TC1CKS-TC1 clock selection

0: Instruction clock

1: System clock

Bit<3:0>: TC1PTEN, TC1PSR2~TC1PSR0 prescaler selection bits:

TC1PTEN	TC1PSR<2>	TC1PSR<1>	TC1PSR	TC1
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.31 R1B1/TC1PRDL (TC1/PWM123 Period Low 8-bit Register)

0X1B1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDL	TC1PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Value	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM2, PWM3) Period Low 8-bit

3.1.32 R1B2/PWM1DTL (PWM1 Duty Cycle Low 8-bit Register)

0X1B2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DTL	PWM1DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM1 duty cycle low 8 bits

3.1.33 R1B3/PWM2DTL (PWM2 Duty Cycle Low 8-bit Register)

0X1B3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2DTL	PWM2DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM2 Duty Cycle Low 8-bit

3.1.34 R1B4/PWM3DTL (PWM3 Duty Cycle Low 8-bit Register)

0X1B4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM3DTL	PWM3DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM3 Duty Cycle Low 8-bit

3.1.35 R1B5/TC1PRDTH (TC1/PWM123 Period High 4-bit and PWM3 Duty Cycle High 4-bit Register)

0X1B5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC1PRDTH	TC1PRD<11:8>				PWM3DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC1 (PWM1, PWM2, PWM3) period high 4 bits and PWM3 duty cycle high 4 bits

3.1.36 R1B6/PWM21DTH (PWM21 duty cycle high 4 bits register)

0X1B6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM21DTH	PWM2DT<11:8>				PWM1DT<11:8>			

Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM2 duty cycle high 4 bits, PWM1 duty cycle high 4 bits

3.1.37 R1B7/PWMCON1 (PWM control register 1)

0X1B7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON1	BZ1EN	PWM3S	PWM2S	PWM1S	IPWM1EN	PWM3EN	PWM2EN	PWM1EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ1EN - BZ1 waveform output enable control bit

0: Disable

1: Output BZ1 waveform (BZ1EN=1 and PWM1EN=0 must be set)

(P60/P53 must be set as output to output the BZ1 waveform)

Bit<6>: PWM3S-PWM3 output selection control bit

0: PWM3 outputs from P63

1: PWM3 outputs from P51

Bit<5>: PWM2S-PWM2 output selection control bit

0: PWM2 outputs from P61

1: PWM2 outputs from P52

Bit<4>: PWM1S-PWM output selection control bit

0: PWM1 outputs from P60

1: PWM1 outputs from P53

Bit<3>: IPWM1EN-IPWM1 enable control bit

0: Disable

1: Output PWM2 XOR PWM3

(Select output port based on PWM2EN (P61/P52) or PWM3EN (P63/P51))

Bit<2>: PWM3EN - PWM3 enable control bit

0: Disable

1: Enable output of PWM3 waveform

(The corresponding port must be set to output to output the PWM3 waveform)

Bit<1>: PWM2EN - PWM2 enable control bit

0: Disable

1: Enable output of PWM2 waveform

(The corresponding port must be set to output to output the PWM2 waveform)

Bit<0>: PWM1EN - PWM1 enable control bit

0: Disable

1: Enable output of PWM1 waveform

(The corresponding port must be set to output to output the PWM1 waveform, and BZ1EN=0)

3.1.38 R1B8/TC2CON(TC2 Control Register)

0X1B8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2CON	TC2EN	PWM4GATE<1:0>		TC2CKS	TC2PTEN	TC2PSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: TC2EN - TC2/PWM456 Counter Enable Control

0: Disable

1: Enable

Bit<6:5>: PWM4GATE<1:0> - PWM4 Gate Output Enable Control Bit

PWM4GATE <1>	PWM4GATE<0>	PWM4 gate output enable control selection
0	0	Unlimited
0	1	PWM4 output is controlled by the comparator result. When CMPOUT=0, it outputs a PWM waveform; when CMPOUT=1, PWM4 remains at a low level.
1	0	PWM4 output is controlled by the external interrupt INT (P60). When INT=1, it outputs a PWM waveform.
1	1	Disable configuration usage

Bit<4>: TC2CKS - TC2 clock selection

0: Instruction clock

1: System clock

Bit<3:0>: TC2PTEN, TC2PSR2～TC2PSR0 prescaler selection bits:

TC2PTEN	TC2PSR<2>	TC2PSR<1>	TC2PSR<0>	TC2 prescaler value
0	0	0	0	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32

1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

3.1.39 R1B9/TC2PRDL(TC2/PWM456 Low 8-bit Period Register)

0X1B9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDL	TC2PRD<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 (PWM4, PWM5, PWM6) Low 8-bit Period

3.1.40 R1BA/PWM4DTL(PWM4 Duty Cycle Low 8-bit Register)

0X1BA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM4DTL	PWM4DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM4 Low 8-bit Duty Cycle

3.1.41 R1BB/PWM5DTL(PWM5 Duty Cycle Low 8-bit Register)

0X1BB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM5DTL	PWM5DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM5 low 8 bits of duty cycle

3.1.42 R1BC/PWM6DTL (PWM6 low 8 bits duty cycle register)

0X1BC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM6DTL	PWM6DT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM6 low 8 bits of duty cycle

3.1.43 R1BD/TC2PRDTH (TC2/PWM456 high 4 bits of period and PWM6 high 4 bits of duty cycle register)

0X1BD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TC2PRDTH	TC2PRD <11:8>				PWM6DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

TC2 (PWM4, PWM5, PWM6) high 4 bits of period and PWM6 high 4 bits of duty cycle

3.1.44 R1BE/PWM54DTH (PWM54 Duty Cycle High 4-bit Register)

0X1BE	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM54DTH	PWM5DT<11:8>				PWM4DT<11:8>			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

PWM5 Duty Cycle High 4-bit, PWM4 Duty Cycle High 4-bit

3.1.45 R1BF/PWMCON2 (PWM Control Register 2)

0X1BF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMCON2	BZ2EN	PWM6S	PWM5S	PWM4S	IPWM4EN	PWM6EN	PWM5EN	PWM4EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: BZ2EN - BZ2 waveform output enable control bit

0: Disable

1: Output BZ2 waveform (BZ2EN=1, PWM4EN=0 must be set, BZ2 waveform outputs from PWM4 port)

Bit<6>: PWM6S - PWM6 output selection control bit

0: PWM6 outputs from P64

1: PWM6 outputs from P66

Bit<5>: PWM5S - PWM5 output selection control bit

0: PWM5 outputs from P65

1: PWM5 outputs from P67

Bit<4>: PWM4S-PWM4 output selection control bit

0: PWM4 outputs from P62

1: PWM4 outputs from P50

Bit<3>: IPWM4EN-IPWM4 enable control bit

0: Disable

1: Output PWM5 XOR PWM6 (select output port based on PWM5EN or PWM6EN)

Bit<2>: PWM6EN-PWM6 enable control bit

0: Disable

1: Enable output of PWM6 waveform

(The corresponding port must be set to output to output the PWM6 waveform)

Bit<1>: PWM5EN - PWM5 enable control bit

0: Disable

1: Output PWM5 waveform enable

(The corresponding port must be set to output to output the PWM5 waveform)

Bit<0>: PWM4EN - PWM4 enable control bit

0: Disable

1: Output PWM4 waveform enable

(The corresponding port must be set to output to output the PWM4 waveform, and BZ2EN=0)

3.1.46 R1C0/LEDRAM0 (LEDRAM register 0)

0X1C0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM0	-	LEDRAM0<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM0<6:0> - LEDRAM data read/write bit

3.1.47 R1C1/LEDRAM1 (LEDRAM register 1)

0X1C1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM1	-	LEDRAM1<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM1<6:0>-LEDRAM data read/writebit

3.1.48 R1C2/LEDRAM2 (LEDRAM Register 2)

0X1C2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM2	-	LEDRAM2<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM2<6:0>-LEDRAM data read/writebit

3.1.49 R1C3/LEDRAM3 (LEDRAM Register 3)

0X1C3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM3	-	LEDRAM3<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0>: LEDRAM3<6:0>-LED RAM data read/writebit

3.1.50 R1C4/LEDRAM4 (LEDRAM Register 4)

0X1C4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM4	-	LEDRAM4<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0> : LEDRAM4<6:0> - LEDRAM Data Read/Write Bit

3.1.51 R1C5/LEDRAM5 (LEDRAM Register 5)

0X1C5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM5	-	LEDRAM5<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:0> : LEDRAM5<6:0> - LEDRAM Data Read/Write Bit

3.1.52 R1C6/LEDCON (LED Control Register)

0X1C6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDCON	LEDEN	LEDDUTY<1:0>		LEDHOLD	LEDCKS	LEDPSR<2:0>		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: LEDEN- LED enable bit

0: Disable

1: Enable

Bit<6:5>: LEDDUTY<1:0>- LED matrix mode selection bit

LEDDUTY<1>	LEDDUTY<0>	LED matrix mode
0	0	4*4
0	1	5*5
1	0	6*6

1	1	6*7

Bit<4>: LEDHOLD - LED hold state

0: LED normal operation

1: LED hold state

Bit<3>: LEDCKS - LED clock source selection bit

0: system clock

1: instruction clock

Bit<2:0>: LEDPSR<2:0> - LED clock division selection bit

LEDPSR<2>	LEDPSR<1>	LEDPSR<0>	Division Ratio
0	0	0	8 clock
0	0	1	16 clock
0	1	0	32 clock
0	1	1	64 clock
1	0	0	128 clock
1	0	1	256 clock

3.1.53 R1C7/LEDDT (LED Duty Cycle Register)

0X1C7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDDT	-	LEDDT<6:0>						
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: Unused

Bit<6:0>: LEDDT<6:0> - LED Brightness Selection Bits

00H (Level 0: Darkest) ~ 7FH (Level 127: Brightest)

3.1.54 R1C8/CMPCON0 (CMP Control Register 0)

0X1C8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON0	CMPEN	CMPOUT	CMPRS<5:0>					
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPEN - CMP Enable Control Bit

0: Disable

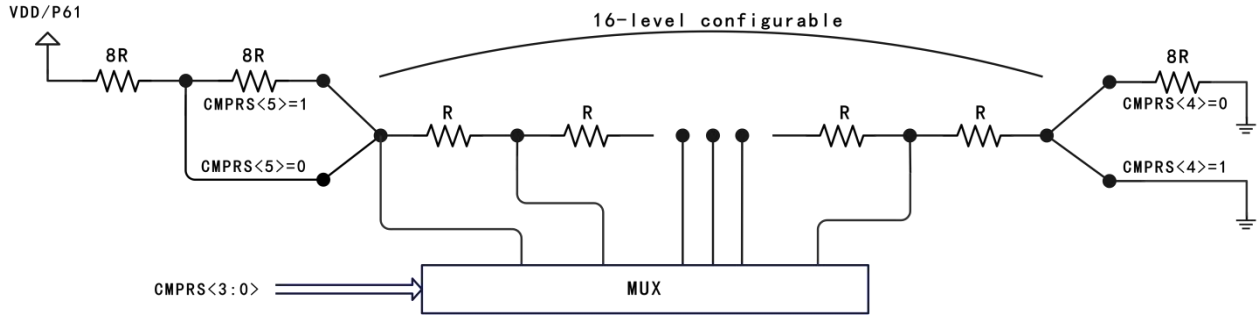
1: Enable

Bit<6>: CMPOUT-CMP result output bit

0: The positive voltage of the comparator is less than the negative voltage

1: The positive voltage of the comparator is greater than the negative voltage

Bit<5:0>: CMPRS<5:0> - Comparator adjustment bits



For example, when CMPCON1=0x07, the ADCCON1 register VREF<2:0> selects 2V, the positive terminal of the comparator selects VDD resistor divider, and the negative terminal of the comparator selects 1/2*2V. Different resistor divider settings CMPRS<5:0> correspond to different detection voltages, as shown in the table below:

CMPRS	Detection Voltage	CMPRS	Detection Voltage	CMPRS	Detection Voltage	CMPRS	Detection Voltage
00H	3.556	10H	24.000	20H	4.444	30H	32.000
01H	3.200	11H	12.000	21H	4.000	31H	16.000
02H	2.909	12H	8.000	22H	3.636	32H	10.667
03H	2.667	13H	6.000	23H	3.333	33H	8.000
04H	2.462	14H	4.800	24H	3.077	34H	6.400
05H	2.286	15H	4.000	25H	2.857	35H	5.333
06H	2.133	16H	3.429	26H	2.667	36H	4.571
07H	2.000	17H	3.000	27H	2.500	37H	4.000
08H	1.882	18H	2.667	28H	2.353	38H	3.556
09H	1.778	19H	2.400	29H	2.222	39H	3.200
0AH	1.684	1AH	2.182	2AH	2.105	3AH	2.909
0BH	1.600	1BH	2.000	2BH	2.000	3BH	2.667
0CH	1.524	1CH	1.846	2CH	1.905	3CH	2.462
0DH	1.455	1DH	1.714	2DH	1.818	3DH	2.286
0EH	1.391	1EH	1.600	2EH	1.739	3EH	2.133
0FH	1.333	1FH	1.500	2FH	1.667	3FH	2.000

Note: The gray part is prohibited for voltage detection.

3.1.55 R1C9/CMPCON1 (CMP Control Register 1)

0X1C9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON1	CMPOE	CMPINV	CMPIS<5:0>					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: CMPOE - Comparator result output enable

0: P67 as GPIO

1: Comparator result output from P67

Bit<6>: CMPINV-CMPOUT output result inverted

0: No inversion

1: Inversion

Bit<5>: CMPIS<5> - Voltage input from voltage divider resistor

0: VDD

1: Input from P61

Bit<4:3>: CMPIS<4:3> - Positive input source selection for comparator

CMPIS<4>	CMPIS<3>	Positive Input Source
0	0	Resistor Voltage Divider
0	1	CIN0+/P51
1	0	CIN1+/P53
1	1	1/2VREF

Bit<2:0>: CMPIS<2:0> - Negative Input Source Selection for Comparator

CMPIS<2>	CMPIS<1>	CMPIS<0>	Negative Input Source
0	0	0	CIN0-/P66
0	0	1	CIN1-/P67
0	1	0	CIN2-/P50
0	1	1	CIN3-/P65
1	0	0	CIN4-/P64
1	0	1	CIN5-/P62
1	1	0	Resistor Voltage Divider
1	1	1	1/2VREF

3.1.56 R1CA/E2PCON (EEPROM Control Register)

0X1CA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2PCON	E2PLOCK<3:0>				-	E2PTIME	E2PRDEN	E2PWREN
Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:4>: E2PLOCK<3:0> - EEPROM function unlock bit

1001: Write data **1001** unlock EEPROM write operation

0110: Write data 0110 unlock ISP function

Bit<3>: Unused

Bit<2>: E2PTIME - EEPROM write time selection bit

0: EEPROM write time selection fast mode

1: EEPROM write time selection slow mode

Bit<1>: E2PRDEN - EEPROM read enable bit

0: Disable

1: Enable

Bit<0>: E2PWREN - EEPROM write enable bit

0: Disable

1: Enable

3.1.57 R1CB/E2PDATL (EEPROM Data Low 8-bit Register)

0X1CB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2PDATL	E2PDAT<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.58 R1CC/E2PDATH (EEPROM Data High 8-bit Register)

0X1CC	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2PDATH	E2PDAT<15:8>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

3.1.59 R1D6/INTE0 (Interrupt Enable Control Register 0)

0X1D6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE0	PWM2DTIE	ADIE	CMPIE	INT1IE	INT0IE	E2PIE	P6ICIE	P5ICIE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM2DTIE - PWM2 duty cycle interrupt enable bit

0: Disable

1: Enable (Must enable PWM2EN bit to enter interrupt normally)

Bit<6>: ADIE - AD interrupt enable bit

0: Disable

1: Enable

Bit<5>: CMPIE - CMP interrupt enable bit

0: Disable

1: Enable

Bit<4>:INT1IE - INT1 interrupt enable bit

0: Disable

1: Enable

Bit<3>:INT0IE - INT0 interrupt enable bit

0: Disable

1: Enable

Bit<2>:E2PIE - E2P write complete interrupt enable bit

0: Disable

1: Enable

Bit<1>P6ICIE - P6IC interrupt enable bit

0: Disable

1: Enable

Bit<0>P5ICIE - P5IC interrupt enable bit

0: Disable

1: Enable

3.1.60 R1D7/INTE1 (Interrupt Enable Control Register 1)

0X1D7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTE1	-	-	-	-	-	TC2IE	TC1IE	TC0IE
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:3>: Unused

Bit<2>: TC2IE - TC2 interrupt enable bit

0: Disable

1: Enable

Bit<1>: TC1IE - TC1 interrupt enable bit

0: Disable

1: Enable

Bit<0>: TC0IE - TC0 interrupt enable bit

0: Disable

1: Enable

3.1.61 R1DA/INTF0 (Interrupt Flag Register 0)

0X1DA	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF0	PWM2DTIF	ADIF	CMPIF	INT1IF	INT0IF	E2PIF	P6ICIF	P5ICIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7>: PWM2DTIF - PWM2 duty cycle interrupt flag

0: Not triggered interrupt

1: Triggered interrupt

Bit<6>: ADIF - AD interrupt flag

0: Not triggered interrupt

1: Triggered interrupt

Bit<5>: CMPIF - CMP interrupt flag

0: Not triggered interrupt

1: Triggered interrupt

Bit<4>: INT1IF - INT1 interrupt flag

0: Not triggered interrupt

1: Triggered interrupt

Bit<3>: INT0IF - INT0 interrupt flag

0: Not triggered interrupt

1: Triggered interrupt

Bit<2>:E2PIF - E2P Write Completion Interrupt Flag

0: Not triggered interrupt

1: Triggered interrupt

Bit<1>: P6ICIF - P6IC interrupt enable bit

0: Not triggered interrupt

1: Triggered interrupt

Bit<0>: P5ICIF - P5IC interrupt flag bit

0: Not triggered interrupt

1: Triggered interrupt

3.1.62 R1DB/INTF1 (Interrupt Flag Register 1)

0X1DB	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTF1	-	-	-	-	-	TC2IF	TC1IF	TC0IF
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit<7:3>: Unused

Bit<2>: TC2IF - TC2 interrupt flag bit

0: Not triggered interrupt

1: Triggered interrupt

Bit<1>: TC1IF - TC1 interrupt flag bit

0: Not triggered interrupt

1: Triggered interrupt

Bit<0>: TC0IF - TC0 interrupt flag bit

0: Not triggered interrupt

1: Triggered interrupt

3.1.63 R1FF/IAR (Indirect Addressing Register)

0X1FF	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAR	IAR<7:0>							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	X	X	X	X	X	X	X	X

The Indirect Addressing Register is not an actual register; its main function is to serve as a pointer for indirect addressing. Any instruction that uses R1FF as a pointer actually corresponds to the address pointed to by R180-RSR<7:0> (RAM Selection Register).

3.2 Interrupt

The JZ8M2632 has 11 interrupt sources. Regardless of which interrupt is used, the global interrupt must be enabled, i.e., the "EI" instruction. The interrupt vector address is fixed at 008H. Below are the characteristics of each interrupt:

Interrupt Sources	Enable Condition	Interrupt Flag
TC0 Overflow Interrupt	EI + TC0IE=1	TC0IF
TC1 Overflow Interrupt	EI + TC1IE=1	TC1IF
TC2 Overflow Interrupt	EI + TC2IE=1	TC2IF
P5 Port Input Change Interrupt	EI + P5ICIE=1	P5ICIF
P6 Port Input Change Interrupt	EI + P6ICIE=1	P6ICIF
EEPROM Write Complete Interrupt	EI + E2PIE=1	E2PIF
INT0 External Interrupt	EI + INT0IE=1	INT0IF
External Interrupt INT1	EI + INT1IE=1	INT1IF
CMP Comparison Complete Interrupt	EI + CMPIE=1	CMPIF
ADC Conversion Complete Interrupt	EI + ADIE=1	ADIF
PWM2 Duty Cycle Overflow Interrupt	EI + PWM2DTIE=1&&PWM2EN=1	PWM2DTIF

R1DA/R1DB are interrupt flag registers that record the interrupt flag bits after an interrupt request is generated. R1D6/R1D7 are interrupt enable control registers, where the permission and prohibition of interrupts are set. The overall interrupt enable is set by the "EI" instruction, while the overall interrupt disable is set by the "DI" instruction. When an interrupt occurs, the execution of the next instruction will start from the interrupt vector address 008H. Before exiting the interrupt service routine, the corresponding interrupt flag bits must be cleared to avoid erroneous interrupt actions. Normally, it is prohibited to use bit operations or logical operations to clear interrupt flag bits; it is recommended to clear them by direct assignment (interrupt flag bits can only be cleared to zero, setting them to one is invalid).

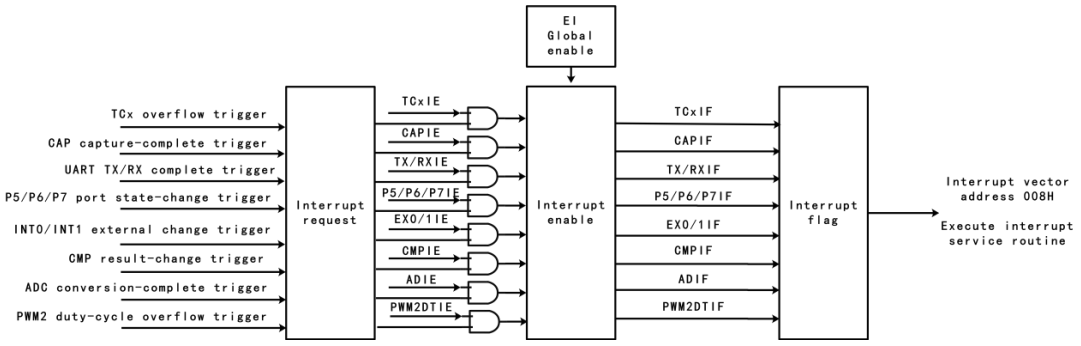
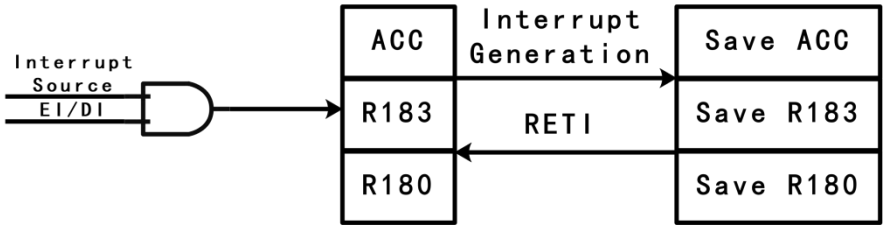


Diagram of Interrupt Principle

3.2.1 Interrupt Context Protection

During the interrupt response process, the hardware has a built-in interrupt protection function that saves the contents of ACC, R183, and R180 until exiting the interrupt service routine. The saved values are then reloaded into ACC, R183, and R180 to avoid any instructions that may change the values of ACC, R183, and R180 during the execution of the interrupt subroutine, which could lead to errors when returning to the main program. As shown in the figure below:



Interrupt Context Protection Diagram

3.3 Reset

3.3.1 Overview of Reset Function

The JZ8M2632 system provides four types of reset methods:

- POR Power-On Reset
- RESET Pin Low-Level Reset
- WDT Watchdog Overflow Reset
- LVR Low Voltage Reset

When any of the above reset events occur, all system registers are initialized to their reset values, the program stops running, and the program counter (PC) is set to zero. After the reset, the system begins to run again from vector 0000H.

Any reset situation requires a certain response time, and the system reset mechanism ensures the reliable reset of the MCU. The time required to complete the reset varies with different types of oscillators. Therefore, the rise time of VDD and the startup time of different oscillators are not fixed. The startup time of an RC oscillator is the shortest, while that of a crystal oscillator is longer. During the use of the user terminal, it is important to consider the application scenario's requirements for power-on reset time.

3.3.2 POR Power-On Reset

Power-on reset is closely related to LVR operations. The process of powering on the system presents a gradually rising curve and requires a certain amount of time to reach the normal voltage level.

- Power-on: The system detects the rise in power supply voltage and waits for it to stabilize;
- System initialization: All system registers are set to their initial values;
- Oscillator starts working: The oscillator begins to provide the system clock;
- Executing program: Power-on is complete, and the program starts running;

Power-on reset time is determined by the "Reset Time" selection in the OPTION, as shown in the table below:

PWRT and WDT	Reset establishment time
PWRT=WDT/2	13ms (followed by watchdog reset time)
PWRT=WDT/2	51ms (followed by watchdog reset time)
PWRT=WDT/2	205ms (followed by watchdog reset time)
PWRT ≠ WDT	350us (independent fixed reset time)

3.3.3 WDT watchdog reset

The watchdog reset is a protective setting for the system. Under normal conditions, the watchdog timer is reset by the program. If an error occurs and the system enters an unknown state, the watchdog timer overflows, causing the system to reset. After the watchdog reset, the system restarts and returns to normal operation.

- Watchdog timer status: The system checks whether the watchdog timer has overflowed; if it has, the system resets;
- System initialization: All system registers are set to their initialization default values;
- Oscillator starts working: The oscillator begins to provide the system clock;
- Executing program: Power-on is complete, and the program starts running;

Explanation of watchdog wake-up:

The watchdog reset can occur in both idle and sleep modes. After a system reset, the program execution starts from address 0X00. The user can check the time overflow bit (Bit4) of the R183 (STATUS) register. If it indicates a WDT watchdog overflow, it can be determined as a watchdog reset, triggering the corresponding wake-up subroutine.

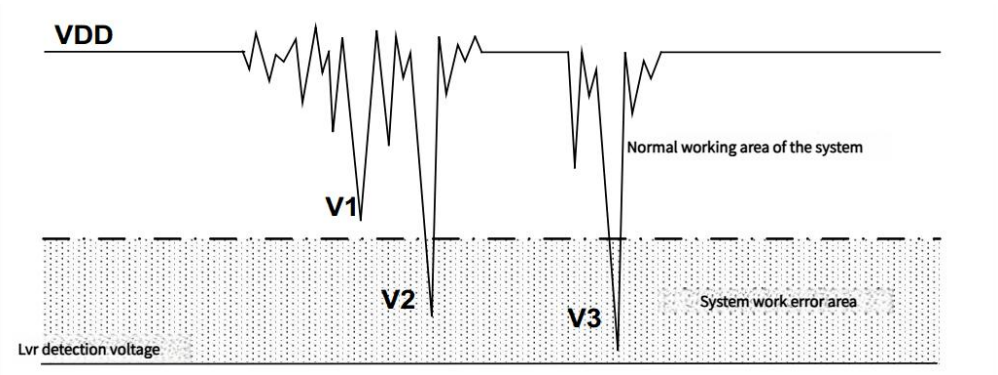
Note that the watchdog wake-up is essentially a special application of the watchdog reset.

Considerations for watchdog timer applications:

- Before clearing the watchdog, checking the status of I/O ports and RAM can enhance program reliability;
- Do not clear the watchdog within an interrupt, as this may prevent detection of the main program running away;
- The matching watchdog reset time in the program should only have one action to clear the watchdog in the main program. This architecture maximizes the protective function of the watchdog.

3.3.4 LVR Low Voltage Reset

Power-off reset addresses situations where external factors cause a drop in system voltage (e.g., interference or changes in external load). Power-off may lead to abnormal system operation or program execution errors.



A voltage drop may lead the system into a dead zone. The dead zone means that the power supply cannot meet the minimum operating voltage requirements of the system. The above diagram is a typical illustration of a power-off reset. In the diagram, VDD is severely disturbed, and the voltage drops very low. The area above the dashed line indicates normal system operation, while the area below the dashed line indicates an unknown operating state, referred to as the dead zone. When VDD drops to V1, the system remains in a normal state; when VDD drops to V2 and V3, the system enters the dead zone, which is prone to errors. The following situations may cause the system to enter the dead zone:

In DC applications:

DC applications generally use battery power. When the battery voltage is too low or the microcontroller drives a load, the system voltage may drop and enter the dead

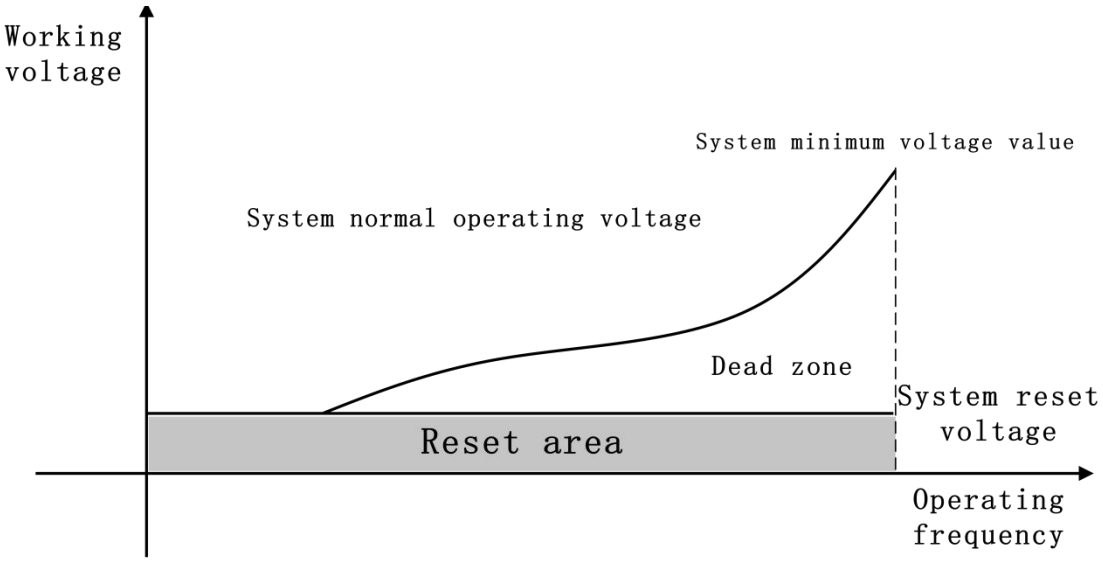
zone. At this point, the power supply will not further decrease to the LVR detection voltage, thus keeping the system in the dead zone.

In the application of AC:

When the system uses AC power supply, the DC voltage value is affected by noise in the AC power source. When the external load is too high, such as when driving a motor, the interference generated by the load also affects the DC power supply. If VDD drops below the minimum operating voltage due to interference, the system may enter an unstable operating state. In AC applications, the power-up and power-down times of the system are relatively long. The power-up timing protection ensures that the system powers up normally, but the power-down process is similar to that in DC applications. After the AC power supply is turned off, the VDD voltage gradually decreases and is prone to entering a dead zone.

3.3.5 Relationship between operating frequency and LVR low voltage detection

To improve the performance of the system's power-off reset, it is essential to clarify the minimum operating voltage value of the system. The minimum operating voltage of the system is related to the execution speed, and the minimum operating voltage value varies at different execution speeds.



As shown in the figure above, the normal operating voltage region of the system is generally higher than the system reset voltage, which is determined by the low voltage detection (LVR) level. When the execution speed of the system increases, the

minimum operating voltage of the system also increases accordingly. However, since the system reset voltage is fixed, a voltage region will appear between the minimum operating voltage and the system reset voltage, where the system cannot operate normally and will not reset. This region is the dead zone.

To avoid the occurrence of dead zone voltage, it is necessary to select the corresponding LVR reset voltage point when choosing the operating frequency. As shown in the table below:

Fosc Frequency	Clocks Division	LVR Reset Voltage Point
Fosc -16MHz	2 Clocks	LVR=2.9V
Fosc-8MHz	2 Clocks	LVR=2.2V
Fosc-4MHz	2 Clocks	LVR=2.0V

Note: 1. Operating frequency = Instruction cycle frequency = Fosc frequency / Clocks division;

2. The corresponding values of this operating frequency and LVR reset voltage point are only recommended values. Users can adjust the reset voltage point appropriately based on the specific application scenario.

3.4 Operating mode

The JZ8M2632 can operate in four different modes with varying clock frequencies. These modes can control the operation of the oscillator, the execution of programs, and the functional loss of analog circuits.

- High-speed mode: The system clock selects the internal high-speed clock, while the low-speed clock operates normally;
- Low-speed mode: System clock selection uses internal low-speed clock, and the high-speed clock is paused;
- Idle mode: The system clock operates normally while other parts of the system enter sleep mode (TC0, TC1, TC2 can select the system clock to continue working and wake up the system). It can also be awakened through P5IWE, P6IWE, INT0WE, INT1WE, ADCWE, CMPWE;
- Sleep mode: All functions are paused, and the system enters sleep mode. It can be awakened through TC0 (P62 external input clock), P5IWE, P6IWE, INT0WE, INT1WE, CMPWE;

Functional module	High-speed mode	Low-speed mode	Idle mode	Sleep mode
IHRC	Run	Stop	Run	Stop
ILRC	Run	Run	Run	Stop
CPU	Execution	Execution	Stop	Stop
TC0	Operational	Operational	Operational	Operational (P62 Input Clock)
TC1	Operational	Operational	Operational	Stop
TC2	Operational	Operational	Operational	Stop
Interrupt	All Valid	All Valid	All Valid (TC0, TC1, TC2 Select System Clock)	TC0IE, P5ICIE, P6ICIE, INT0IE, INT1IE, CMPIE
Wake-up function	-	-	(TC0, TC1, TC2 can wake up when selecting the system clock) P5IWE, P6IWE, INT0WE, INT1WE, ADCWE, CMPWE	TC0WE, P5IWE, P6IWE, INT0WE, INT1WE, CMPWE
Watchdog	WDT option	WDT option	WDT option control	WDT option

3.4.1 High-speed mode

High-speed mode is the system high-speed clock operating mode, with the system clock source provided by the high-speed RC oscillator. The program is executed. After power-on reset or any reset trigger, the system enters high-speed mode to execute the program. In high-speed mode, the high-speed oscillator operates normally, and power consumption is at its maximum.

- The program is executed, and all functions can be controlled;
- The system rate is high-speed;
- Both the high-speed oscillator and the internal low-speed oscillator operate normally;
- High-speed mode can switch to low-speed mode;
- Entering sleep mode from high-speed mode, and returning to high-speed mode after waking up;
- Entering idle mode from high-speed mode, and returning to high-speed mode after waking up;

3.4.2 Low-speed mode

Low-speed mode is the system's low-speed clock operating mode. The system clock source is provided by a low-speed RC oscillator. Low-speed mode is controlled by the CLKMD bit in the CPU mode control register. When CLKMD=0, the system is in high-speed mode; when CLKMD=1, the system enters low-speed mode. After entering low-speed mode, the system cannot automatically disable the high-speed RC oscillator and must be disabled by setting SPTHX=1 to reduce power consumption.

- The program is executed, and all functions can be controlled;
- The system rate is low-speed;
- The internal low-speed oscillator operates normally, while the high-speed oscillator stops working.
- Low-speed mode can switch to high-speed mode;

- Entering sleep mode from low-speed mode, and returning to low-speed mode after waking up;
- Entering idle mode from low-speed mode, and returning to low-speed mode after waking up;

3.4.3 Idle mode

Idle mode is another ideal state. In sleep mode, all functions and hardware devices are disabled, but in idle mode, the system clock remains operational, and the power consumption in idle mode is greater than that in sleep mode. In idle mode, no programs are executed, but the wake-up functions of TC0, TC1, TC2, P5IWE, P6IWE, INT0WE, INT1WE, ADCWE, and CMPWE still operate normally, with the clock source for timers TC0, TC1, and TC2 being the still-operational system clock. Whether to enter idle mode is determined by the IDLE bit in the system clock and status control register; when IDLE=1, executing SLEEP will enter idle mode.

- The program has stopped executing, and all functions are disabled;
- The module with wake-up function is working normally;
- The system clock is working normally;
- Transitioning from high-speed mode to idle mode, and returning to high-speed mode after being awakened;
- Transitioning from low-speed mode to idle mode, and returning to low-speed mode after being awakened;
- The wake-up methods in idle mode are P5IWE, P6IWE, INT0WE, INT1WE, ADCWE, CMPWE;
- Functions TC0, TC1, and TC2 remain effective in idle mode;

3.4.4 Sleep mode

Sleep mode is the ideal state of the system, where no programs are executed, and the oscillator also stops working. The total power consumption of the chip is less than 3 uA. Sleep mode can be awakened by TC0 (P62 input clock), P5IWE, P6IWE, INT0WE, INT1WE, CMPWE. Transitioning from high-speed mode or low-speed mode to sleep mode,

it will return to the corresponding mode after being awakened. The entry into sleep mode is controlled by the system clock and the IDLE bit of the status control register; when IDLE=0, executing SLEEP will enter sleep mode.

- The program has stopped executing, and all functions are disabled;
- All oscillators, including the external high-speed oscillator, internal high-speed oscillator, and internal low-speed oscillator, stop working;
- Power consumption is less than 3 uA;
- Transitioning from high-speed mode to sleep mode, and returning to high-speed mode after being awakened;
- Transitioning from low-speed mode to sleep mode, and returning to low-speed mode after being awakened;
- The wake-up methods in sleep mode are TC0 (P62 input clock), P5IWE, P6IWE, INT0WE, INT1WE, CMPWE;

3.5 System Clock

The JZ8M2632 integrates two types of oscillators: a high-speed RC oscillator (IHRC) and a low-speed RC oscillator (ILRC), allowing for system clock switching between high-speed and low-speed oscillators via the R188/CPUCON register.

3.5.1 Internal IHRC Oscillator

The JZ8M2632 features a built-in IHRC high-speed oscillator, providing adjustable IHRC frequency with a default value of 8MHz, and the IHRC frequency can be fine-tuned via the IHRCCAL register.

The IHRC oscillator includes four frequency values: 1M/4M/8M/16M Hz. By setting the configuration bits of OPTION, the IHRC operating frequency can be selected, as shown in the corresponding relationship below:

RCM	IRC Frequency
1M	The system clock frequency (Fosc) is selected as 1 MHz.
4M	The system clock frequency (Fosc) is selected as 4MHz
8M	The system clock frequency (Fosc) is selected as 8MHz
16M	The system clock frequency (Fosc) is selected as 16MHz

JZ8M2632 provides multiple frequency division options, which can be selected in OPTION, suitable for more occasions. As shown in the table below:

Clocks	Clocks Division
2clock	The 2 division of the system clock (Fcpu)
4clock	4-division of system clock (Fcpu)
8clock	8-division of system clock (Fcpu)
16clock	16-division of system clock (Fcpu)
32clock	32-division of system clock (Fcpu)

3.5.2 Internal ILRC Oscillator

The JZ8M2632 has a built-in ILRC low-speed oscillator that provides a stable 40KHz low-speed clock.

3.6 I/O port

JZ8M2632 has 2 sets of bidirectional I/O ports, with a total of 14 inputs and 14 outputs. Most I/O can be reused for other functions.

14 programmable pull-up I/O pins: P50 to P55, P60 to P67;

14 programmable pull-down I/O pins: P50 to P55, P60 to P67;

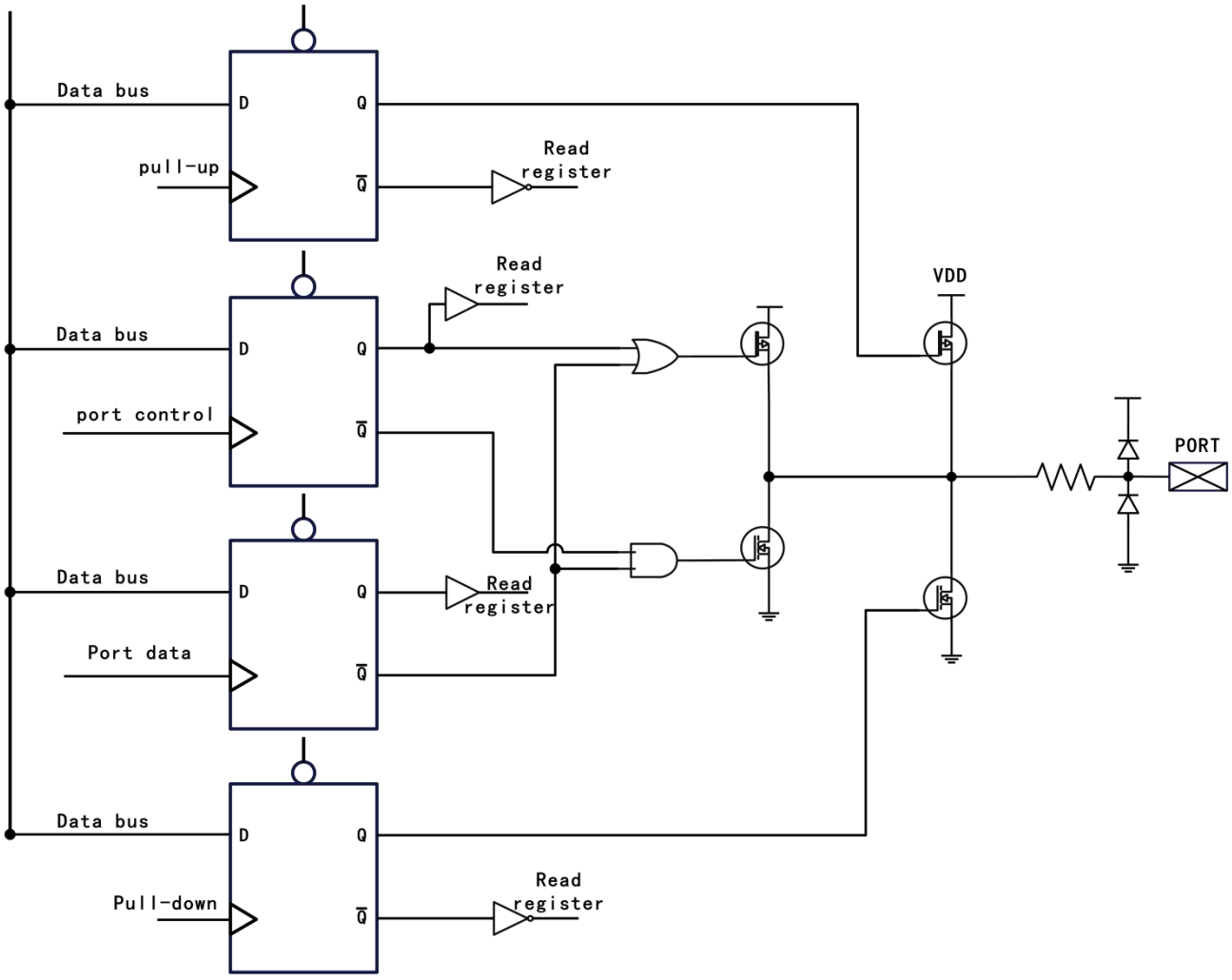
7 selectable option drive enhanced I/O pins: P50 to P54, P66 to P67;

14 programmable wake-up I/O pins: P50 to P55, P60 to P67;

14 programmable analog ports: P50 to P55, P60 to P67;

3.6.1 GPIO internal structure diagram

The following internal structure diagram is for reference only and does not represent the actual circuit.



IO control register/data register/pull-up/pull-down structural circuit

3.6.2 Port input change wake-up

JZ8M2632 includes 14 programmable port input change wake-up I/O: P50 to P55, P60 to P67. The chip can enter sleep mode or idle mode by executing the "SLEEP" instruction. At this time, the CPU does not execute instructions. The port input change wake-up can continue to execute the original process (DI executed before SLEEP) or perform an interrupt jump (EI executed before SLEEP) by program selection, requiring the corresponding interrupt enable control to be turned on. After the port input change wake-up, it jumps to the interrupt service routine.

Port status change query wake-up settings:

1. Set the wake-up port for input changes to input;
2. Choose internal pull-up or pull-down for the wake-up port as needed;
3. Enable port input change wake-up control P5IWE/P6IWE;
4. Execute the DI instruction, do not enter the interrupt address port;
5. Execute the "SLEEP" instruction, IDLE=0 to enter sleep mode or IDLE=1 to enter idle mode;
6. After waking up, execute the next instruction after SLEEP;

Port status change interrupt wake-up settings:

1. Set the wake-up port for input changes to input;
2. Choose internal pull-up or pull-down for the wake-up port as needed;
3. Enable port input change wake-up control P5IWE/P6IWE;
4. Enable port input change interrupt P5ICIE/P6ICIE;
5. Execute the "EI" instruction, waiting to enter the interrupt address port;
6. Execute the "SLEEP" command; IDLE=0 enters sleep mode or IDLE=1 enters idle mode.
7. After waking up, it will enter the interrupt address, and after exiting the interrupt, it will execute the next instruction of SLEEP;

3.6.3 Port Schmitt parameters

The Schmitt characteristics of the JZ8M2632 port are as follows (for reference only):

Port	SMT	
P50～P55	0.25*VDD	0.54*VDD
P60～P67	0.25*VDD	0.54*VDD

The above parameters are for reference only; please refer to the actual measured data of the target prototype.

3.7 Timer Counter

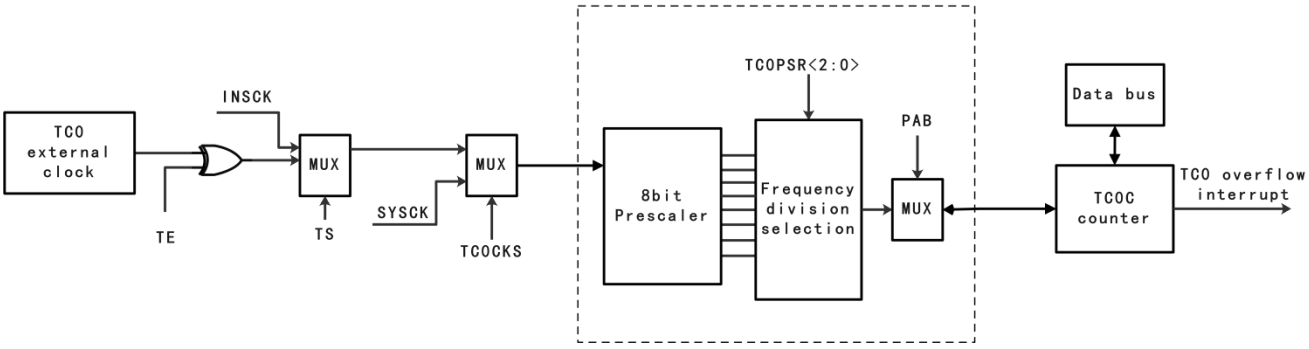
3.7.1 TC0 Timer Counter

The JZ8M2632 provides an 8-bit timer counter as the TC0 prescaler. The TC0PTEN bit in the TC0CON register determines whether the prescaler is enabled, and the TC0PSR<2:0> three bits determine the prescale ratio.

TC0 is an 8-bit up counter. After enabling TC0EN, the TC0 timer starts working. The clock source can be the internal instruction clock, system clock, or low-speed clock, and an external clock can also be selected (input via the P62 pin, with selectable trigger edge). The counter increments by 1 with each clock pulse.

TC0 count overflow can generate an interrupt signal.

In IDLE mode, the TC0 overflow interrupt can wake up the circuit, and after waking up, it can choose to enter the interrupt or continue executing the original program. In sleep mode, when TC0 is set to the P62 external input clock, it can interrupt on overflow and wake up the circuit.



TC0 Structural Block Diagram

3.7.1.1 TC0 Timer Setting Instructions

1. Assign an initial value to the TC0C register;
2. Set the value of the TC0CON register (select clock source and prescale ratio);
3. To be used as a counter, it is necessary to select the TC0 signal source as an external input signal in the TC0CON register;

4. After all configurations are set, finally set the TC0EN in the TC0CON register to enable the timer counter;
5. If interrupt functionality is required, set TC0IE (Bit0) in the INTE1 register to 1 and execute the EI instruction;
6. The system will automatically save ACC, STATUS, and RSR data when executing the interrupt service routine. After executing the RETI instruction, the data will be automatically restored. Before exiting the interrupt, the TC0 interrupt flag must be cleared;

3.7.1.2 TC0 Timer Calculation Explanation

The TC0 timing function is achieved by writing a value to the TC0C register, assigning an initial value to the timer, which starts counting from the initial value until it overflows and generates an interrupt.

TC0 Timing Time Calculation Formula (Selecting Internal System Clock):

$$\text{TC0 Timing duration} = (1/\text{Fosc}) \times (\text{TC0 } \textit{division}) \times (256 - \text{TC0 } \textit{Initial value})$$

Example:

Fosc=8 MHz, TC0 Prescaler Selection=8, TC0 Initial Value=156;

$$\text{TC0 Timing duration} = (1/8) \times (8) \times (256 - 156) = 100 \text{ us}$$

TC0 Timing Time Calculation Formula (Selecting External Input Clock):

$$\text{TC0 Timing duration} = (1/\text{External input clock}) \times (\text{TC0 } \textit{division}) \times (256 - \text{TC0 } \textit{Initial value})$$

Example:

External Input Clock=1 MHz, TC0 Prescaler Selection=4, TC0 Initial Value=156;

$$\text{TC0 Timing duration} = (1/1) \times (4) \times (256 - 156) = 400 \text{ us}$$

3.7.1.3 TC0 Idle Mode Wake-Up Description

In idle mode, system instructions stop executing, while modules with wake-up functionality and the system clock operate normally, and other functions are disabled.

TC0 can wake up from idle mode by setting Bit 3 of the R188/CPUCON register (TC0WE) to 1. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle

mode, and the TC0 timer operates normally (selecting the system clock). After the TC0 timer overflows, the system is awakened. If TC0IE and EI are enabled, it will enter an interrupt after waking up; if DI is executed, it will execute the next instruction after waking up.

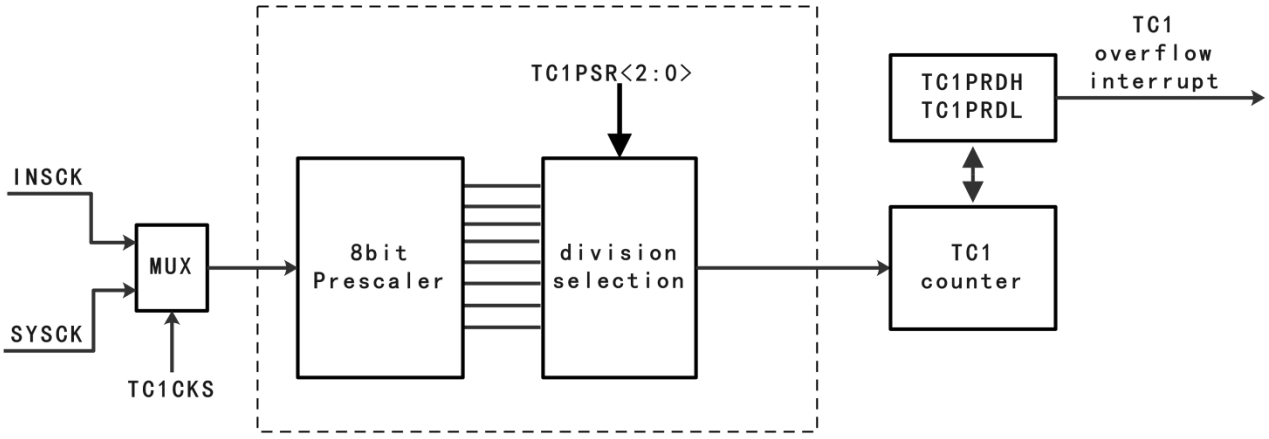
When the clock source is selected as the external clock from P62, enabling TC0WE=1 and directly executing the SLEEP instruction can also wake up the system.

3.7.2 TC1 Timer Counter

The TC1 timer counter provides an 8-bit prescaler, with the TC1PSR<2:0> bits in the TC1CON register determining the prescale ratio.

TC1 is a 12-bit up counter. The TC1 timer must be enabled (TC1EN) to operate, with the clock source selectable as either the system clock or the instruction clock. With each clock cycle, the counter increments by 1. When the TC1 count value matches the TC1PRD setting, an overflow occurs. If TC1IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service routine.

In IDLE mode, the TC1 interrupt can wake up the circuit (with the clock being the system clock). After waking up, it can either enter the interrupt or continue executing the original program.



TC1 Structural Block Diagram

3.7.2.1 TC1 Timer Setting Description

1. Assign initial values to the TC1PRD<11:0> register;
2. Set the TC1CON register and configure the prescaler as needed;
3. Enable the TC1IE interrupt in the R1D7/INTE1 register and execute the EI instruction;
4. Enable TC1EN to start the TC1 timer counting;
5. The system will automatically save ACC, STATUS, and RSR data when executing the interrupt service routine. After executing the RETI instruction, the data will be automatically restored, and the TC1 interrupt flag must be cleared before exiting the interrupt;

3.7.2.2 TC1 Timing Calculation Description

The TC1 timing function starts counting by writing a value to TC1PRD<11:0>. The timer will accumulate until the timer count matches the TC1PRD<11:0> value, at which point an overflow will trigger the execution of the interrupt service routine.

TC1 Timing Calculation Formula:

$$\text{TC1Timing duration} = (1/\text{Fosc}) \times (\text{TC1 } division) \times \text{TC1PRD}$$

Example:

Fosc = 16 MHz, TC1 prescaler selection = 16, TC1PRD value = 512;

$$\text{TC1Timing duration} = (1/16) \times (16) \times 512 = 512\text{us}$$

3.7.2.3 TC1 Idle Mode Wake-up Description

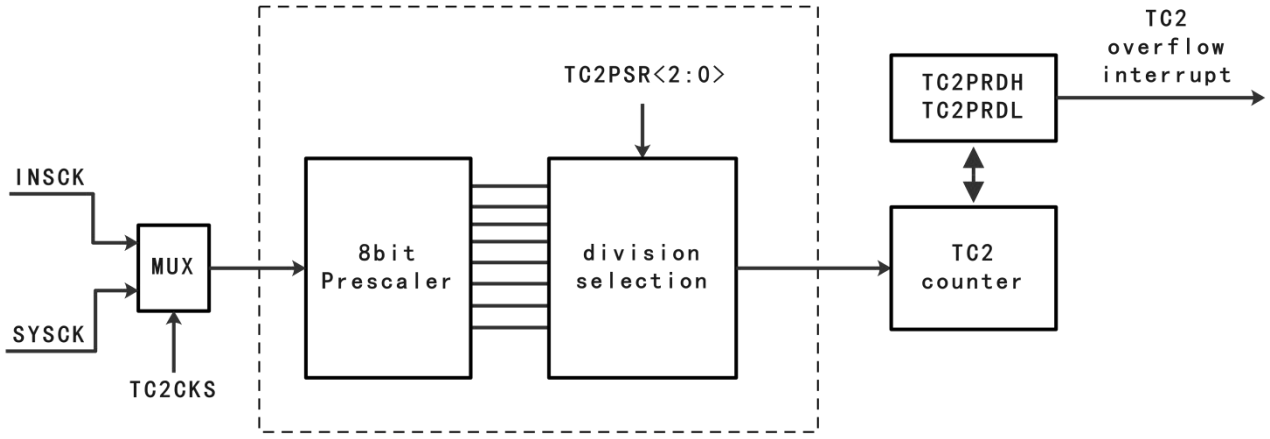
TC1 can wake up from idle mode by enabling the TC1WE bit in the R188/CPUCON register and selecting the TC1 clock source as the system clock. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC1 timer operates normally. After the TC1 timer overflows, the system is awakened. If TC1IE and EI are enabled, it will enter an interrupt after waking up; if DI is executed, it will execute the next instruction after waking up.

3.7.3 TC2 Timer Counter

TC2 Timer Counter provides an 8-bit prescaler, with the TC2PSR<2:0> bits in the TC2CON register determining the prescale ratio.

TC2 is a 12-bit up counter. The TC2 timer must be enabled by setting TC2EN to function, and the clock source can be either the system clock or the instruction clock. With each clock cycle, the counter increments by 1. The TC2 count value matches the TC2PRD set value to generate an overflow. If TC2IE and EI are enabled, the system jumps to the corresponding interrupt vector address to execute the interrupt service routine.

In IDLE mode, the TC2 interrupt can wake up the circuit (with the clock being the system clock). After waking up, it can choose to enter the interrupt or continue executing the original program.



TC2 Block Diagram

3.7.3.1 TC2 Timer Configuration Instructions

1. Assign an initial value to the TC2PRD<11:0> register;
2. Set the TC2CON register and configure the prescale ratio as needed;
3. Enable the TC2IE in the R1D7/INTE1 register to turn on interrupt enable and execute the EI instruction;
4. Enable TC2EN to start the TC2 timer counting;
5. The system's interrupt service routine will automatically save the ACC, STATUS, and RSR data. After executing the RETI instruction, the data will be

automatically restored. Before exiting the interrupt, the TC2 interrupt flag must be cleared;

3.7.3.2 TC2 Timer Calculation Description

The TC2 timing function starts counting by writing a value to TC2PRD<11:0>. The timer continues to accumulate until the timer count matches the TC2PRD<11:0> value, at which point an overflow triggers the interrupt service routine.

TC2 Timing Time Calculation Formula:

$$\text{TC2 Timing duration} = (1/\text{Fosc}) \times (\text{TC2 } \textit{division}) \times \text{TC2PRD}$$

Example:

Fosc=16 MHz, TC2 Prescaler Selection=16, TC2PRD Value=512;

$$\text{TC2 Timing duration} = (1/16) \times (16) \times 512 = 512\text{us}$$

3.7.3.3 TC2 Idle Mode Wake-up Description

TC2 can wake up from idle mode by enabling the TC2WE bit in the R188/CPUCON register and selecting the TC2 clock source as the system clock. When IDLE = 1 and the SLEEP instruction is executed, the system enters idle mode, and the TC2 timer operates normally. After the TC2 timer overflows, the system is awakened. If TC2IE and EI are enabled, it will enter an interrupt after waking up; if DI is executed, it will proceed to the next instruction after waking up.

3.8 PWM Pulse Width Modulation

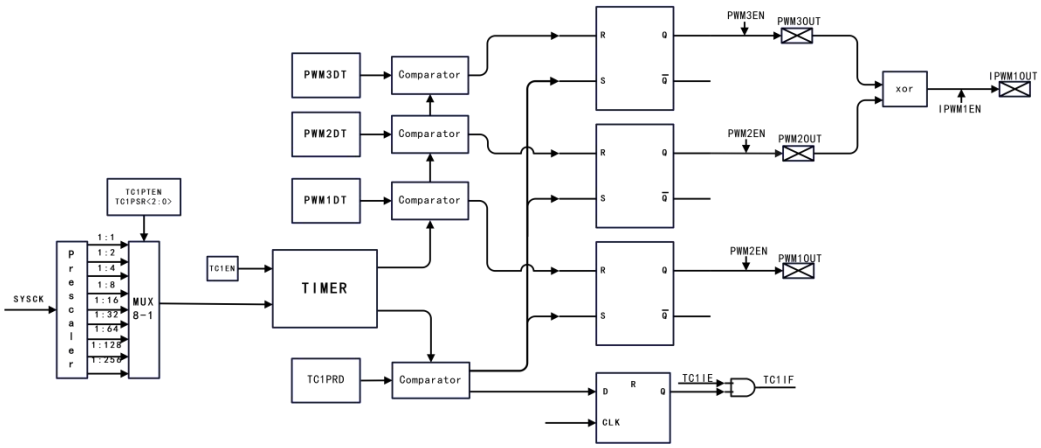
The JZ8M2632 provides 2 sets of 12-bit TC1 and TC2 counters, each of which can be divided into three PWM channels to generate pulse width modulation signals. The PWM output waveform is determined by the period and duty cycle, while the transmission rate is determined by the period. The chip provides complementary outputs with dead time, where PWM2 and PWM3 are XORed to form IPWM1, and PWM1 serves as the complementary signal. (IPWM4 is the same as IPWM1)

The PWM has a period overflow interrupt, which can be enabled to jump to the interrupt.

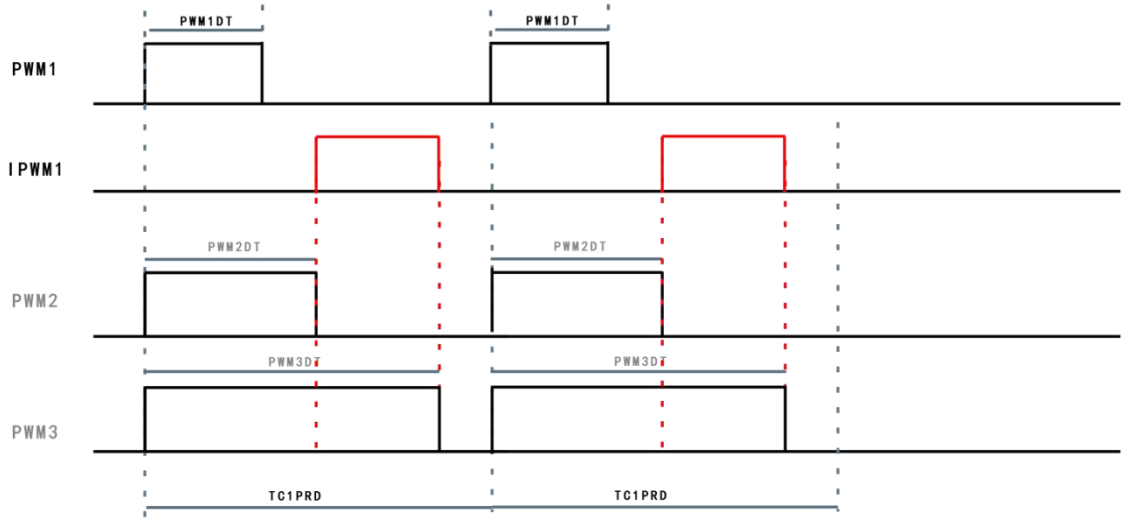
In IDLE (Idle Mode), TC1 and TC2 can wake up the system by selecting TC1CKS=1, TC2CKS=1 in the TC1 and TC2 control registers, and enabling TC1WE and TC2WE in the CPU mode control register.

3.8.1 PWM Internal Structure and Timing

The following internal structure diagram is for reference only and does not represent the actual circuit.



PWM Working Structure Circuit



3-Channel Common Period PWM and IPWM Timing Description

3.8.2 PWM Cycle and Duty Cycle

PWM provides a 12-bit clock counter with an 8-bit programmable prescaler, serving as the baud rate clock generator for the PWM module. The counter function can be enabled by setting the TCxEN bit in the TCxCON control register. The prescaler settings for the counter can be configured using the TCxPSR<2:0> control bits. PWMxE and IPWMxE enable the PWM function and the complementary PWM function, respectively.

The PWM cycle is set by writing values to the TCxPRDL (low eight bits) and TCxPRDTH (high four bits) period registers. When the counter value equals the PRD value, the following events occur in the next increment cycle:

- Counter reset;
- Corresponding PWM output pin set to high;
- Generate PWM period overflow interrupt (if enabled);
- PWM duty cycle is latched from PWMxDTL/TCxPRDTH registers to the DT/TIMER compare register;

PWM cycle calculation formula:

$$\text{PWM Period} = (\text{PRD}) \times (\text{PWM_CK}) \times (\text{PWM } division)$$

Example:

TCxRD=100, Fosc=16MHz, PWMCKS=1, PWM prescaler selection=2 prescaler;

$$\text{PWM Period} = (100) \times (1/16) \times (2) = 12.5\ \text{us}$$

PWM duty cycle is set by writing a value to the PWM duty cycle register. When the counter overflows and resets to zero, the value of PWMxDT is latched into the DT/TIMER comparison register. When the value of the DT/TIMER comparison register equals the TIMER counter value, the PWM output pin is set to low. The value of PWMxDT can be written at any time, but the value of the DT/TIMER comparison register is only written during a period overflow:

PWM duty cycle calculation formula:

$$\text{PWM Duty cycle} = (\text{DT}) \times (\text{PWM_CK}) \times (\text{PWM } \textit{division})$$

Example:

PWMxDT=50, Fosc=16MHz, PWMCKS=1, PWM prescaler selection=2 prescaler;

$$\text{PWM Duty cycle} = (50) \times (1/16) \times (2) = 6.25\ \text{us}$$

3.8.3 PWM idle mode wake-up description

In idle mode, CPU instruction execution stops, while modules with wake-up functionality and the system clock operate normally, and other functions are disabled.

PWM can wake up from idle mode by setting TC1/TC2WE wake-up enable, selecting the clock source as the system clock (SYSCK). Set the corresponding period or duty cycle interrupt enable, set IDLE (R188) to 1, and use the SLEEP instruction to enter idle mode, allowing the PWM timer to operate normally.

When the corresponding interrupt condition is met, the system is awakened. If EI is enabled, it enters an interrupt after waking up; if DI is enabled, it executes the next instruction after waking up.

3.8.4 PWM comparator gating description

The gating function of PWM1 is controlled by the PWM1GATE of the TC1CON register. When PWM1GATE=1, the PWM1 output is controlled by the comparator result; when CMP_FLAG=0, it outputs the PWM waveform, and when CMPOUT=1, PWM1 remains at low level.

The gate function of PWM4 is controlled by the PWM4GATE<1:0> of the TC2CON register. When PWM4GATE<0>=1, the PWM output is controlled by the comparator result, and a PWM waveform is output when CMP_FLAG=0. When PWM4GATE<1>=1, the PWM output is controlled by the external interrupt EXINT (P60), and a PWM waveform is output when EXINT=1.

3.8.5 IPWM waveform and Buzzer settings description

The IPWM waveform is not directly inverted; instead, IPWM1EN is enabled, and the outputs of PWM2 and PWM3 are XORed. If IPWM1EN is enabled at this time, the output selection control bit can choose to output from P52/P61 through PWM2; enabling PWM3EN allows the output selection control bit to choose from P51/P63 through PWM3. It also supports simultaneous output of the IPWM1 waveform from two ports.

Similarly, enabling IPWM4EN outputs the XOR of PWM5 and PWM6. If PWM5EN is enabled at this time, the output selection control bit can choose to output from P65/P67 through PWM5; enabling PWM6EN allows the output selection control bit to choose from P64/P66 through PWM6. It also supports simultaneous output of the IPWM4 waveform from two ports.

The PWM module also includes a buzzer function, which can be enabled for PWM output through the control bit BZXEN (R1B7, R1BF). The buzzer can select ports through PWM1S (R1B7) and PWM4S (R1BF), outputting from P60/P53 and P50/P62, respectively. It is important to note that to enable the buzzer, PWM1EN and PWM4EN must be cleared, and the corresponding output ports must be set to output.

3.8.6 PWM2DT interrupt and (single) trigger ADC description

PWM2DT provides the function of triggering an interrupt based on the duty cycle. After enabling PWM2DTIE (R1D6) and turning on PWM2EN, executing the EI instruction will enter the interrupt program based on the configured PWM2 duty cycle.

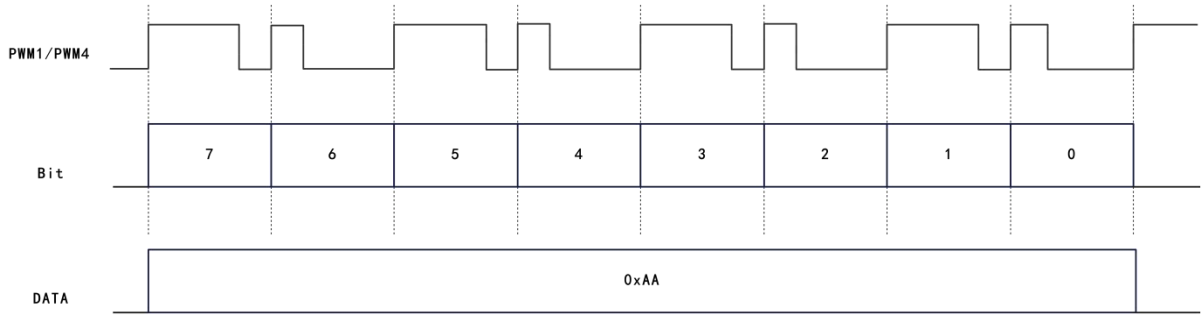
PWM can be configured to trigger ADC conversion based on the PWM2 duty cycle by setting ADCGATE (R1A7) to position 1, so that the ADC conversion will be triggered on the falling edge of the PWM2 duty cycle.

It can also enable single triggering of the ADC by setting PWM2_PULSE_EN (R1AE) to position 1. After a single trigger, PWM2 stops outputting, and the user can re-enable the PWM single trigger for ADC through software.

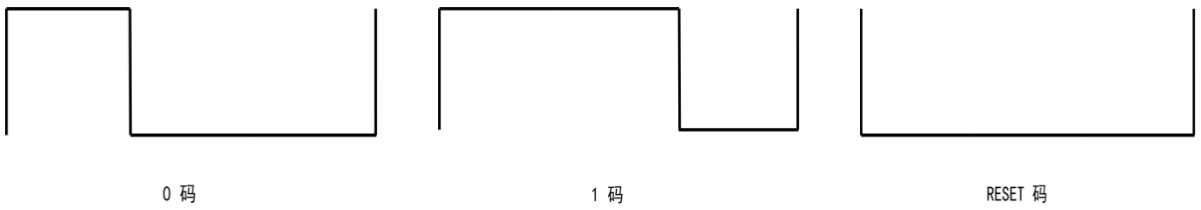
Note: The clock level that triggers ADRUN should be maintained for half a PWM2 clock cycle. In applications, avoid having the trigger level time exceed the ADC conversion period.

3.9 LED single-line cascading

JZ8M2632 supports 2-channel single-wire cascading LED driving, outputting cascading control timing through PWM1 and PWM4 ports. The timing diagram for cascading LED driving is as follows:



Single-wire cascading LED timing description



PWM1 and PWM4 are two independent single-wire cascading LED driving controls. When using PWM1 as the LED driving control, the period of the 0/1 code type is set by the TC1PRD period register, the high-level time of the 0 code type is set by the PWM1 duty cycle register, the high-level time of the 1 code type is set by the PWM2 duty cycle register, and the data to be sent is set by the lower 8 bits of the PWM3 duty cycle register. After enabling PWM1_LEDEN (R186) + TC1EN, the transmission of 8-bit cascading data begins, output from the PWM1 port. After the transmission of the 8-bit cascading data is completed, TC1EN automatically resets to zero, and re-enabling TC1EN starts the transmission of the next 8-bit cascading data.

When using PWM4 as the LED driving control, the period of the 0/1 code type is set by the TC2PRD period register, the high-level time of the 0 code type is set by the PWM4 duty cycle register, the high-level time of the 1 code type is set by the PWM5 duty cycle register, and the data to be sent is set by the lower 8 bits of the

PWM6 duty cycle register. After enabling PWM4_LEDEN (R186) + TC2EN, the transmission of 8-bit cascading data begins, output from the PWM4 port. After the transmission of the 8-bit cascading data is completed, TC2EN automatically resets to zero, and re-enabling TC2EN starts the transmission of the next 8-bit cascading data.

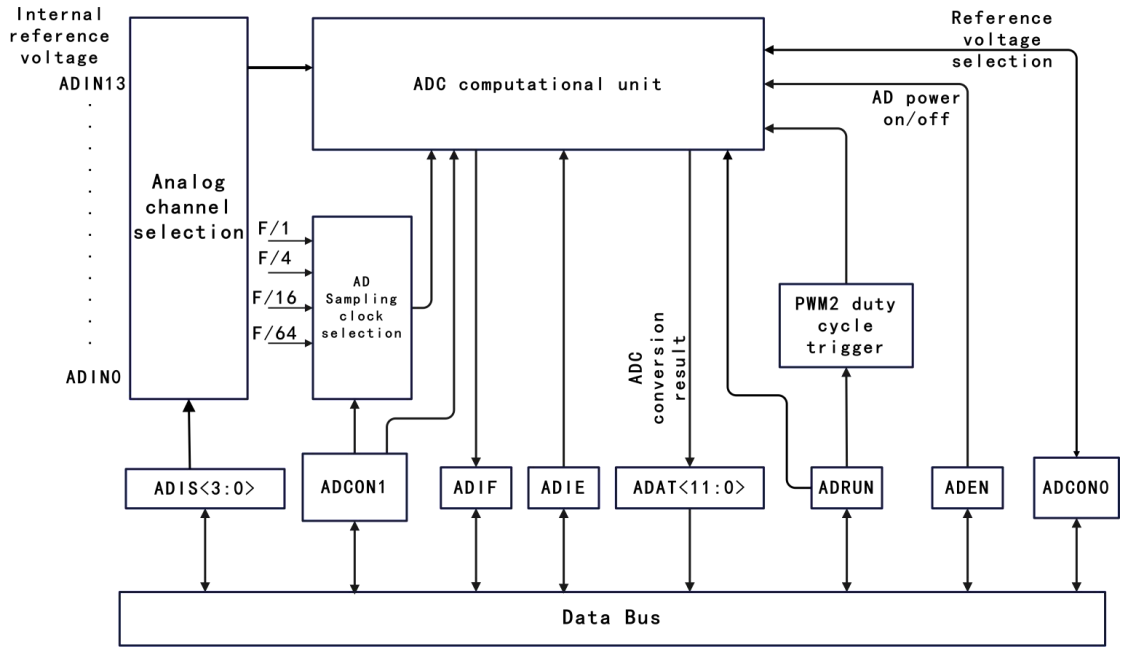
3.10 ADC Analog-to-Digital Conversion

The JZ8M2632 ADC module provides a 12-bit precision SAR ADC converter, including 15 analog channels.

The ADC converter uses a successive approximation method for analog-to-digital conversion, with results stored in R1A3/ADATH (ADC data high 8-bit register), R1A4/ADATL (ADC data low 8-bit register), and R1A6/ADCON0 (ADC control register 0). The channel selection, internal/external reference voltage source, sampling clock, ADC start, and ADC power consumption are controlled through the ADCON0 and ADCON1 control registers. When switching ADC channels, it is important to add a certain delay before the next conversion.

AD conversion completion can trigger an interrupt, or the ADRUN bit in R1A7/ADCON1 can be queried to determine completion.

If the AD wake-up function is enabled, the completion of AD conversion can wake the system from sleep mode or idle mode.



AD conversion function schematic diagram

AD Conversion Time:

The time to convert 1 bit in an AD conversion is defined as TAD, and a complete 12-bit ADC conversion requires 16 TAD cycles. It is essential to strictly adhere to the TAD time specifications to ensure normal sampling and obtain correct results. The time settings required for different reference voltages and different VDD levels also vary; please refer to the table below for reasonable frequency division settings.

Reference Voltage/V	Operating Voltage/V	Fastest Frequency Division Setting Fosc=16MHz	Conversion Time/us
VDD	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64
4	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64
3	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64
2	4.0～5.5	Fosc/16	16
	2.7～4.0	Fosc/64	64

AD Sampling Voltage Value Calculation:

$$\text{ADC } sampling\ voltage = \frac{\text{Sampling value}}{4096} * \text{Reference voltage}$$

For example: The reference voltage is an internal reference of 3V, and the sampled value is 0x800=2048

$$\text{ADC } sampling\ voltage = \frac{2048}{4096} * 3 = 1.5\text{V}$$

3.10.1 Explanation of ADC Power Supply Voltage Detection

By configuring the ADCCON0 (R1A6) register, the channel selection bits ADIS<7:4> select 0.254*VDD as the sampling channel. The VREF<2:0> in the ADCON1 (R1A7) register selects the reference voltage. The conversion result is obtained through ADC conversion. The voltage value of VDD can be derived as follows:

$$\text{Conversion result} = （（0.254 * \text{VDD}）/\text{VREF}） \times 4096$$

Then $\text{VDD} = （\text{Conversion result}/4096） / 0.254 \times \text{VREF}$

3.10.2 Explanation of ADC Analog-to-Digital Conversion Settings

1. Enable ADC input ports and select analog channels by setting registers R1A0/P5AE, R1A1/P6AE, and R1A6/ADCON0;
2. Set ADC clock prescaler and reference voltage by configuring register R1A7/ADCON1;
3. If interrupt functionality is needed, set ADIE=1 and execute the “EI” instruction;
4. Set “ADEN=1” to start the AD power supply voltage;
5. Select IDLE/SLEEP mode as needed, and enable AD wake-up function by setting ADCWE=1;
6. Set “ADRUN=1” to start AD conversion;
7. Wait for the interrupt or for ADRUN to be cleared to 0. If an AD interrupt occurs, ADIF must be cleared to 0 when exiting the interrupt routine;
8. Save the conversion results. If multiple AD conversions are needed, jump to step 6;

3.11 LED Dot Matrix Driver

The LED dot matrix driver circuit supports a maximum of 6*7 mode for driving 42 LEDs. The LEDCON register can be configured with LEDDUTY<1:0> to select dot matrix modes of 4*4, 5*5, 6*6, and 6*7. The LED addresses for different sizes of dot matrices remain unchanged (all start from LED0), and the LED data is set by LEDRAM0 to 5. The LED clock source can be selected as either the system clock or the instruction clock, with clock division of 8/16/32/64/128/256 through LEDPSR<2:0>. The brightness of the LEDs can be adjusted using the LED duty cycle register LEDDT<6:0>.

3.11.1 LED Function Description

The LED dot matrix has two main scanning modes. The general 6*7 dot matrix primarily uses a dual-light scanning mode, which lights up two LEDs at a time (common cathode). Other dot matrix modes may alternate between single-light and dual-light scanning modes, lighting up one or two LEDs at a time. LEDRAM0 to 5 correspond to the table showing the lighting status of the corresponding addresses, where 1 indicates the LED is on and 0 indicates it is off.

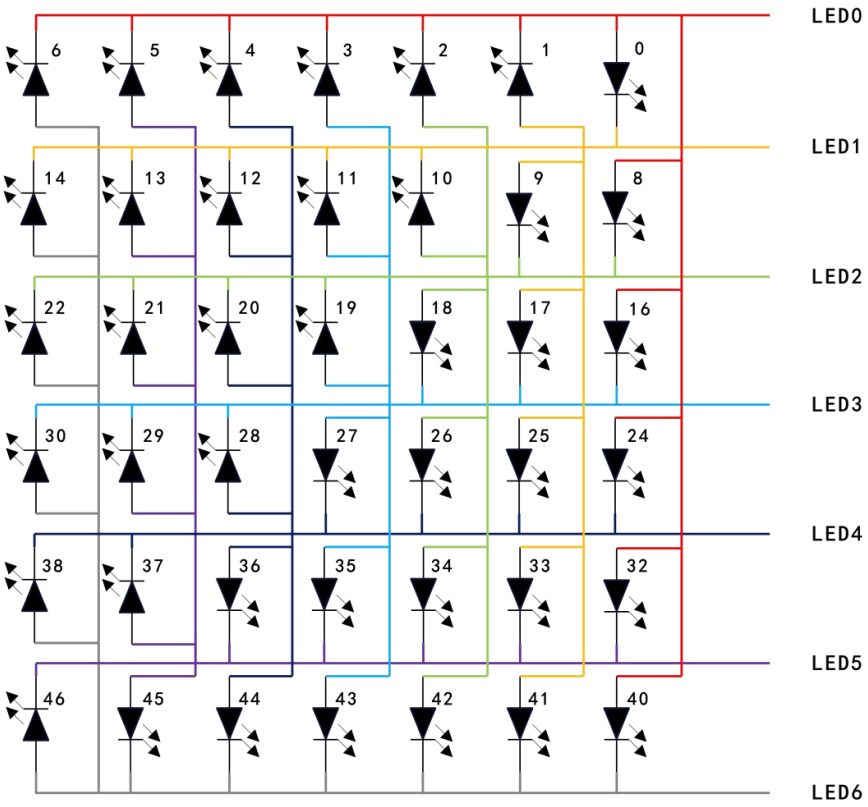
Set the register LEDEN=1 to enable the LED dot matrix mode. Setting LEDDT<6:0> to 0x7F provides the highest brightness.

The correspondence between LED output and ports is shown in the table below:

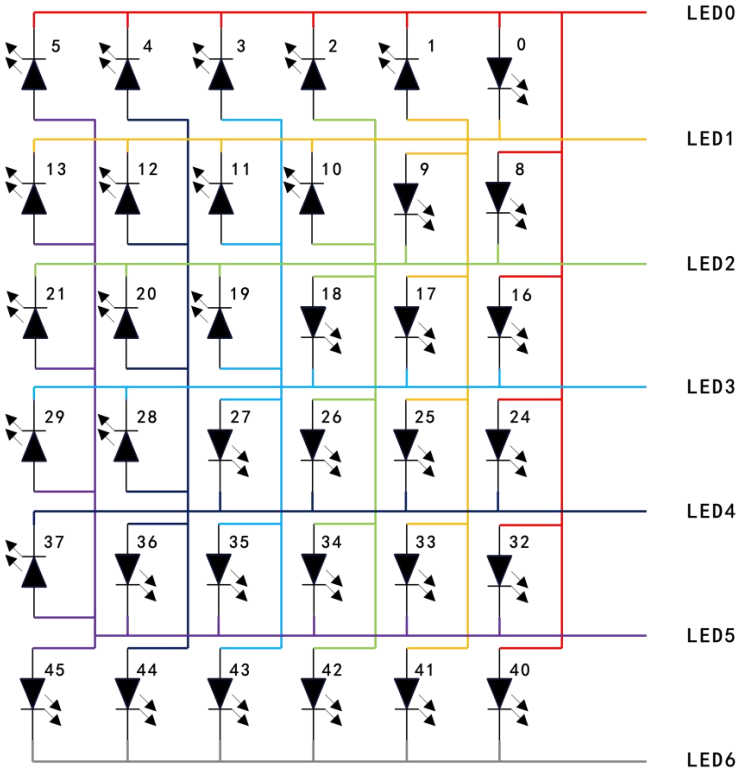
LED0	LED1	LED2	LED3	LED4	LED5	LED6
P66	P67	P50	P51	P52	P53	P54

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDRAM0	-	6	5	4	3	2	1	0
LEDRAM1	-	14	13	12	11	10	9	8
LEDRAM2	-	22	21	20	19	18	17	16
LEDRAM3	-	30	29	28	27	26	25	24
LEDRAM4	-	38	37	35	35	34	33	32
LEDRAM5	-	46	45	44	43	42	41	40

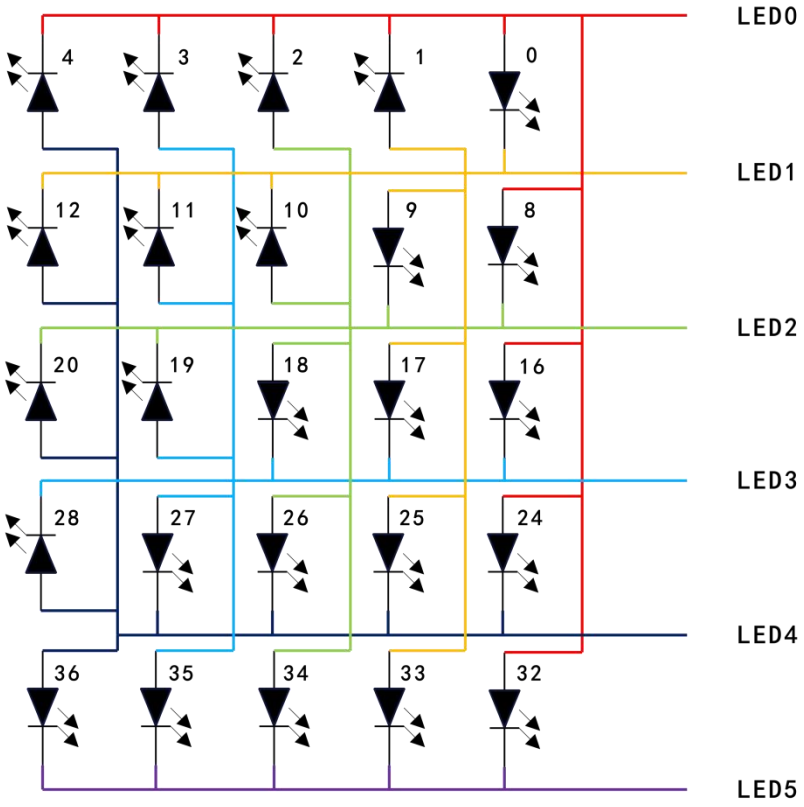
6*7 Matrix:



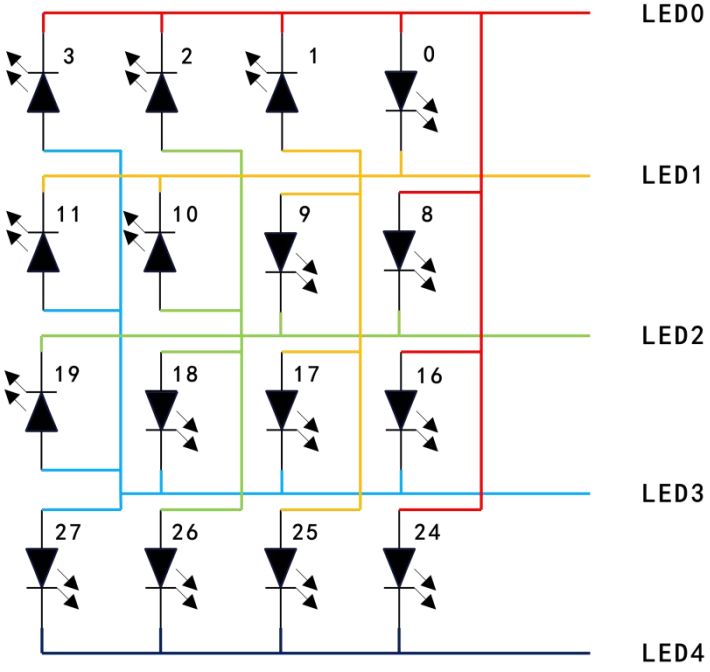
6*6 Matrix:

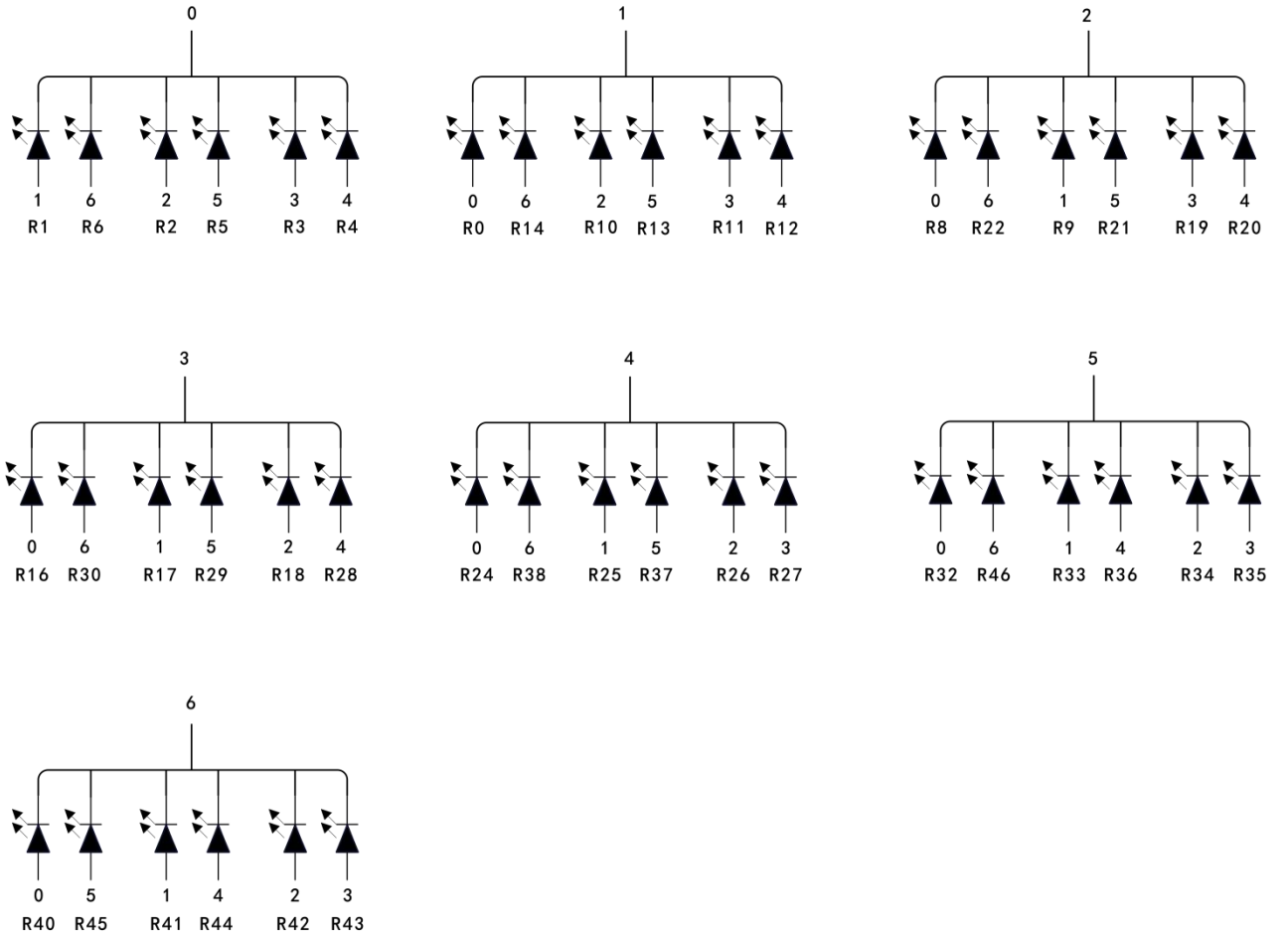


5*5 matrix:



4*4 Matrix:





Dot Matrix Scanning Distribution Diagram

3.11.2 LED Dot Matrix Driver Setup Instructions

1. Set the register LEDRAM0～5 write values to light up the corresponding LED lights.
2. Set the LED duty cycle register LEDDT<6:0> to configure the brightness required for the LED lights.
3. Configure the LED control register to enable the LEDs, set the dot matrix mode, and select the LED clock source and division ratio.

Note:

1. The LED dot matrix module can turn off the lights by disabling LEDEN. Setting the duty cycle LEDDT<6:0> to 0 may cause abnormal light-off;
2. Refer to the dot matrix scanning distribution diagram. When two lights are lit simultaneously, due to the inconsistent electrical characteristics of different colored lights, it may lead to uneven brightness. Users should pay attention to the actual effect during application;

3.12 CMP Comparator

JZ8M2632 has a built-in hardware comparator that can compare any two of the input pins, the internal reference voltage Vinternal R, and 1/2VREF, selecting one as the positive input and the other as the negative input. The negative input of the comparator can be P50, P62, P64, P65, P66, P67, a voltage divider (selected by CMPRS<5:0>), or 1/2VREF. When selecting 1/2VREF as the input, the internal reference voltage is selected through the ADCON1 register VREF<2:0>. The positive input of the comparator can be P51, P53, a voltage divider (selected by CMPRS<5:0>), or 1/2VREF. (When using the comparator function, avoid connecting unused comparator ports to negative voltage, as this may affect comparison accuracy.)

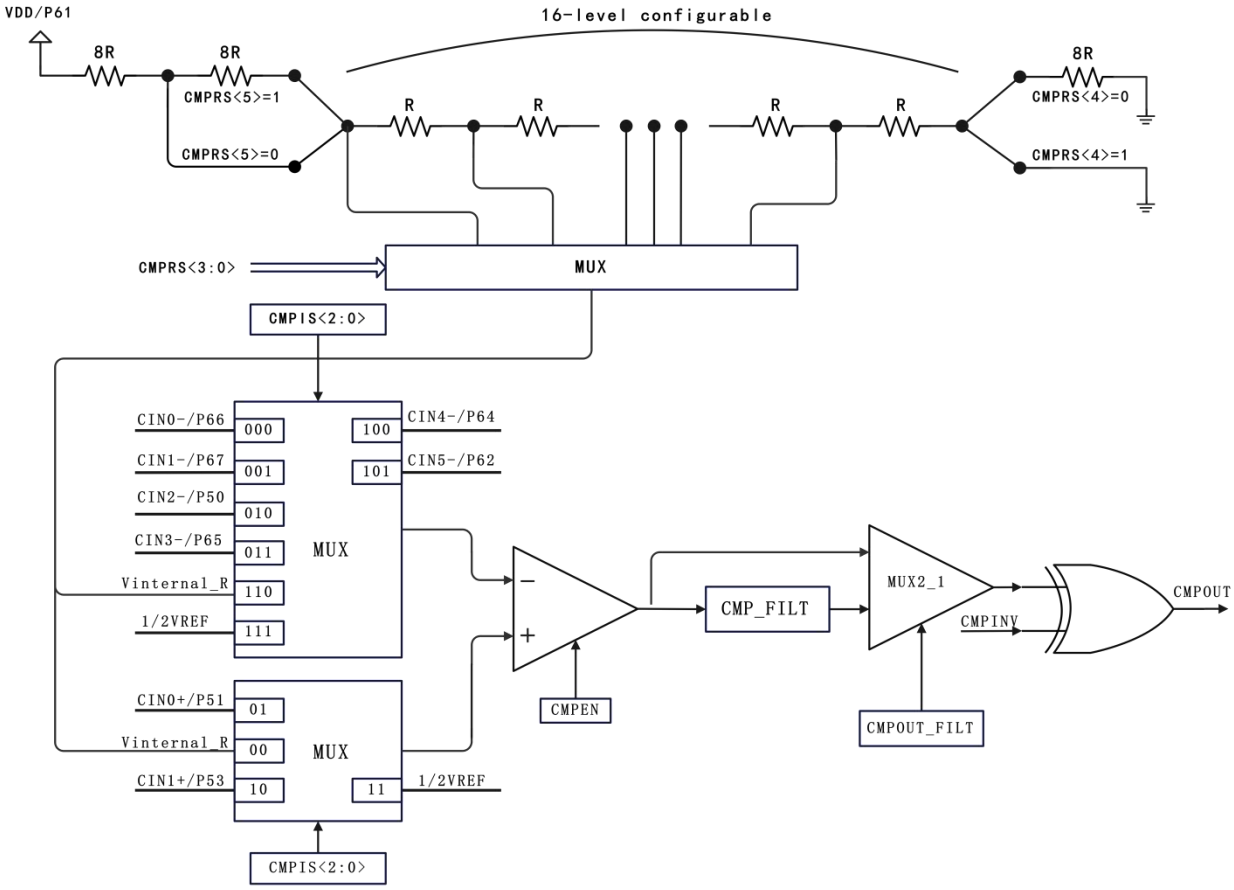
The voltage divider can be configured through the CMPCON control register to select the input voltage source as either the P61 pin input or VDD.

The output result of the comparator can be selected to output from the P67 pin, supporting inverted output. The chip supports digital filtering of the output result, which can be selected in OPTION.

The comparator supports interrupt triggering based on output result changes, enabling CMPIE to generate interrupt signals.

The comparator supports waking up from output result changes, enabling CMPWE to wake up from idle mode and sleep mode. In idle mode and sleep mode, if CMPEN is enabled, it will enable the low-speed oscillator, increasing sleep power consumption.

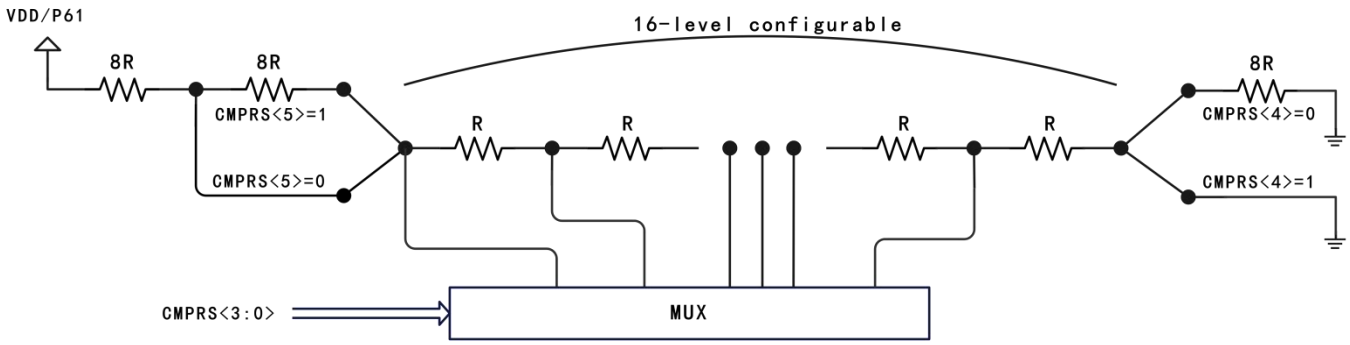
The comparator can select the comparator hysteresis function's level in [OPTION], and the hysteresis function is effective only on the falling edge of the comparison result.



Comparator schematic diagram explanation

3.12.1 Voltage output Vinternal R of the voltage divider

The voltage output Vinternal R of the voltage divider consists of a series of resistors, which can generate different levels of reference voltage. CMPRS<5:0> collectively determines the magnitude of Vinternal R, with CMPRS<5> and CMPRS<4> selecting the maximum and minimum values of Vinternal R, and CMPRS<3:0> used to select the desired voltage level, which is divided into 16 equal parts between the maximum and minimum values of Vinternal R, selected by CMPRS<3:0>.



Comparator tuning schematic diagram

Example 1: CMPRS<5>=0, CMPRS<4>=0

Value range: $V_{internal\ R} = (3/4) * VDD \sim (1/4) * VDD + (1/32) * VDD$

Calculation formula: $V_{internal\ R} = (1/4) * VDD + \frac{(n+1)}{32} * VDD$

Example 2: CMPRS<5>=0, CMPRS<4>=1

Value range: $V_{\mathbf{internal\ R}} = (2/3) * VDD \sim (1/24) * VDD$

Calculation formula: $V_{internal\ R} = \frac{(n+1)}{24} * VDD$

Example 3: CMPRS<5>=1, CMPRS<4>=0

Value range: $V_{\mathbf{internal\ R}} = (3/5) * VDD \sim (1/5) * VDD + (1/40) * VDD$

Calculation formula: $V_{internal\ R} = (1/5) * VDD + \frac{(n+1)}{40} * VDD$

Example 4: CMPRS<5>=1, CMPRS<4>=1

Value range: $V_{\mathbf{internal\ R}} = (1/2) * VDD \sim (1/32) * VDD$

Calculation formula: $V_{internal\ R} = \frac{(n+1)}{32} * VDD$

n=CMPRS<3:0>

3.12.2 Comparator configuration

When using the comparator, CMPEN must be enabled (this will activate LRC for filtering the output result CMPOUT, increasing power consumption). Set CMPIS<5:0> to select the positive and negative input sources, and configure the ports for positive and negative inputs as inputs; the same port cannot be used as both positive and negative inputs simultaneously, and the voltage divider resistor input source cannot be used as both positive and negative at the same time.

If a resistor divider is selected as the input source, configure the register CMPRS<5:0> as needed to select the desired voltage output V_internal R for comparison.

Example 1:

Select P62 as the negative input and V_internal R voltage as (18/32)*VDD as the positive input. Choose the configuration of V_internal R as CMPRS<5>=0, CMPRS<4>=0, and CMPRS<3:0>=4b' 1001 (n=9) to obtain

V_internal R = (1/4)*VDD + [(9+1)/32]*VDD = (18/32)*VDD

Once the configuration is complete, enable the CMPEN bit (Bit7) of the CMPCON0 (R1C8) control register. The comparator will start comparing, and the comparison result can be output through the P67 port by configuring the CMPOE bit (Bit7) of the CMPCON1 (R1C9) control register (the P67 port must be set as output). The output result can also be inverted by configuring the CMPINV bit (Bit6) of this control register.

3.12.3 VREF Usage

The built-in VREF reference voltage can provide 2V/3V/4V. By using 1/2VREF as the reference voltage source for the comparator, it can measure the external power supply voltage level. Specifically, if VREF=2V is selected, then 1/2VREF=1V, and the reference voltage is used as the negative input to compare with the positive input V_internal R. Set the power supply of V_internal R to VDD, and by adjusting the voltage level of V_internal R and comparing it with the Bandgap reference voltage, the voltage of VDD can be determined. If n (CMPRS[3:0] in decimal) is set to make V_internal R closest to 1V, using the four cases in 3.12.1 as an example, the voltage of VDD can be calculated using the following formulas:

For using Case 1: VDD = [32/(n+9)] * 1V;

For using Case 2: VDD = [24/(n+1)] * 1V;

For using Case 3: VDD = [40/(n+9)] * 1V;

For using Case 4: VDD = [32/(n+1)] * 1V;

3.13 RFC Resistance Frequency Conversion

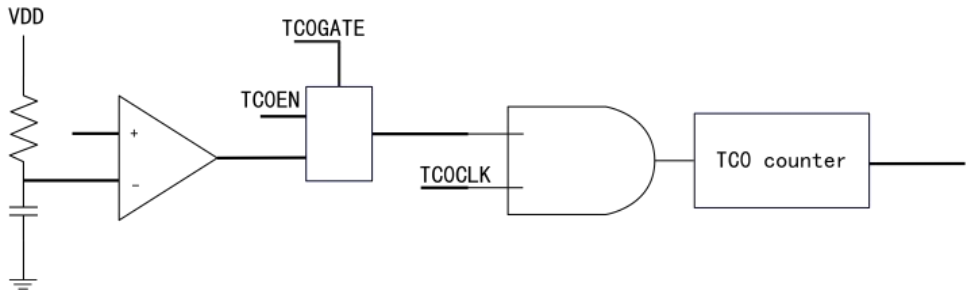
The JZ8M2632 has a built-in RFC resistor frequency conversion function, which controls TC0 capture based on the comparison results of the comparator, enabling time counting for external voltage changes.

RFC Principle:

The change in RFC port voltage affects the output result of the comparator. After enabling the TC0GATE bit in the EXINTCON register, the TC0 count is controlled by the output result CMPOUT of the comparator. When the RFC port voltage is lower than the positive voltage of the comparator, CMPOUT=1 and TC0 starts counting; when the RFC port voltage is higher than the positive voltage of the comparator, CMPOUT=0 and TC0 stops counting. The TC0 count value records the time it takes for the RFC port voltage to charge to the preset voltage value (the positive voltage of the comparator).

Application Steps:

1. Set the P5AE and P6AE registers to select the analog port of the comparator;
2. Set the CMPCON0 and CMPCON1 registers to define the positive input source of the comparator as a fixed voltage, and set the negative input source of the comparator to an external port (as shown in the diagram);
3. Set the output of the port for the negative input source of the comparator to low level to discharge the port capacitor;
4. Clear the initial value of the TC0 timer;
5. Set the port for the negative input source of the comparator as an analog input port to start sampling the RFC port voltage;
6. Read the TC0 count value to calculate the charging time of the RFC port;

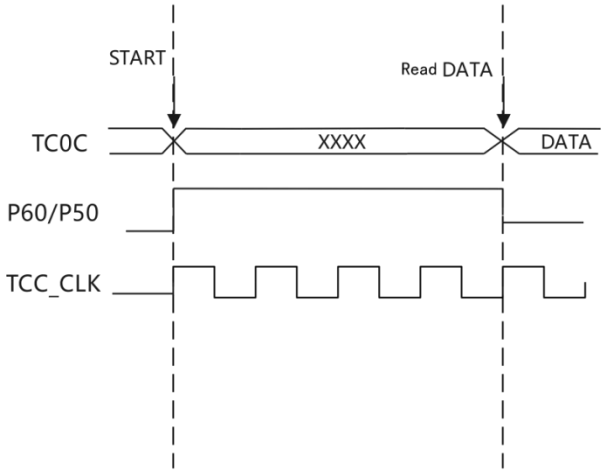


RFC Structure Diagram

3.14 TC0 Port Level Capture

The JZ8M2632 provides external INT0 or INT1 (i.e., P60 or P50) level capture functionality by multiplexing the TC0 8-bit prescaler TPRE (low 8 bits of the level capture counter) and the 8-bit counter TC0C (high 8 bits of the level capture counter) to form a 16-bit level capture counter (the prescaler needs to be enabled and set to 256 division). It also works with the EXINT external interrupt to trigger an interrupt on level changes, allowing the interrupt program to determine the capture time of the previous level.

Set the TC0GATE<0> bit in the EXINTCON register to enable TC0 capture gating, and set CAPS to choose INT0 (P60) or INT1 (P50) as the capture source. Set INT1S/INT0S to select rising edge trigger or falling edge trigger. For rising edge trigger, counting occurs when the external port is low, and counting stops when it is high; an external interrupt is also generated on the rising edge. For falling edge trigger, counting occurs when the external port is high, and counting stops when it is low; an external interrupt is also generated on the falling edge. Users can read the count values from the R185/TC0C and R1AD/TPRE registers in the interrupt program triggered by the edge of the P60/P50 external port to calculate the level time. After reading the values, TC0C and TPRE need to be cleared (by turning TC0PTEN off and on).



P60/P50 Falling Edge Trigger TC0 Capture

3.15 EEPROM and ISP Programming

3.15.1 EEPROM Read and Write Operations

The JZ8M2632 has a built-in 256 Byte 16-bit EEPROM data storage, with the default factory data set to 0xFFFF. It supports real-time reading or writing of data by user programs while powered on. During data writing, the MCU will stop executing instructions and will resume after the writing is complete.

Writing to EEPROM:

Before writing to the EEPROM unit, the user must first write the address to the TBRDL register to select the EEPROM address. Then, write the value to the EEPROM data registers E2PDATL/E2PDATH. Finally, unlock the EEPROM write operation by setting the E2PLOCK bit, setting the E2PWR bit to 1. Once a write process is initiated, clearing the E2PWR bit will not affect the write cycle. When the write cycle is complete, the E2PWR bit will be cleared by hardware and must be manually set by the user before the next write.

Note: During the EEPROM write period, the instruction clock stops, and the MCU does not execute any instructions. The high-speed oscillator and low-speed oscillator operate normally, and the system clock is normal;

Read EEPROM:

To read the EEPROM memory cell, the user must first write the address into the TBRDL register and set the E2PRD bit of the E2PCON register to 1. After enabling the read control bit, execute the TBRD instruction, and the data from the EEPROM will be stored in the corresponding R (high 8 bits of data) and ACC (low 8 bits of data).

3.15.2 ISP Programming

The JZ8M2632 supports three different programming methods: conventional programming (off-board), in-circuit programming without power, and in-circuit programming with power. For in-circuit programming with power, the user must configure the programming port and functionality in advance.

1、 Conventional Programming (Off-Board):

In the OPTION settings, select [Programming Port Settings] to choose [P60/P65 as non-programming ports, not supporting in-circuit programming with power], and in the OPTION settings, select [Programming Function Selection] to choose [Conventional Programming (powered by the programmer)]. The above configuration does not affect the use of ports P60/P65.

2、 In-Circuit Programming Without Power:

In the OPTION settings, select [Programming Port Settings] to choose [P60/P65 as non-programming ports, not supporting in-circuit programming with power], and in the OPTION settings, select [Programming Function Selection] to choose [Conventional Programming (powered by the programmer)]. The above configuration requires P60/P65 to be set as input ports as much as possible to avoid external components like transistors or MOSFETs.

3、 In-Circuit Programming With Power:

In-circuit programming with power requires the MCU to pre-select "Conventional Programming" to program the software. It cannot be programmed with an empty chip. In the in-circuit programming mode with power, the programmer needs to connect three wires: GND, P60, and P65, while VDD should not be connected. The following two programming methods are supported.

Method One: P60/P65 serves as the programming port only during reset, and the program can be used.

OPTION option [Burning Port Settings] select [P60/P65 only as burning port (program can be used only during reset)], OPTION option [Burning Function Selection] select [Burning while powered on], the instruction clock (Fcpu) frequency must be greater than 1M (e.g., IRC frequency = 16M, Clocks division

= 4 Clocks). With the above configuration, P60/P65 can be used as GPIO normally, and the program needs to configure specific registers and enable external interrupt 0 (INT0) to receive the clock data sent by the programmer. After correct decoding, the software unlocks the ISP function, see ISP demo for details.

The software unlock of ISP mainly consists of the following two steps:

1) The program writes 0110 to the high 4 bits E2PLOCK<3:0> of the E2PCON (0x1CA) register to complete the first step of unlocking;

2) The program writes 0xC5 to the E2PDATH (0x1CC) register and then writes 0x3A to the E2PDATL (0x1CB) register to complete the second step of unlocking;

After completing the two steps of unlocking, the MCU hardware will set P60 and P65 as input ports, and then wait for external timing to control the MCU reset.

Method Two: P60/P65 only as burning port, program uncontrollable

OPTION option [Burning Port Settings] select [P60/65 only as burning port (hardware pull-up, program uncontrollable), chip can switch to burning mode at any time], OPTION option [Burning Function Selection] select [Burning while powered on]. With the above configuration, P60/P65 needs to be left floating; if Type-C port upgrade is needed, then P60/P65 connects to CC1/CC2 ports.

Note: The P60/P65 burning port has a default hardware pull-up, and the program cannot control it; external pull-down will cause leakage.

According to the Type-C port model, choose the appropriate powered burning method. For example, for powered burning via Type-C port:

1) If P60/P65 connects to the CC1/CC2 of the Type-C port and has a pull-down resistor, please choose Method One for software control;

2) If there are no pull-down resistors on the CC1/CC2 of the Type-C port, please choose method two;

3) If P60/P65 connects to Type-C port D+/D-, please select option two;

4 OPTION Configuration Table

CODE OPTION	Option	Function Description
Watchdog	Enable	Watchdog WDT Enable
	Disabled	Watchdog WDT Disable
Clocks Division	2 Clocks	Instruction Clock Division Select 2 Clocks
	4 Clocks	Instruction Clock Division Select 4 Clocks
	8 Clocks	Instruction clock division selection 8 Clocks
	16 Clocks	Instruction clock division selection 16 Clocks
	32 Clocks	Instruction clock division selection 32 Clocks
IRC Frequency	1M	IRC frequency selection 1M
	4M	IRC frequency selection 4M
	8M	IRC frequency selection 8M
	16M	IRC frequency selection 16M
Low Voltage Reset Option	Enabled: LVR always	Default LVR function is always enabled
	Enabled: Software control	LVR enable bit can be modified by software, attention to dead zone is required
Low Voltage Reset	LVR=1.8V	Low Voltage Reset point selection 1.8V
	LVR=2.0V	Low Voltage Reset point selection 2.0V
	LVR=2.2V	Low Voltage Reset Point Selection 2.2V
	LVR=2.5V	Low Voltage Reset Point Selection 2.5V
	LVR=2.9V	Low Voltage Reset Point Selection 2.9V
	LVR=3.3V	Low Voltage Reset Point Selection 3.3V
	LVR=3.6V	Low Voltage Reset Point Selection 3.6V
	LVR=3.8V	Low Voltage Reset Point Selection 3.8V
Reset Time	PWRT=13ms, WDT=25ms	Reset establishment time=13ms, WDT overflow time=25ms (4x frequency)
	PWRT=51ms, WDT=102ms	Reset establishment time=51ms, WDT overflow time=102ms (4x frequency)
	PWRT=205ms, WDT=409ms	Reset establishment time=205ms, WDT overflow time=409ms (4x frequency)
	PWRT=350us, WDT=6.5ms	Reset establishment time=350us, WDT overflow time=6.5ms (4x frequency)
	PWRT=350us, WDT=25ms	Reset establishment time=350us, WDT overflow time=25ms (4x frequency)
	PWRT=350us, WDT=102ms	Reset establishment time=350us, WDT overflow time=102ms (4 frequency division)

	PWRT=350us, WDT=409ms	Reset establishment time=350us, WDT overflow time=409ms (4 frequency division)
LED port drive level 1	Enable	Port drive level 1 enhancement function enabled
	Disabled	Port drive level 1 enhancement function disabled
LED port drive level 2	Enable	Port drive level 2 enhancement function enabled
	Disabled	Port drive level 2 enhancement function disabled
CMP_FILT	Enable	Comparator Result Digital Filtering Enable
	Disabled	Comparator Result Digital Filtering Disable
Programming Mode Selection	FLASH	Program Only FLASH Area
	EEPROM	Program Only EEPROM Area, EEPROM Supports
	FLASH+EEPROM	Program FLASH+EEPROM Area
Programming Port Settings	P60/P65 is not used as a programming port	P60/P65 does not have a programming interface and does not support in-circuit programming while powered on.
	P60/P65 only during reset Programming Port Burning port	P60/P65 only during reset Programming port (can be used by the program) Burning port
	P60/P65 is for programming only	P60/P65 is only for programming (the program cannot control it). The chip can switch to programming mode at any time.
Burning Function Selection	Regular Programming	Conventional programming (programmer powered programming)
	In-circuit programming	In-circuit programming
OS testing	Enable	OS testing enabled, check all pin contacts
	Disabled	OS testing disabled, only detect programming pins
Power-on time selection	Fast power-on	Capacitance between power ground ≤ 50uF
	Slow power-on	50uF ≤ Capacitance between power ground ≤ 470uF

Notes on programming option [Power-up Time Selection]:

1) If [Power-up Time Selection] is set to [Fast Power-up], then [Reset Time] can be chosen arbitrarily;
2) If [Power-up Time Selection] is set to [Slow Power-up], then [Reset Time] must be one of [PWRT=13ms/51ms/205ms];
3) If during the first programming, [Power-up Time Selection] is set to [Fast Power-up] + [PWRT=350us], and during the second programming, [Power-up Time Selection] is desired to be [Slow Power-up], then it is necessary to first program with [Fast Power-up] + [PWRT=13ms] (the purpose is to set the chip to a long reset time), and then select [Slow Power-up] for programming;

5 Instruction Set

Instruction	Instruction Action	Flag Bit Impact
ADD A,R	A+R→A	Z,C,DC
ADD R,A	A+R→R	Z,C,DC
AND A,R	A&R→A	Z
AND R,A	A&R→R	Z
CLRA	0→A	Z
CLR R	0→R	Z
INVA R	/R→A	Z
INV R	/R→R	Z
DA	A register adjusted to BCD value	C
DECA R	R-1→A	Z
DEC R	R-1→R	Z
DJA R	R-1→A, skip if zero	-
DJ R	R-1→R, skip if zero	-
INCA R	R+1→A	Z
INC R	R+1→R	Z
IJA R	R+1→A, skip if zero	-
IJ R	R+1→R, skip if zero	-
MOV R,A	A→R	-
MOV A,R	R→A	Z
MOV R,R	R→R	Z
OR A,R	A∨R→A	Z
OR R,A	A∨R→R	Z
SUB A,R	R-A→A	Z,C,DC
SUB R,A	R-A→R	Z,C,DC
XOR A,R	A⊕R→A	Z
XOR R,A	A⊕R→R	Z
BTC R,b	0→R(b)	-
BTS R,b	1→R(b)	-
JBTC R,b	if R(b)=0, skip	-
JBTS R,b	if R(b)=1, skip	-

LCR R	R(n)→R(n+1),R(7)→C, C→R(0)	C
LCA R	R(n)→A(n+1),R(7)→C, C→A(0)	C
RCR R	R(n)→R(n-1),R(0)→C, C→R(7)	C
RCA R	R(n)→A(n-1),R(0)→C, C→A(7)	C
SWAP R	R(0-3) ↔ R(4-7)	-
SWAPA R	R(0-3)→A(4-7),R(4-7)→A(0-3)	-
ADD A,k	A+k→A	Z,C,DC
AND A,k	A&k→A	Z
MOV A,k	k→A	-
OR A,k	A∨k→A	Z
SUB A,k	k-A→A	Z,C,DC
XOR A,k	A⊕k→A	Z
CALL k	PC+1→[SP], (Page,k)→PC	-
DI	Interrupt Disabled	-
EI	Enable Interrupt	-
JMP k	K (Page,k)→PC	-
NOP	No Operation	-
RET	[Stack Top]→PC	-
RETI	[Stack Top]→PC, enable interrupt	-
RETL k	k→A,[Stack Top]→PC	-
SLEEP	0→WDT, oscillator stops oscillating (sleep mode)	T,P
CWDT	0→WDT	T,P
TBRD R	Machine code bit7～0 to ACC Machine code bit15～8 to R (general-purpose register)	-

Note: The execution of the instruction changes the value of the program counter ("MOV R182,A", "ADD R182,A", "JMP *", "CALL*") or performs arithmetic or logical operations on R182 (for example, "SUB R182,A", "BTS(C) R182,3", "CLR R182"). Otherwise, executing all instructions only occupies a single instruction cycle (one instruction cycle consists of 2 oscillation cycles).

6 Electrical Characteristics

6.1 Limit Parameters

Operating Temperature..... -40℃～85℃
Storage Temperature..... -40℃～125℃
Input Voltage..... Vss-0.3V～Vdd+0.5V
Output Voltage..... Vss-0.3V～Vdd+0.5V
Operating Voltage..... 1.8V-5.5V

6.2 Electrical Characteristics

(VDD =5V, Operating Temperature=25℃, unless otherwise specified)
Operating Characteristics

Parameter		Minimum	Typical	Maximum	Unit	Condition
System Clock (SYSCK)		-	16	-	MHz	[Oscillation Mode] Select IRC mode, frequency value is selected through [IRC Frequency]
		-	8	-	MHz	
		-	4	-	MHz	
		-	1	-	MHz	
Instruction Clock (Fcpu)	2T	-	-	8	MHz	VDD=2.9V～5.5V
	4T/8T	-	-	4	MHz	VDD=2.5V～5.5V
	16T/32T	-	-	2	MHz	VDD=2.0V～5.5V
Power-on reset hold time			350		μs	PWRT independent time
		Reset time=WDT overflow			ms	PWRT=WDT
External reset pulse		2			μs	25℃

Low Voltage Reset (LVR)

Parameter	Minimum	Typical	Maximum	Unit	Condition
ILVR		0.8		uA	25℃, VDD= 5V
LVR threshold	-10%	1.8	+10%	V	25℃
	-10%	2.0	+10%		
	-10%	2.2	+10%		
	-10%	2.5	+10%		
	-15%	2.9	+15%		
	-15%	3.3	+15%		
	-15%	3.6	+15%		
	-15%	3.8	+15%		
LVR delay	50	-	120	μs	25℃, VDD = 1.8V-5V

Note: To avoid process fluctuations, please leave a margin in the actual product

I/O port circuit

Parameter		Minimum	Typical	Maximum	Unit	Condition
VIL		0	-	0.25*VDD	V	
VIH		0.54*VDD	-	VDD	V	
Source current	General		17.5			
	L0 (LED		9.5		mA	25℃, VDD=5V, VOH=4.4V
	L1 (LED		17.5			
	L2 (LED		25			
Sourcing current	General		31.5		mA	25℃, VDD=5V, VOH=0.6V
	L0 (LED		13.5			
	L1 (LED		34			
	L2 (LED		50			
Pull-up resistor (P5/P6/P7)			90		KΩ	25℃, VDD=5V
Pull-down resistors			90		KΩ	25℃, VDD=5V

LED ports: P50, P51, P52, P53, P54, P66, P67.

General ports: P55, P60, P61, P62, P63, P64, P65.

Operating current (IDD)

Parameter	SYSCK	Minimum	Typical	Maximum	Unit
Normal mode (4T)	16 MHz	-	1.1	-	mA
	8 MHz	-	0.7	-	
	4 MHz	-	0.33	-	
	1 MHz	-	0.32	-	
	40 KHz	-	12	-	uA
Sleep mode (WDT off, LVR on)	-	-	1.5	3	uA
Sleep mode (WDT on, LVR on)	-	-	6.2	-	
Sleep mode (WDT off, LVR on, ADC on)	-	-	120	-	
Sleep mode (WDT off, LVR on, CMP on)	-	-	35	-	

MTP and EEPROM

Parameter		Minimu	Typica	Maximu	Unit	Condition
VDD-READ	MTP/EEPROM	1.8	-	5.5	V	25℃, FCPU≤8MHz
VDD-WRIT	MTP	2.5	-	5.5	V	25℃
	EEPROM	2.5	-	5.5	V	25℃
Endurance	MTP/EEPROM		10000		Times	25℃
Retention	MTP/EEPROM		10		Years	25℃
T_{WRI} Fast Write	MTP/EEPROM		4.5		ms	25℃
T_{WRI} Slow Write	MTP/EEPROM		7.5		ms	25℃
T_{ERASE} Erase Time	MTP/EEPROM		1.5		ms	25℃
IP/E Erase Current	MTP/EEPROM		2.5		mA	25℃, V DD = 5V

6.3 AD Conversion Characteristics

(VDD = 5V, VSS = 0V, Operating Temperature = 25℃)

Symbol	Parameter Description	Condition	Minimum	Typical	Maximum	Unit
VDD	ADC Operating Voltage	-	2.5	-	5.5	V
I_{VDD}	ADC Operating Current	VDD = VREF = 5V	-	110	-	uA
V_{AIN}	Simulated input voltage	-	VSS	-	VREF	V
EXVREF	External reference	-	2.0	-	VDD	V
VREF	Reference voltage output	2V, 3V, 4V	-	±1	±2	%
T_{AD}	AD clock cycle	VDD=2.5～5.5V	1	-	-	us
T_{CN}	AD conversion time	VDD=2.5～5.5V	-	16	-	TAD
RN	Resolution	-	-	12	-	Bit
VDDmin	Minimum supply voltage	-	-	VREF+0.5	-	V
E_{IL}	Integral Error	VDD = VREF = 5V	-	±8.0	-	LSB
E_{DL}	Differential Error		-	±4.0	-	LSB
E_{OFF}	Offset Error		-	±5.0	-	LSB
E_{GN}	Gain Error		-	±2.0	-	LSB

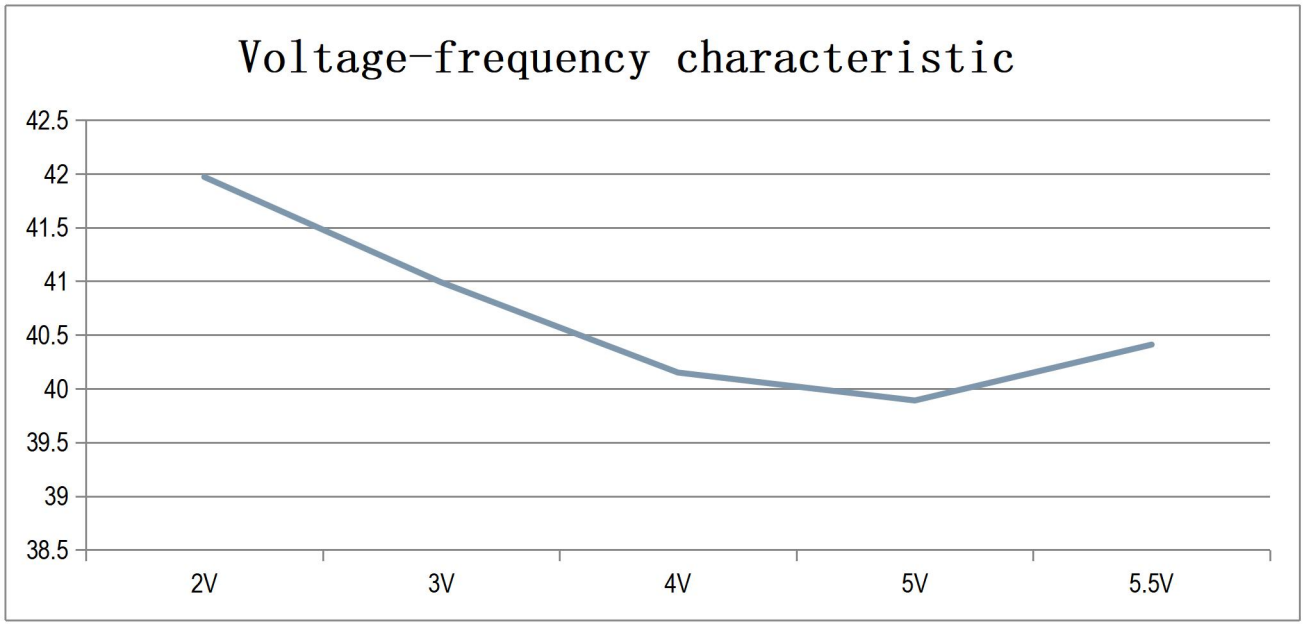
Note: The error is derived from evaluation and is not tested during production.

6.4 Characteristic Curves

The curves listed in this chapter are for design reference only. Some of the data provided may exceed the specified operating range of the chip. To ensure the normal operation of the chip, please strictly refer to the electrical characteristics description.

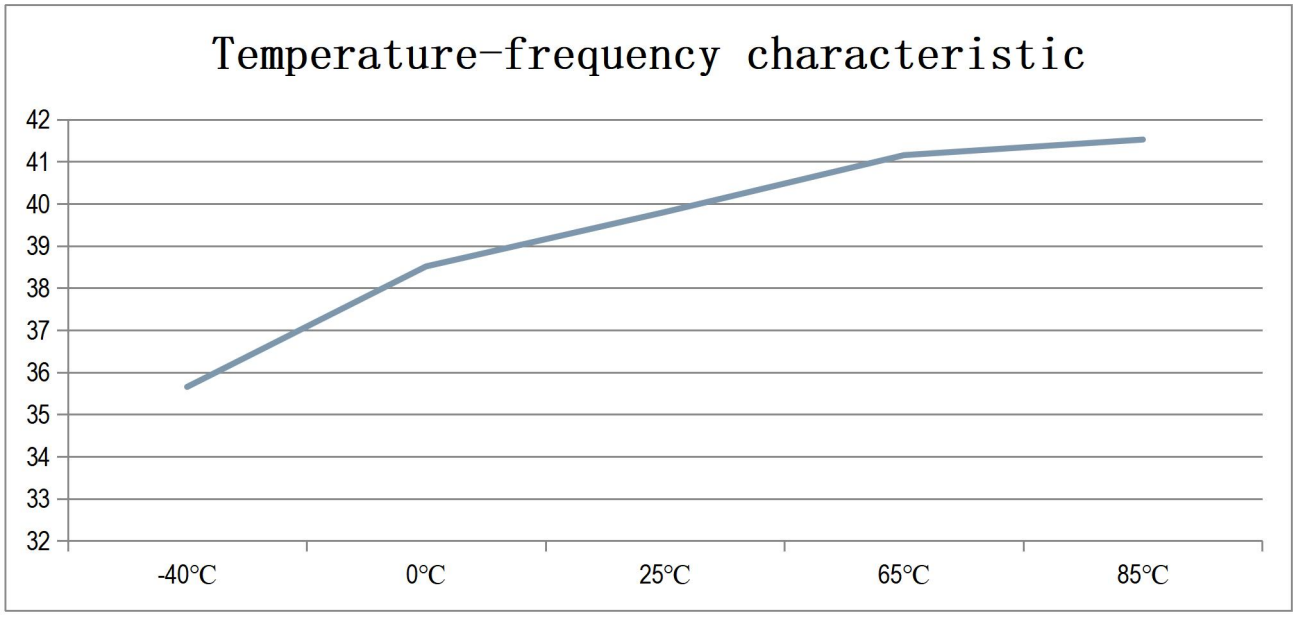
6.4.1 Internal Low-Speed Oscillator – Frequency Characteristics Curve

Operating temperature at 25° C: (Unit: kHz)



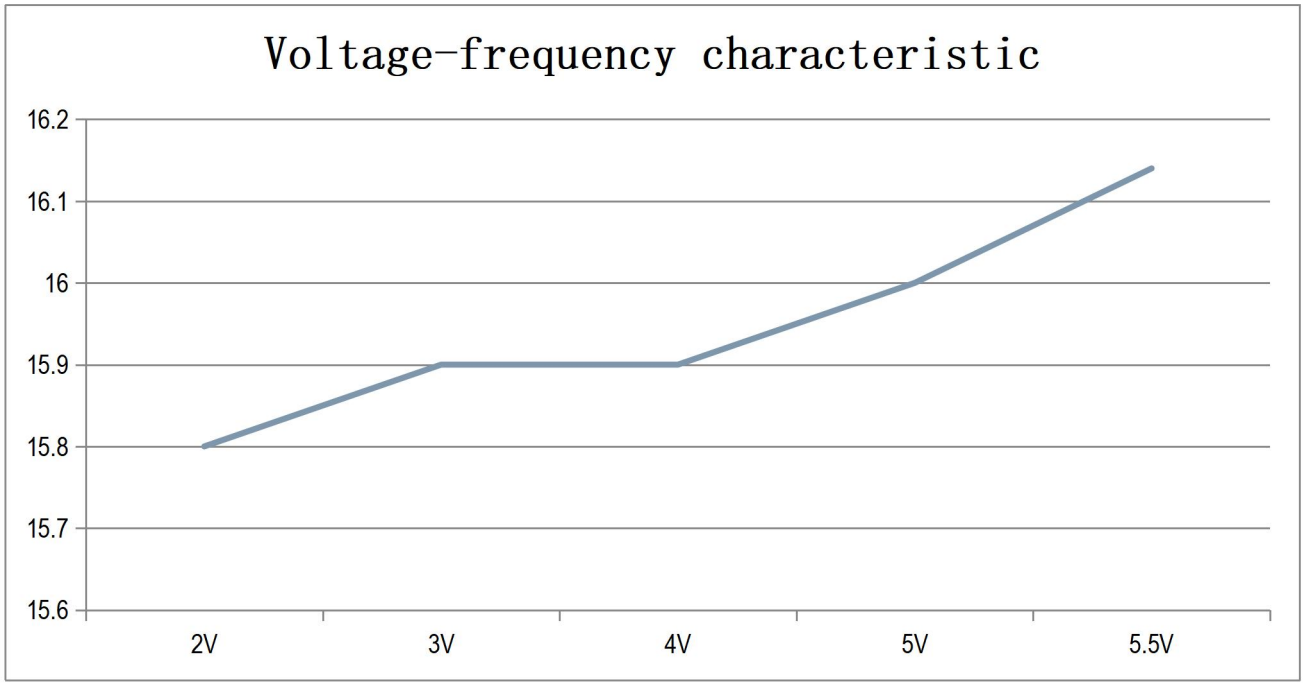
6.4.2 Internal Low-Speed Oscillator – Temperature Characteristics Curve

Operating voltage at 5V: (Unit: kHz)



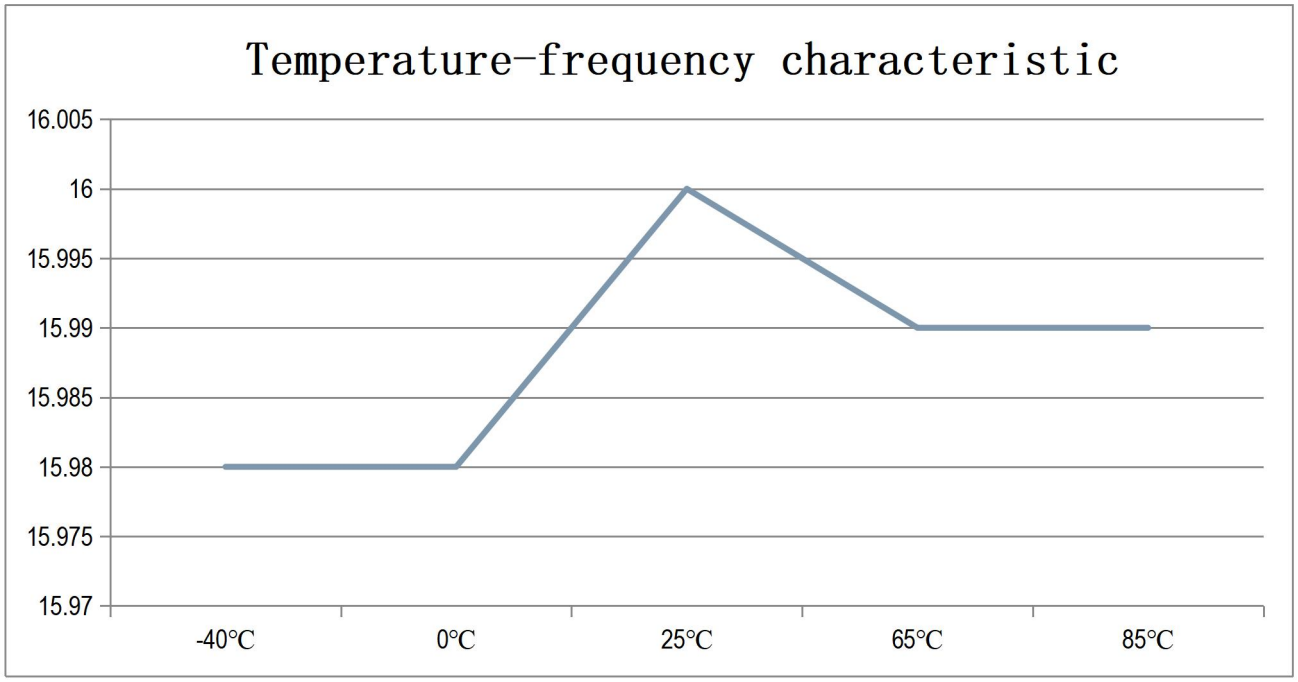
6.4.3 Internal 16MHz RC Oscillator - Frequency Characteristics Curve

Operating temperature at 25℃ conditions: (Unit: MHz)



6.4.4 Internal 16MHz RC oscillator - Temperature frequency characteristic curve

Operating voltage at 5V conditions: (Unit: MHz)



6.5 IHRC frequency tuning parameter description

Parameter description is for reference of variation trends only; actual values may vary.

IHRCCAL tuning value (Hexadecimal)	Frequency (MHz)	Tuning deviation
00	12.92	-21.87%
01	12.96	-21.63%
02	13.00	-21.36%
03	13.04	-21.14%
04	13.09	-20.82%
05	13.13	-20.57%
06	13.18	-20.28%
07	13.22	-20.03%
08	13.27	-19.71%
09	13.32	-19.44%
0A	13.37	-19.16%
0B	13.41	-18.89%
0C	13.46	-18.57%
0D	13.51	-18.29%
0E	13.56	-18.00%
0F	13.61	-17.70%
10	13.67	-17.29%
11	13.72	-16.99%
12	13.77	-16.69%
13	13.82	-16.42%
14	13.87	-16.10%
15	13.92	-15.79%
16	13.97	-15.52%
17	14.02	-15.20%
18	14.08	-14.84%
19	14.13	-14.53%
1A	14.18	-14.23%
1B	14.23	-13.95%
1C	14.28	-13.62%
1D	14.34	-13.24%
1E	14.39	-12.95%
1F	14.45	-12.63%
20	14.54	-12.07%
21	14.59	-11.75%
22	14.65	-11.39%
23	14.71	-11.05%

24	14.77	-10.67%
25	14.83	-10.33%
26	14.88	-9.97%
27	14.94	-9.65%
28	15.00	-9.28%
29	15.06	-8.93%
2A	15.12	-8.54%
2B	15.17	-8.23%
2C	15.24	-7.81%
2D	15.31	-7.43%
2E	15.36	-7.08%
2F	15.43	-6.67%
30	15.51	-6.20%
31	15.58	-5.77%
32	15.64	-5.43%
33	15.70	-5.02%
34	15.77	-4.59%
35	15.83	-4.23%
36	15.90	-3.82%
37	15.97	-3.40%
38	16.04	-2.96%
39	16.11	-2.59%
3A	16.18	-2.17%
3B	16.24	-1.75%
3C	16.32	-1.27%
3D	16.39	-0.87%
3E	16.47	-0.40%
3F	16.53	0.00%
40	16.67	0.82%
41	16.74	1.26%
42	16.81	1.69%
43	16.89	2.13%
44	16.97	2.62%
45	17.05	3.11%
46	17.12	3.54%
47	17.19	3.98%
48	17.28	4.54%
49	17.35	4.96%
4A	17.44	5.50%
4B	17.52	5.96%
4C	17.61	6.51%
4D	17.69	7.00%
4E	17.77	7.49%

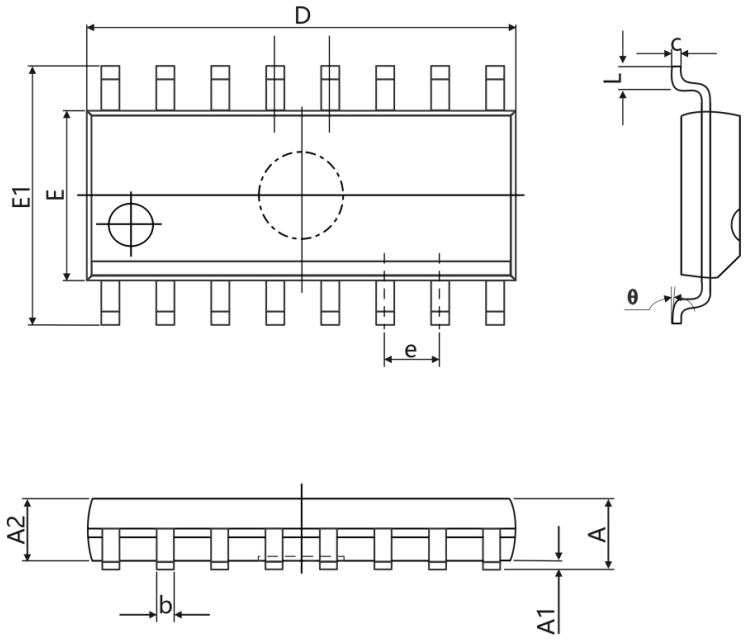
4F	17.86	8.01%
50	17.98	8.74%
51	18.06	9.20%
52	18.14	9.72%
53	18.23	10.24%
54	18.32	10.81%
55	18.41	11.35%
56	18.51	11.92%
57	18.59	12.43%
58	18.69	13.02%
59	18.79	13.63%
5A	18.88	14.22%
5B	18.97	14.70%
5C	19.07	15.34%
5D	19.17	15.96%
5E	19.29	16.66%
5F	19.37	17.13%
60	19.55	18.23%
61	19.65	18.84%
62	19.76	19.50%
63	19.86	20.14%
64	19.98	20.84%
65	20.08	21.44%
66	20.21	22.24%
67	20.31	22.87%
68	20.44	23.61%
69	20.54	24.25%
6A	20.66	24.93%
6B	20.77	25.63%
6C	20.89	26.35%
6D	21.02	27.10%
6E	21.12	27.76%
6F	21.24	28.46%
70	21.41	29.52%
71	21.52	30.16%
72	21.64	30.87%
73	21.76	31.63%
74	21.90	32.45%
75	22.02	33.19%
76	22.16	34.00%
77	22.29	34.80%
78	22.42	35.62%
79	22.57	36.51%

7A	22.70	37.31%
7B	22.83	38.11%
7C	22.99	39.05%
7D	23.12	39.83%
7E	23.25	40.59%
7F	23.39	41.48%

7 Package Size

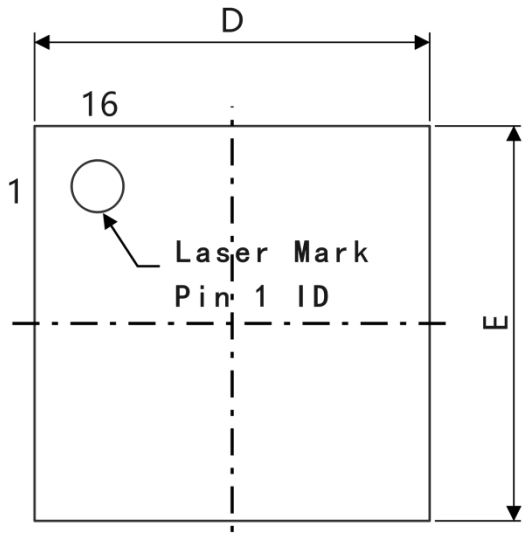
7.1 16PIN package size

(Unit: mm)

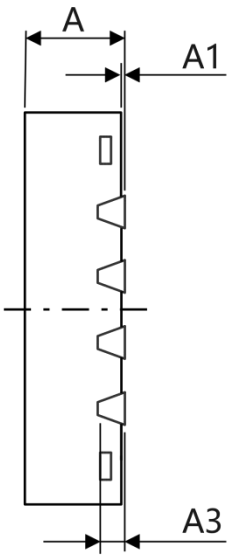


Symbol	Dimensions In Millimeter		Dimensions In Lnches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

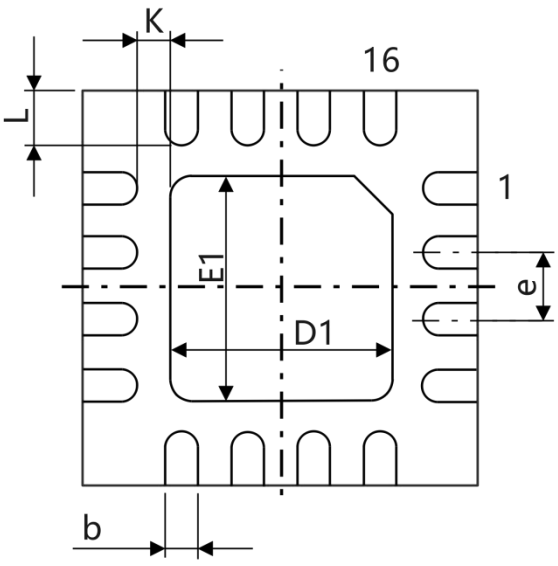
SOP16 Package Dimensions



Top View



Side View



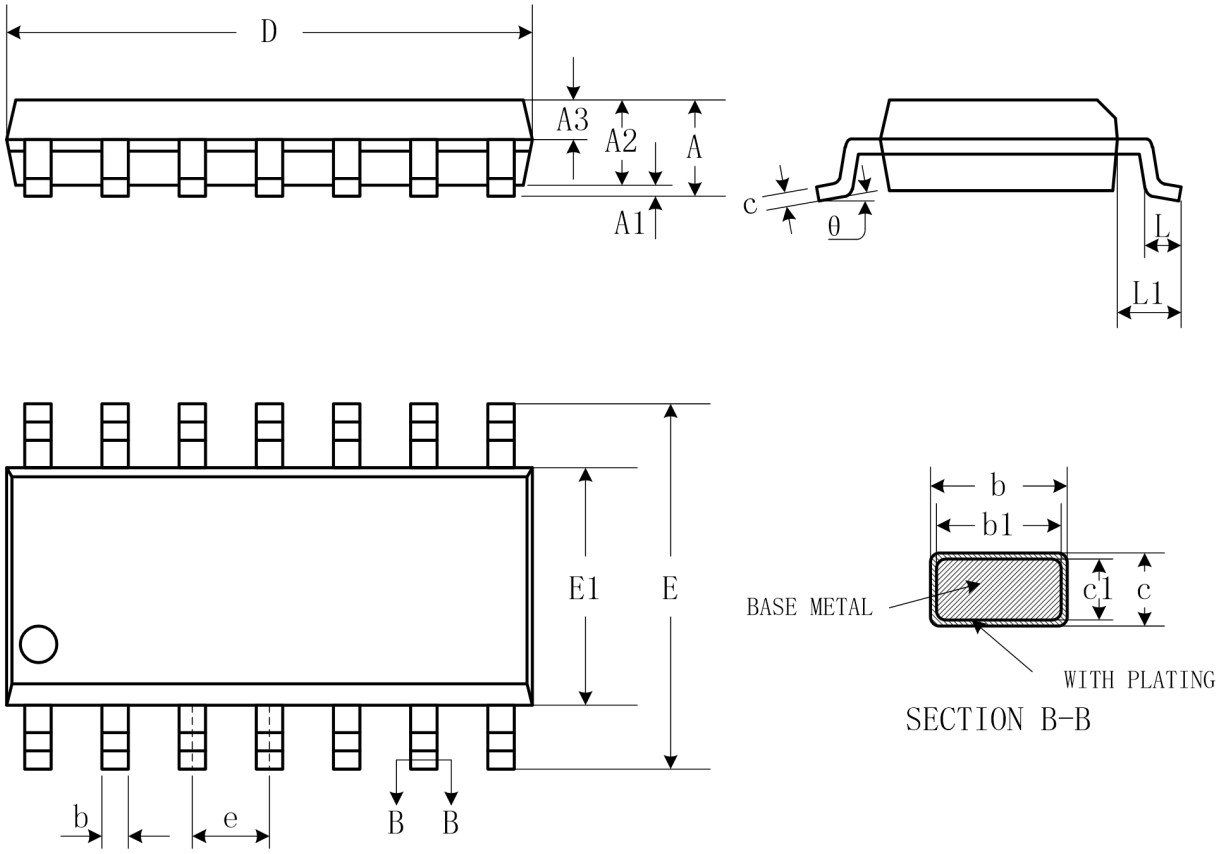
Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e	0.50TYP		
K	0.20	—	—
L	0.30	0.40	0.50

QFN16 Package Dimensions

7.2 14PIN Package Dimensions

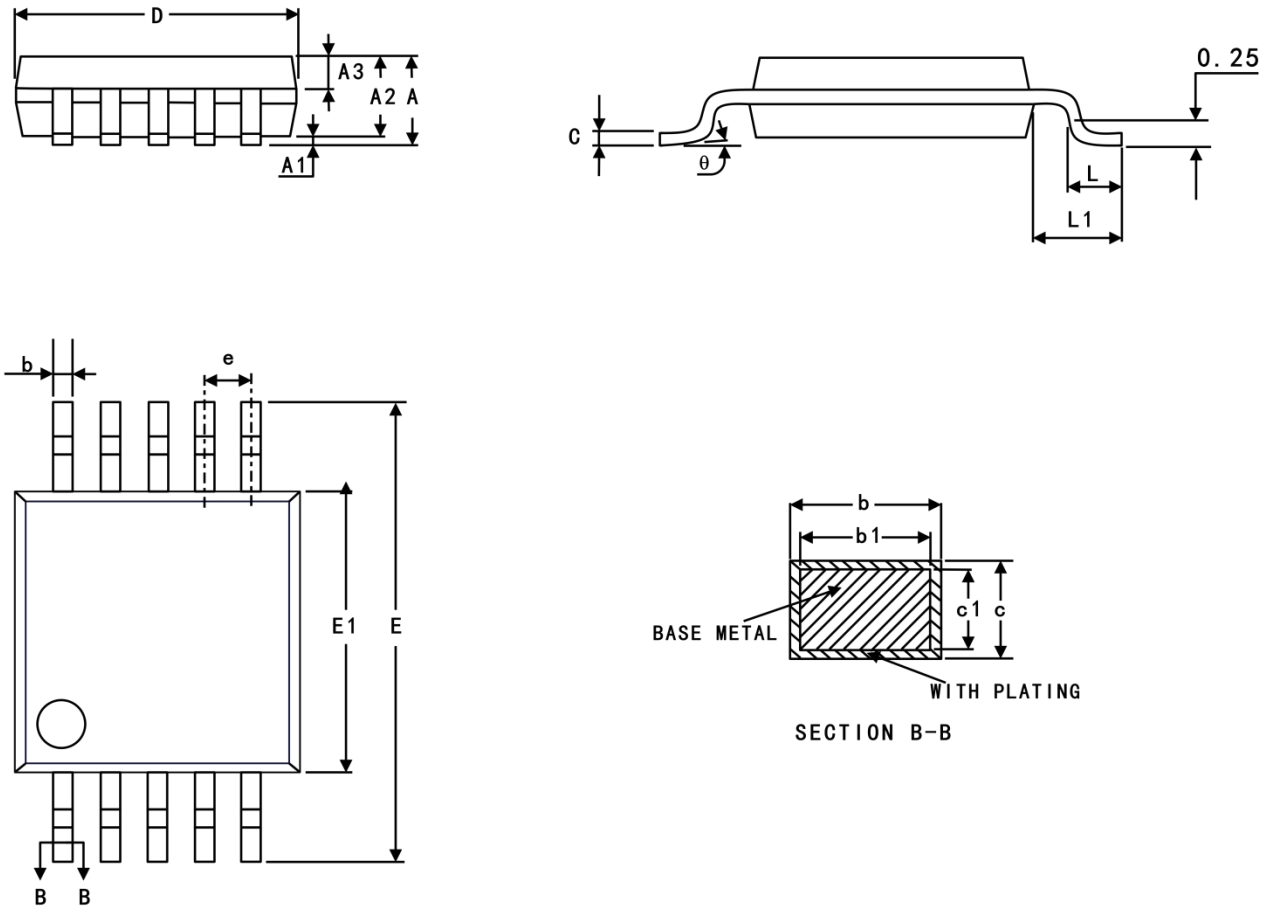
SOP14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	-	8°

SOP14 package size

7.3 10PIN package size

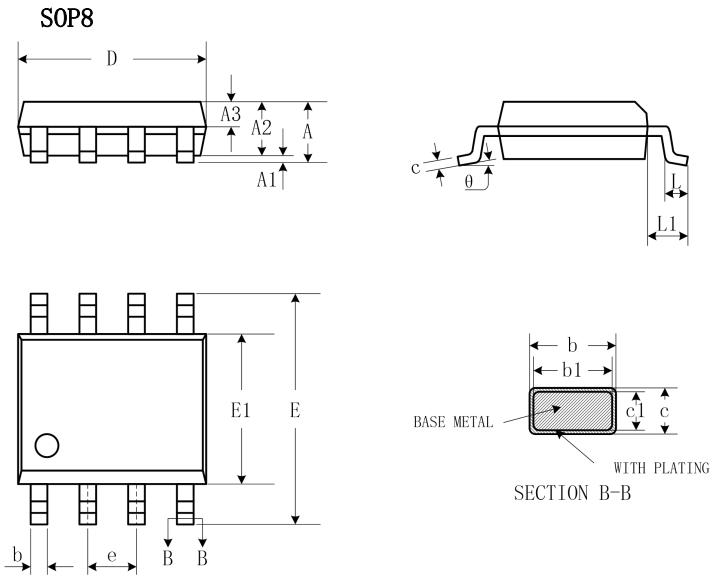


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	_	_	1.10
A1	0.05	_	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18	_	0.26
b1	0.17	0.20	0.23
c	0.15	_	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.50BSC		
L	0.40	_	0.70
L1	0.95REF		
θ	0	-	8°

MSOP10 package size

7.4 8PIN package size

(Unit: mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	-	8°

SOP8 Package Dimensions